SWTEST 2026 CONFERENCE

35th ANNIVERSARY

A Novel Advanced Probe Card Approach for Multi-Temperature HBM Testing

SK hynix

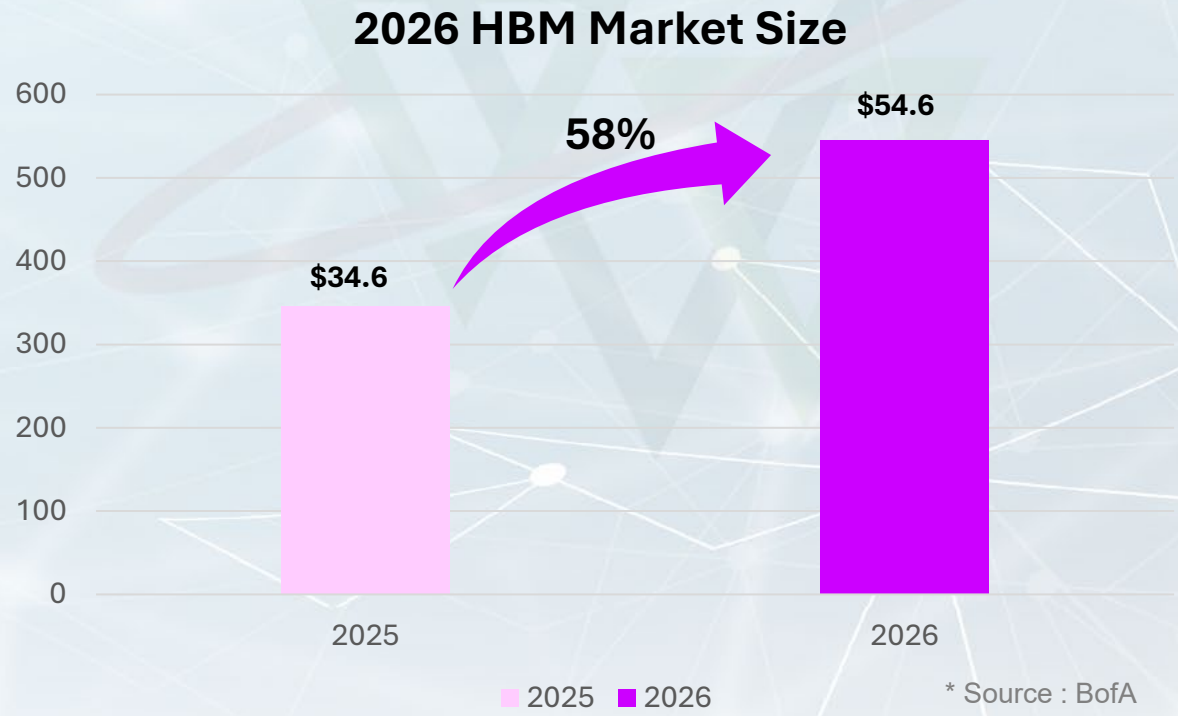
FormFactor™

Seunghoon Yang - SK hynix Inc.

Timothy Blomgren - FormFactor

HBM Market & Probing Tech.

- As AI technology advances, the HBM market size this year is projected to grow by 58% compared to last year, and this scale is expected to expand annually.
- Due to this increasing demand for HBM, Wafer Probing technology in the HBM Test sector also requires advanced development.
- However, HBM Probing faces significant challenges.



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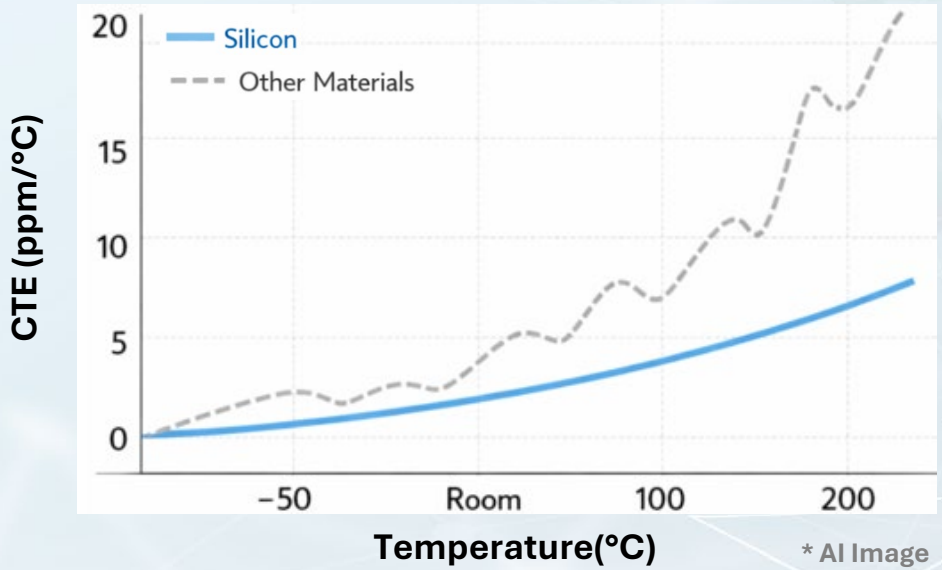
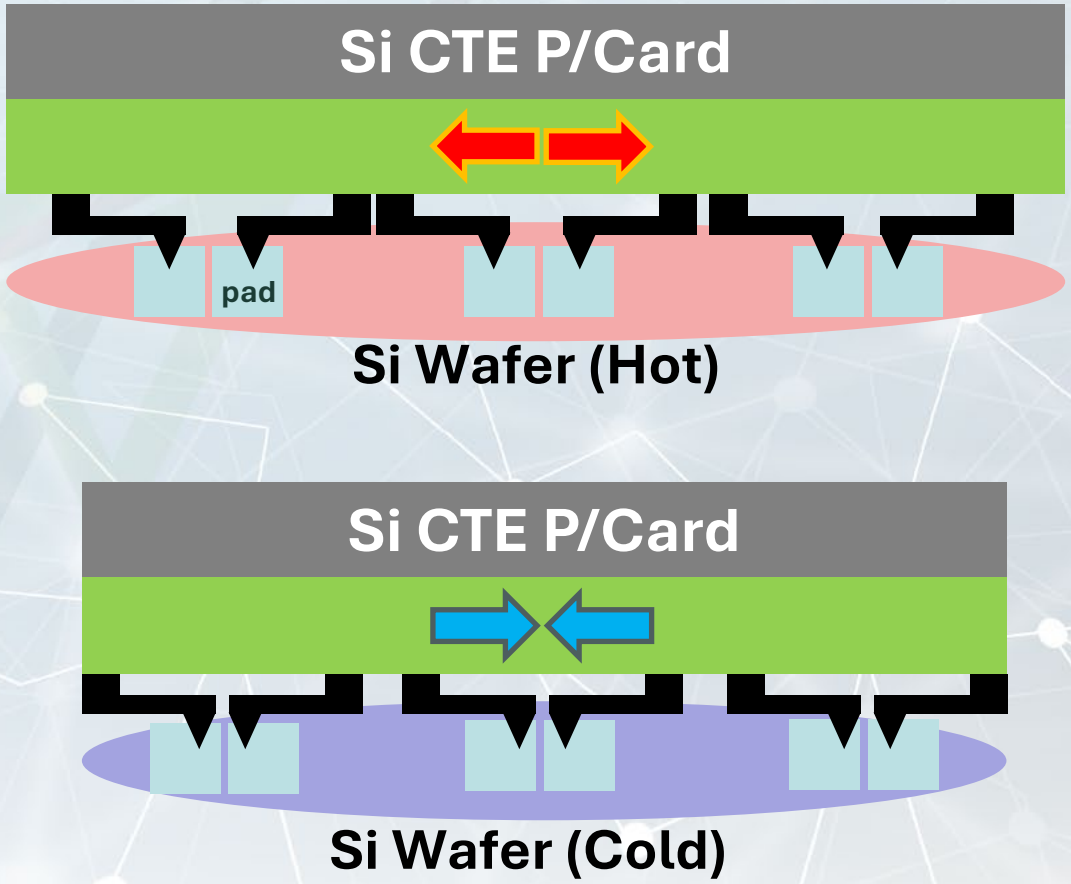
Probing Alignment to Si Wafer

- **Unlike other materials, standard silicon has predictable Coefficient of Thermal Expansion (CTE) behavior which is advantageous for pad alignment with a Multi-Temp Probe Card**



* AI Image



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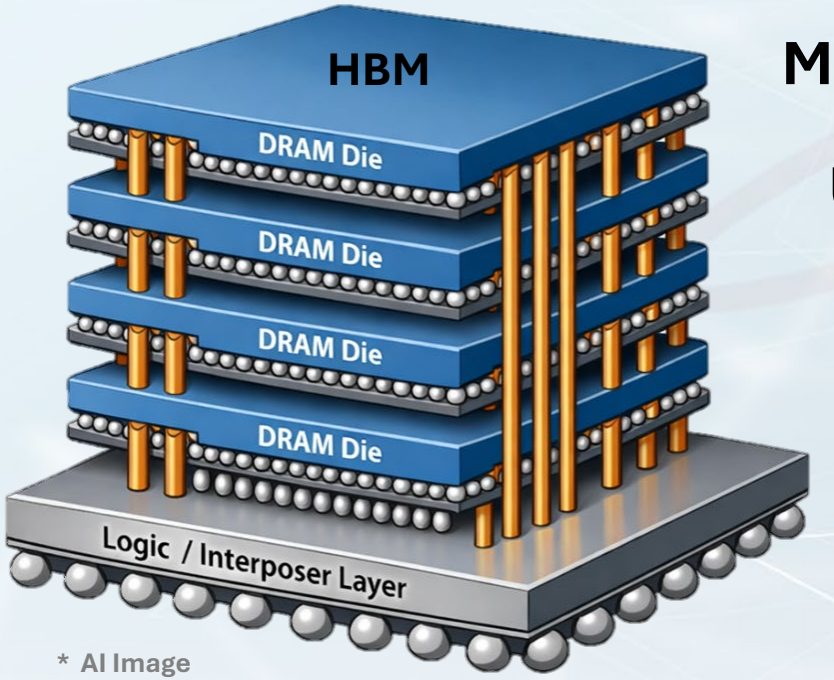
HBM Alignment Challenge

- Unlike standard Si Wafers, HBM wafers feature a unique Logic Die + Core Die stacked structure
- CTE mismatch between stacked DRAM materials affects the net CTE of the HBM wafer
- The CTE change causes alignment issues for typical Si Probe Cards, limiting their usage for Multi-Temp HBM testing



* AI Image

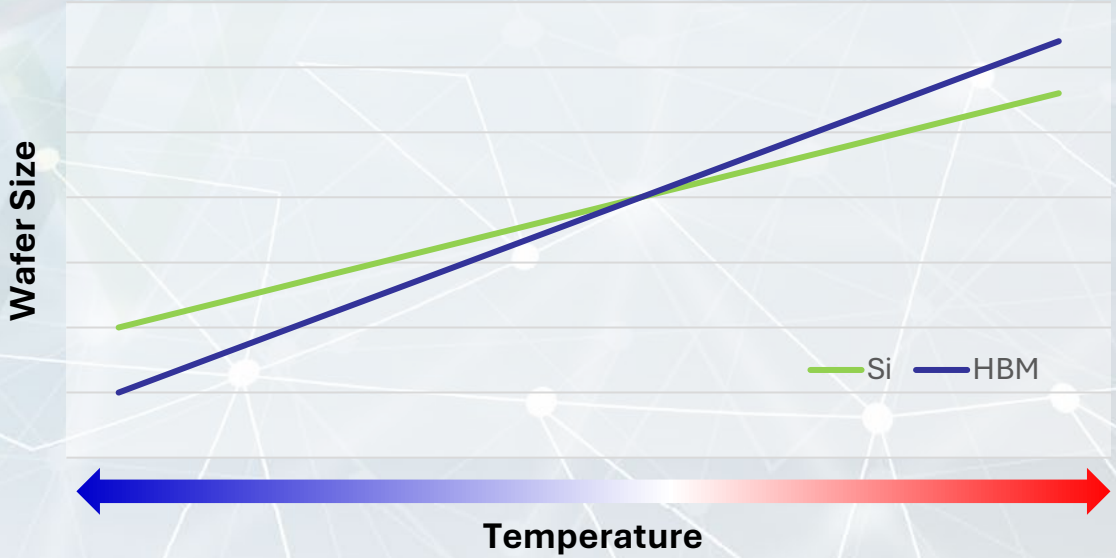
Micro Bump

Underfill

Via

EMC

Size Change Rate: Si vs HBM (Example)



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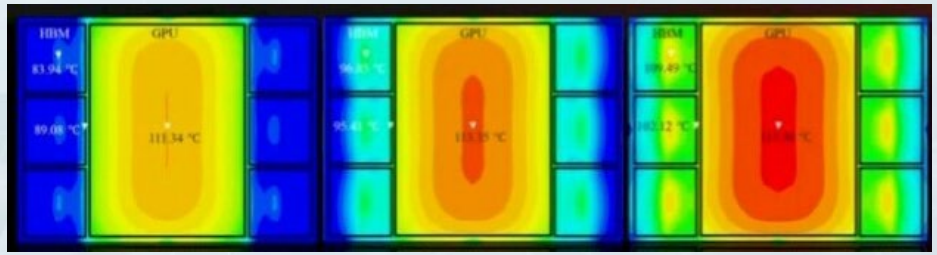
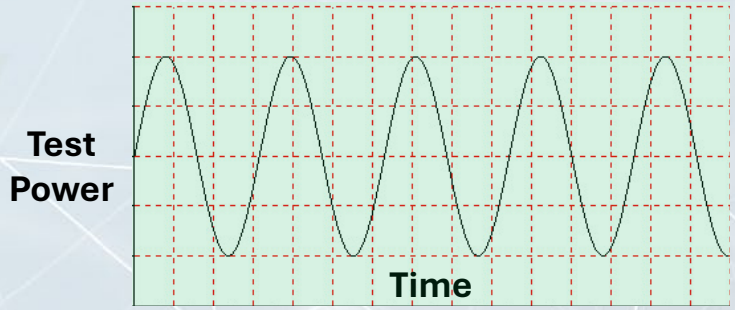
HBM Probing Challenges

- **Joule Heating**
  - High Power/Current results in:
    - Die hot spots
    - Net wafer temperature > Prober chuck temp setpoint

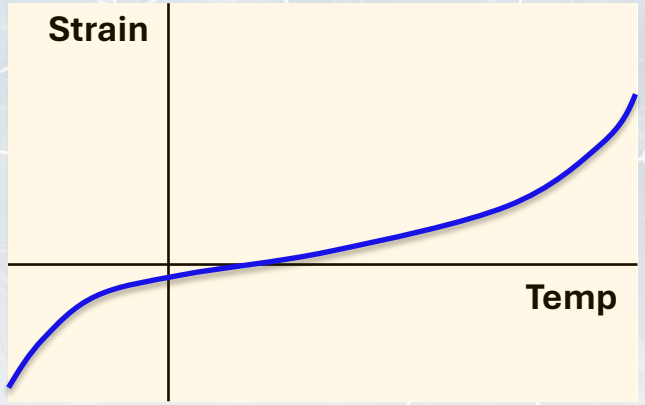


Source: Qualcomm

- **Transient Heating**
  - Pulsed power, transient surges



- **Non-Linear CTE of HBM wafers**



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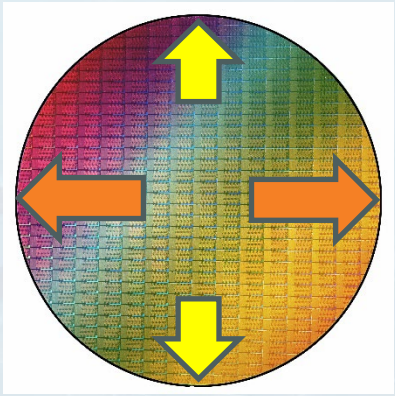
HBM Probing Challenges (continued…)

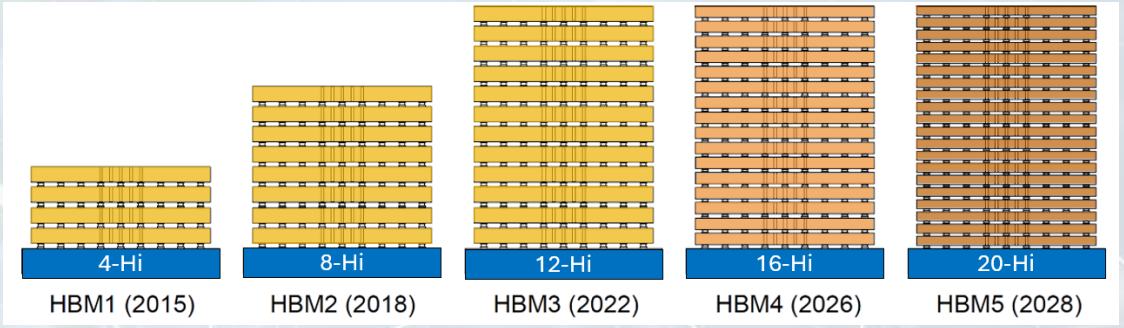
- **Anisotropic wafer CTE**
  - X-direction CTE can differ from Y-direction CTE



Source: *Intel Corp.*

- **Design Variability / Device Dependence**
  - DRAM stack height
  - Wafer filler materials
  - Die size / wafer layout

    ➔ CTE behavior is unique for *every* chip design



Source: *Terabyte Interconnection and Package Laboratory*

- **Pad size shrinkage**

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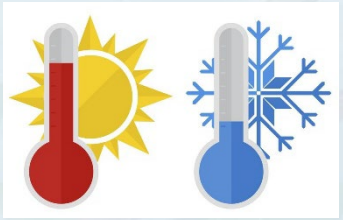
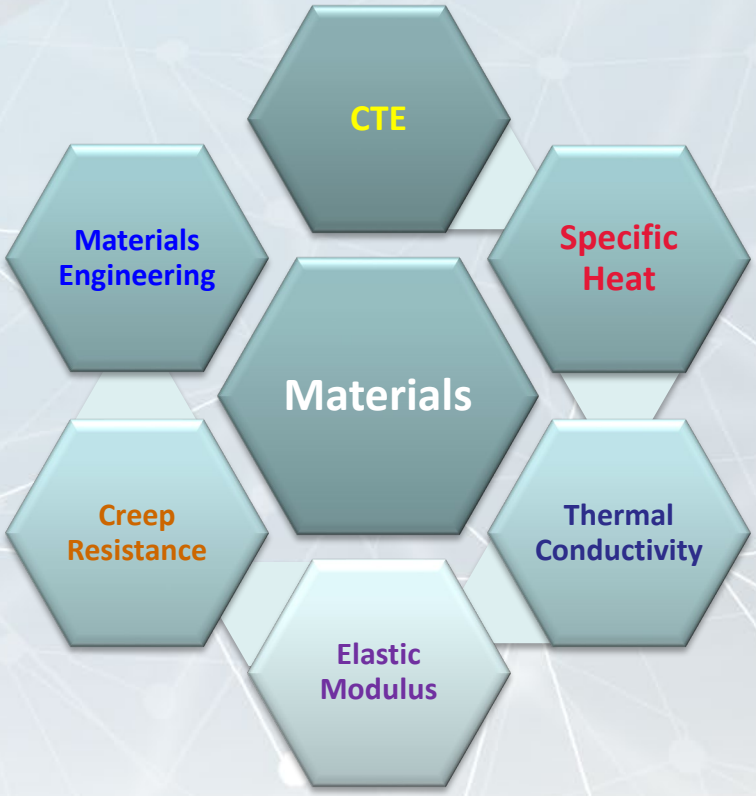
Probe Card Supplier Responses

- **Probe Card Thermal Management (Scaling Control)**
  - **Active Controls**
    - PC Heating -- Historical industry norm
    - PC Cooling -- Likely future requirement



  - **Passive Controls**
    - Thermo-Mechanical Design
    - Material Selection
    - Materials Engineering
      - Customization of key material properties



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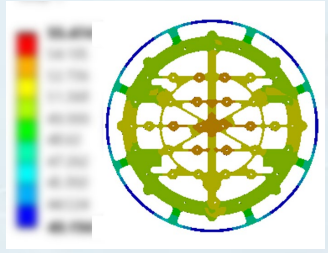
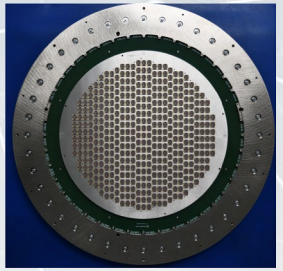
Probe Card Supplier Responses (continued…)

- **Thermal Simulation**
  - Determine optimal Room Temp scaling target as a function of:
    - Probe Card design parameters
    - Production test parameters
    - Measured wafer CTE data

Wafer CTE data

Design | **Thermal FEA** | **Thermal Simulation Model** | **Fabrication**





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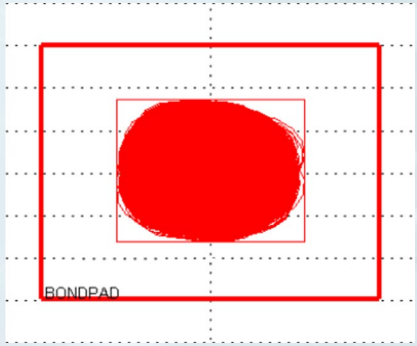
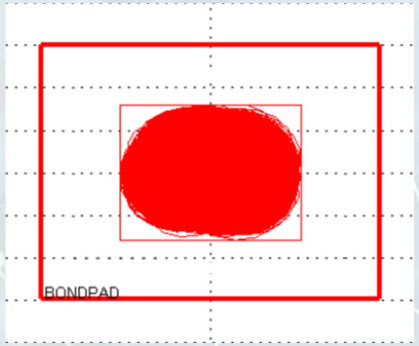
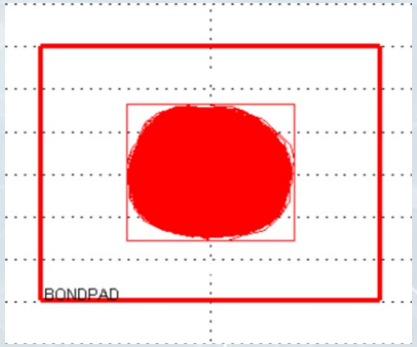
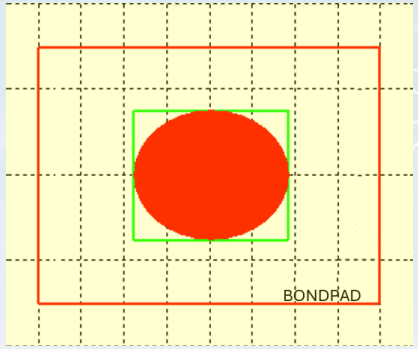
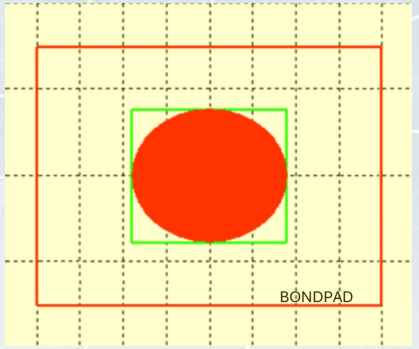
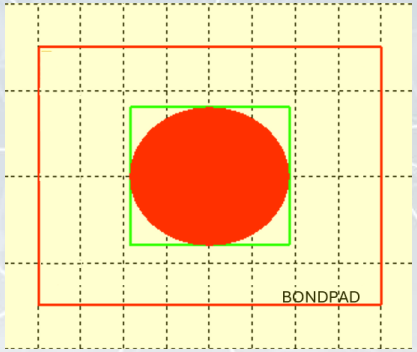
HBM Alignment Evaluation Results

- Good SuperBondPad (SBP) performance was achieved at multiple production test temperatures
- The thermal simulation model generated SBP predictions that correlated well with empirical data, though slightly underestimated, primarily in the scrub direction (🡐🡒)

	Cold Temp	Hot Temp A	Hot Temp B
Empirical Results: *(~62k probes)*			
Simulation Results:			

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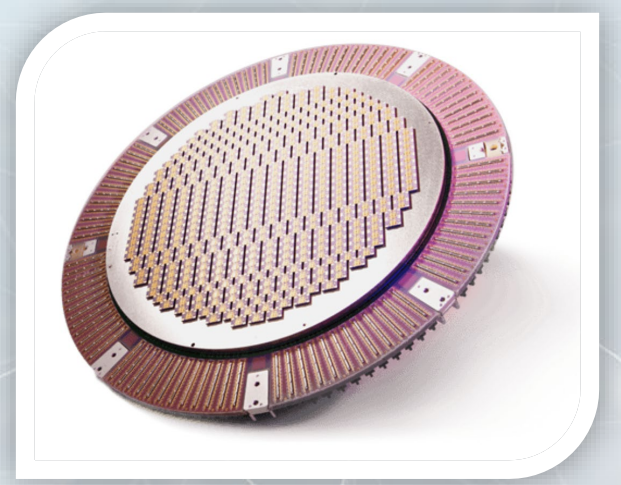
Conclusions

- **Key factors that enabled successful multi-temperature HBM probing**
  - **Collaborative partnership between SK hynix and FormFactor**
    - Joint wafer CTE characterization
  - **SmartMatrix Architecture**
    - Thermal stability; Resilience to thermal transients
  - **Thermal Simulation**
    - Development and fine-tuning of FTSM (FormFactor Thermal Simulation Model)
  - **Advances in Materials Engineering**
    - Material property customization / optimization



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Acknowledgements

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  - HBM Wafer CTE characterization
  - Evaluation Support
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  - HBM Wafer CTE characterization
- **Kalyanjit Ghosh, FormFactor**
  - Thermo-mechanical design and Materials Engineering
  - FTSM (FormFactor Thermal Simulation Model) development

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