# ENABLING DIE LEVEL KGD TESTING FOR CPO OPTICAL ENGINE

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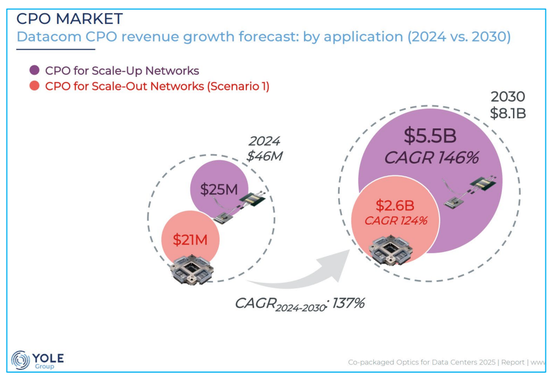
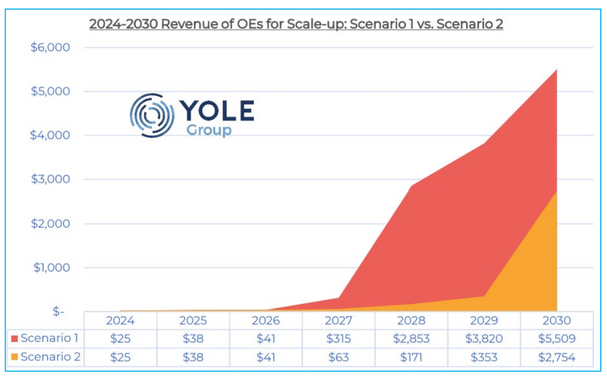
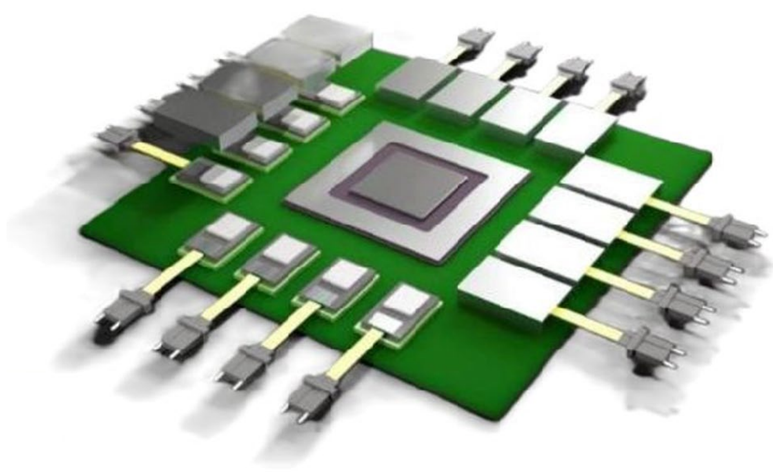
## Co-Packaged Optics (CPO) Market Size and Optical Engine Known Good Die

- CPO Market Size
  - CAGR : 137% from 2024 to 2030
  - OE revenue projected to reach $5.5B (optimistic) or $2.75B (conservative) by 2030
- Optical Engine (OE) Known Good Die (KGD)
  - Yield Assurance: Perform KGD testing on every OE to ensure only verified dies are integrated with GPUs/ASICs.
  - Cost Mitigation: Prevent expensive assembly losses by filtering defective components before they enter non-reworkable CPO systems.



Source: Yole 2025 CPO Report

## Co-Packaged Optics (CPO) Typical Test Insertions

Advanced Packaging (AP) Process (COUPE/ FOWLP)

Singulation Process & Receptacle Attach

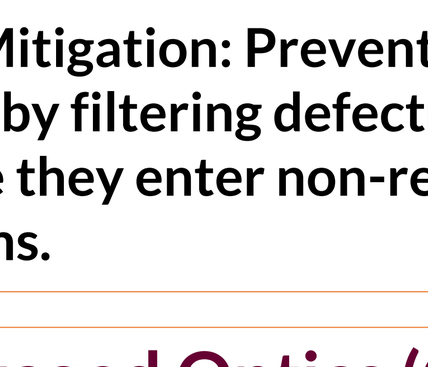
Process Control Monitor

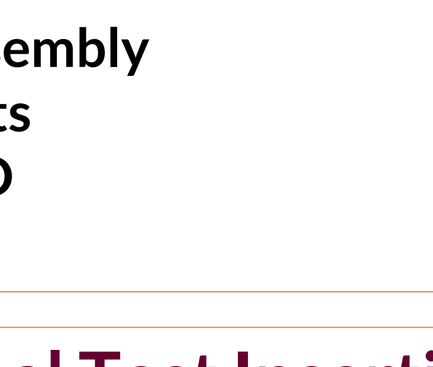
Insertion 1 (PIC Wafer Sort)

Insertion 2 (OE Wafer Sort)

Insertion 3 (OE Die Level Test)

Insertion 4 (CPO Module Test)









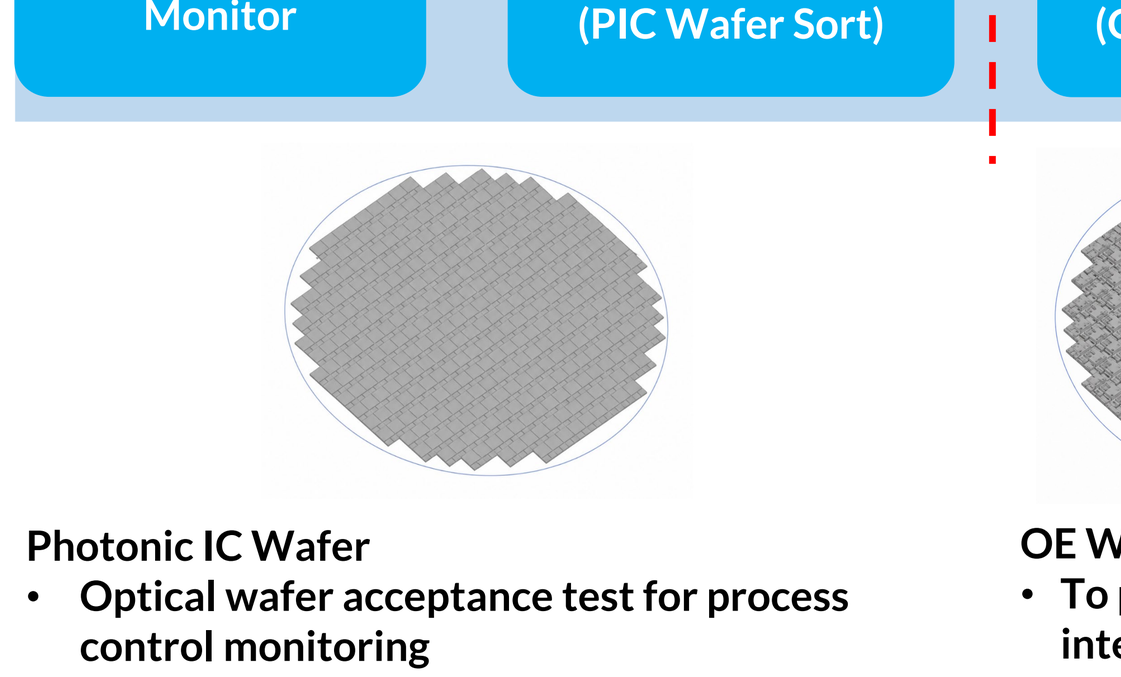
Source: FiberMall website

**Photonic IC Wafer**
- Optical wafer acceptance test for process control monitoring
- Wafer sort to produce PIC KGD

**OE Wafer Sort**
- To perform DC and interconnectivity tests for AP process qualification

**OE Die Level Test (DLT)**
- To perform OE at-speed functional test
- To produce OE KGD

## Wafer Level Test vs. Die Level Test for Optical Engine KGD




Source: TSMC COUPE

| Parameters | Wafer Level Test (WLT) | Die Level Test (DLT) |
|---|---|---|
| Test Coverage | DC test | At-speed test |
| Parallelism | 1 – 2 sites (limited by active coupling) | 4 sites |
| Temperature (self-heating effect; ~80W/die) | Affected by high power load and causing warpage | RT - 85°C with active temperature control (ATC) |

# OPB8201 + SP9000e Optical Engine Die Levet Test KGD Solution

OPB8201 DLT KGD


SP9000e OE Tester




Singulated OE Die
With Receptacle

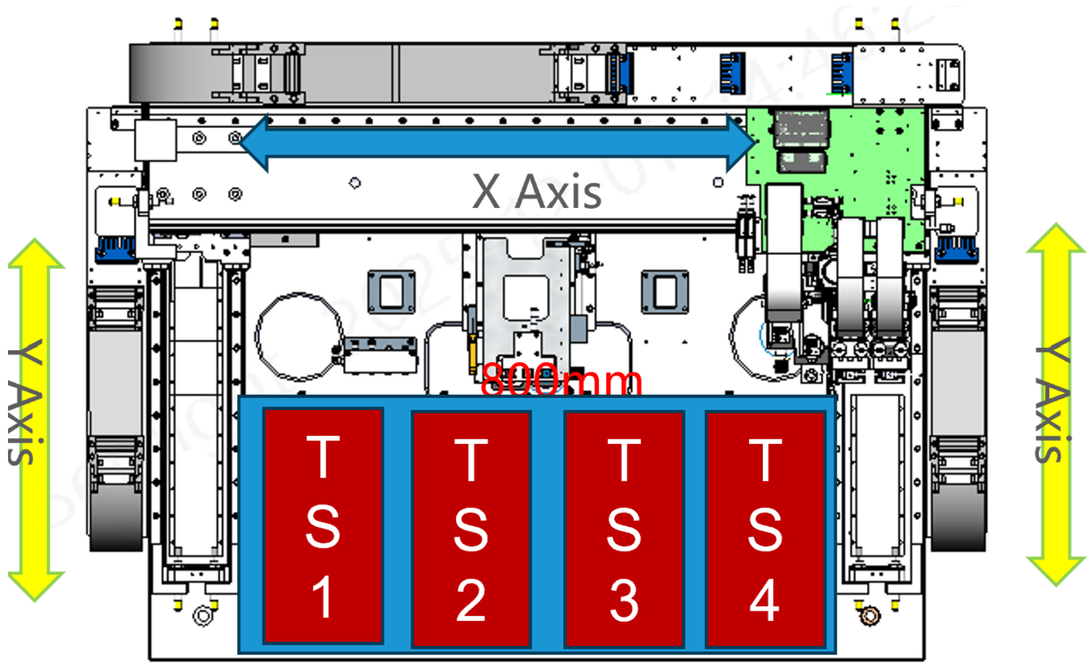
## OPB8201 OE DLT KGD Handler

- Enable die-level test for singulated OE die assembled with receptacle
- Support optical connector and detachable FAU
- ≤±10μm system alignment accuracy
- Air damper socket based with dual contact force design
- 4sites parallel test with UPH: ~570

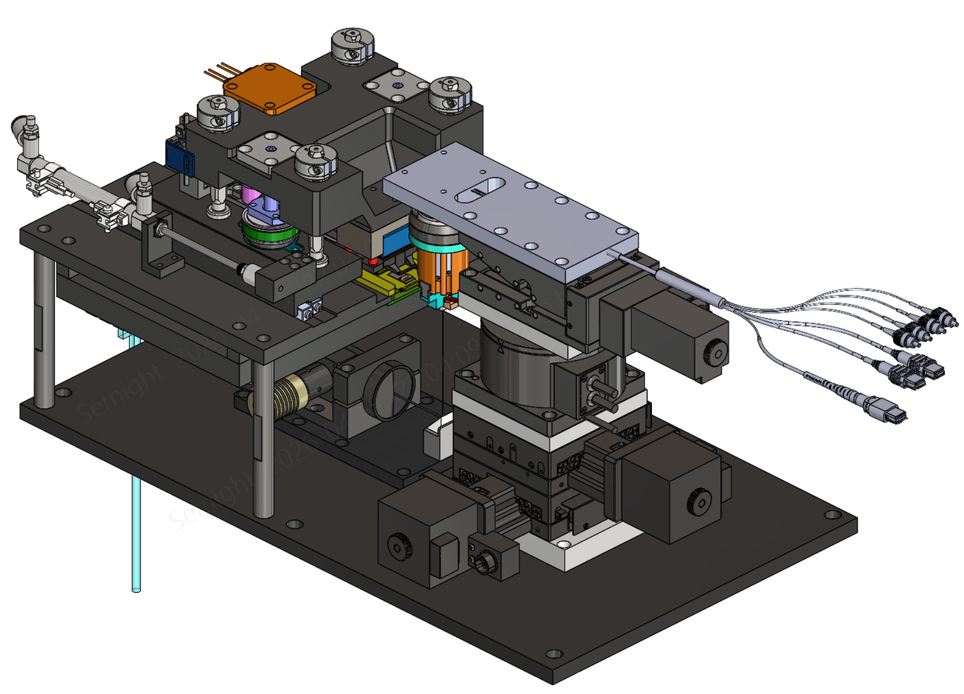
## SP9000e OE Tester

- Tester-on-DUT-Board system architecture design for electrical test resources
- Cabinet populated with 65GHz BW optical instruments
- 224Gbps BERT board for high-speed electrical testing
- High density test resources support multisite (1 system to cover 4 test sites)

# Technical DoE Data: UPH and Thermal Control Data




OPB8201 Test Station (with 4 Test Sites)



OPB8201 Test Site Structure

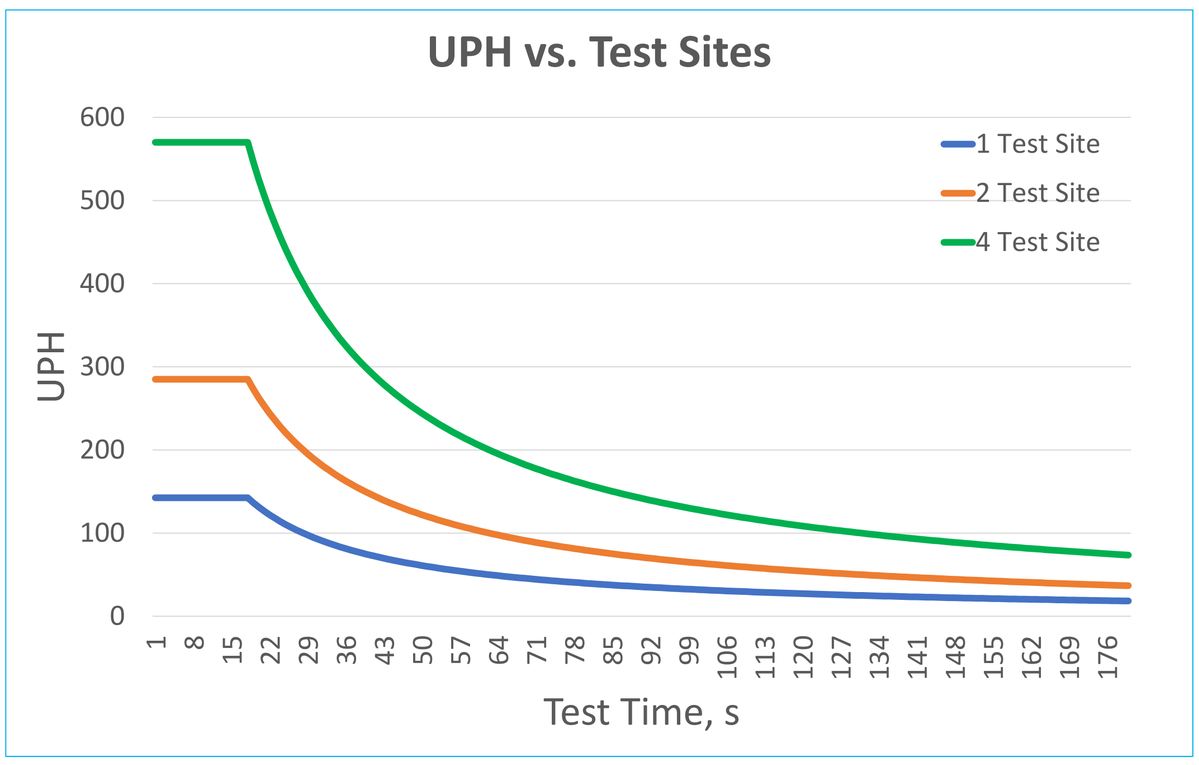



**Figure 1: OPB8201 4 test sites UPH graph.**

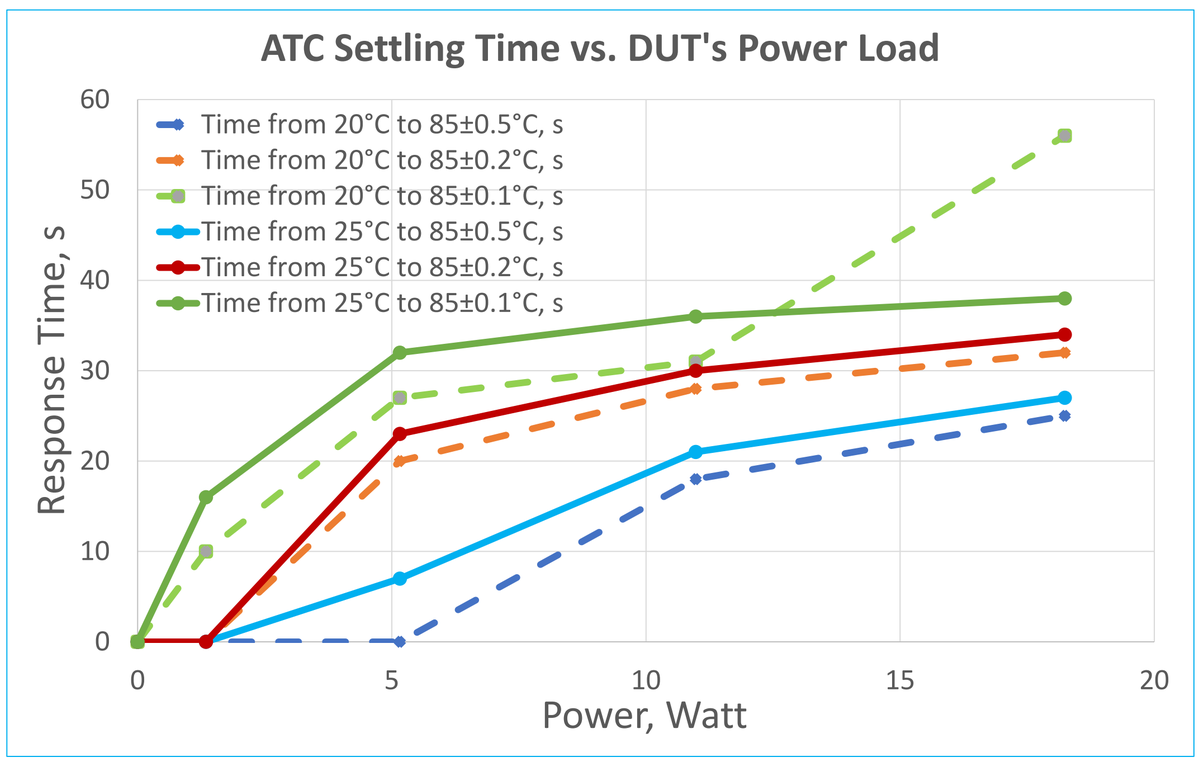
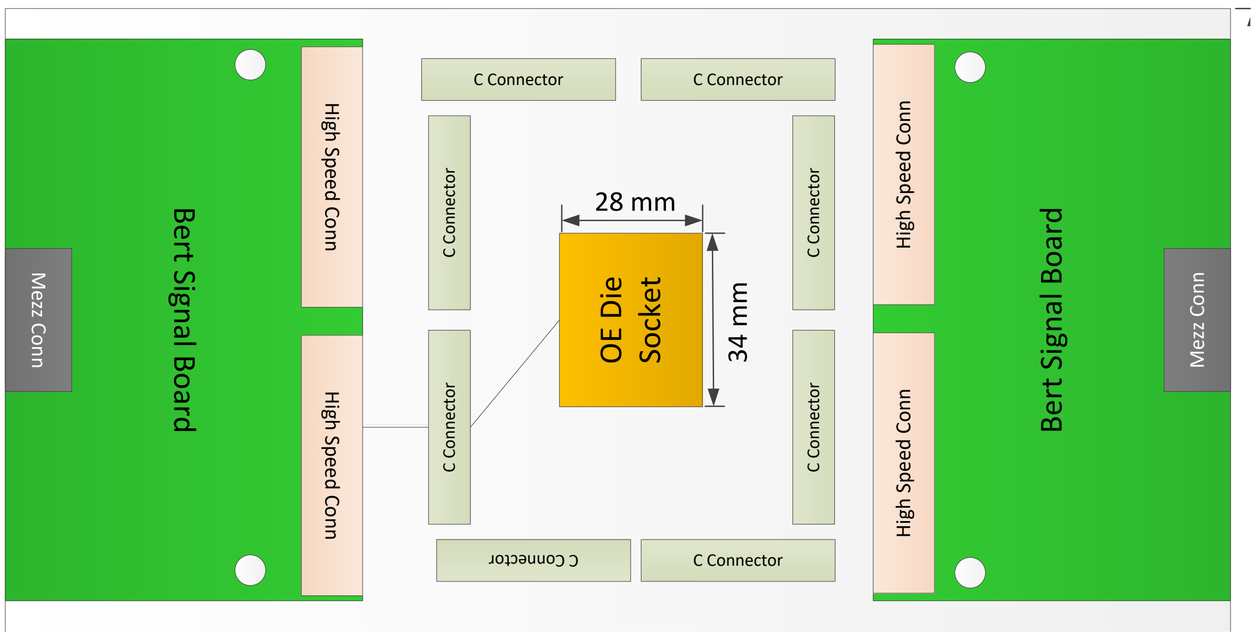



**Figure 2:** ATC temperature settling time at various power loads

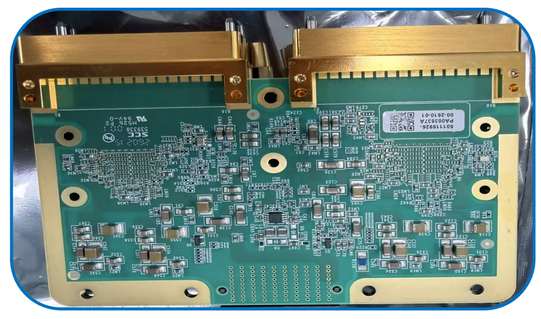
- **High Parallelism and Accuracy of Temperature Control**
  - **OPB8201 features 4-site parallel testing to maximize throughput and support HVM environments.**
  - **ATC system precisely regulates the target test temperature while compensating for DUT power dissipation during at-speed operation.**

# Signal Integrity Measurement Data

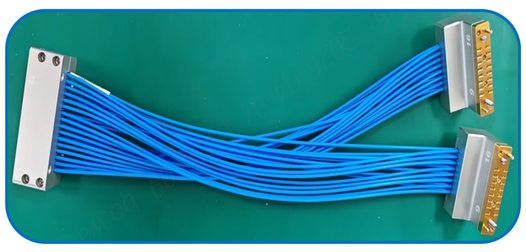



**SP9000e DUT Board Layout**

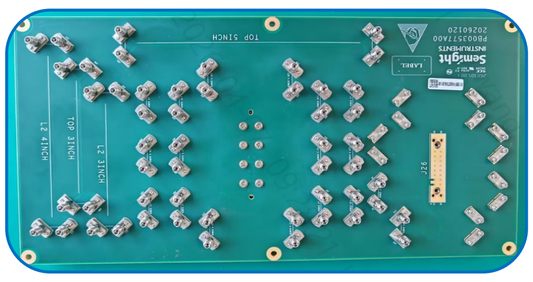
**224Gbps BERT Board (≤1.5”)**



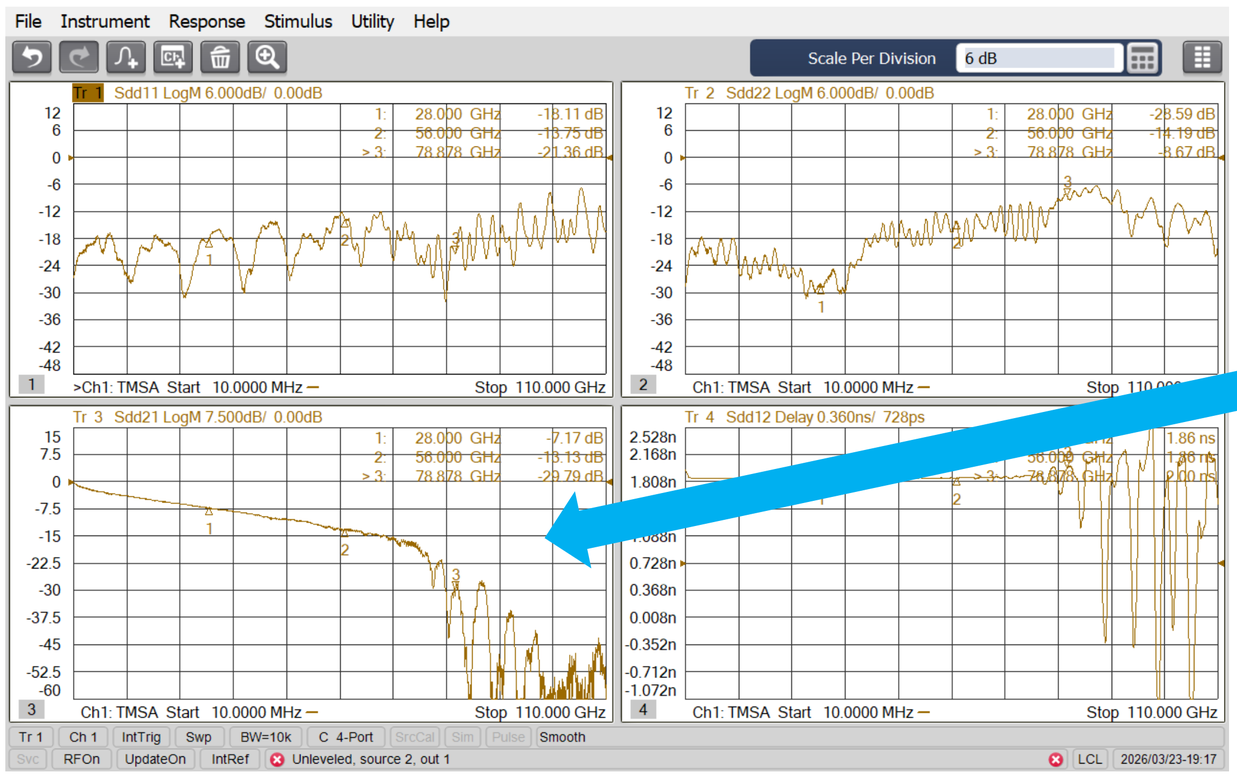
**110GHz Flyover Cables (250mm)**

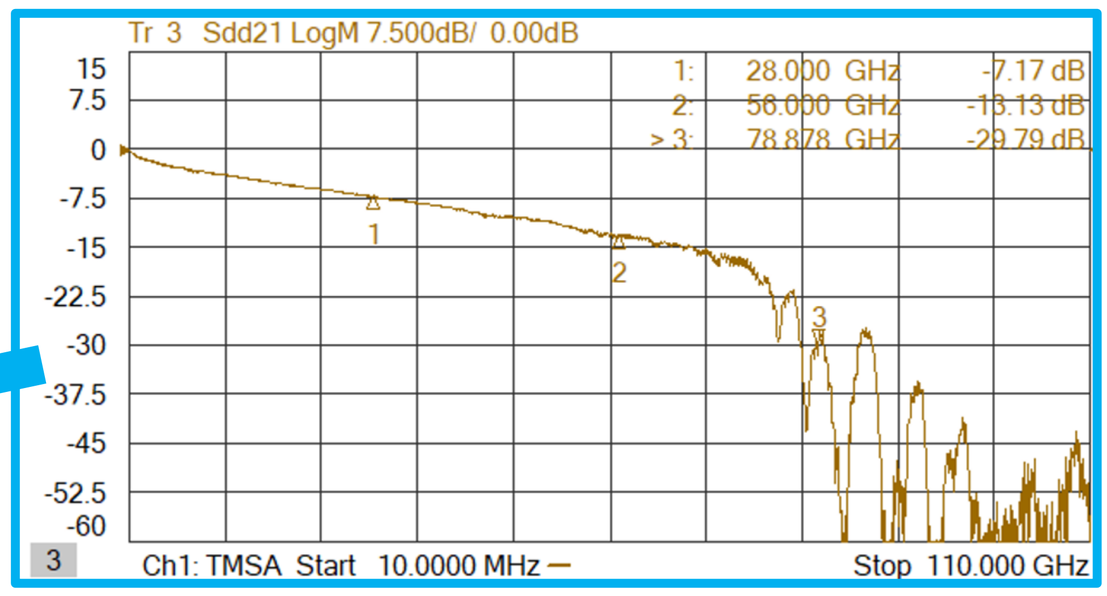


**Breakout Test Fixture (≤2”)**



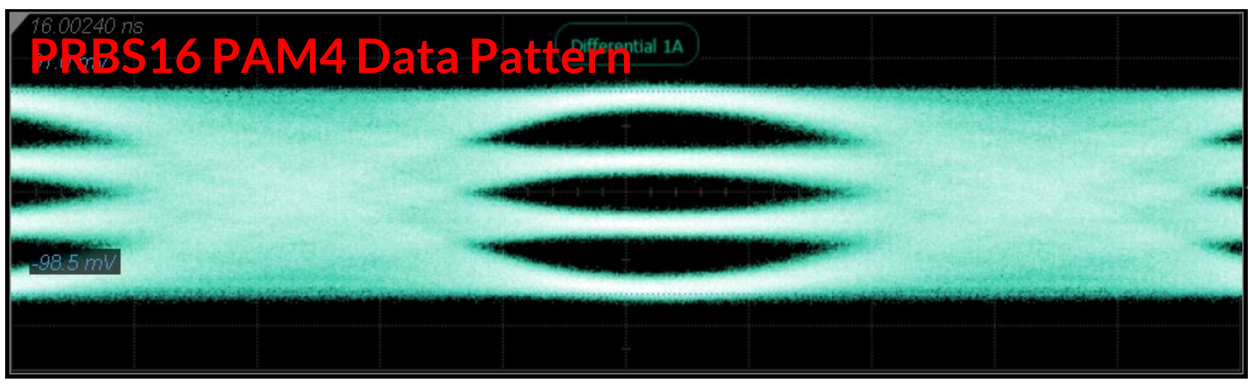
## Experimental Measurement Setup

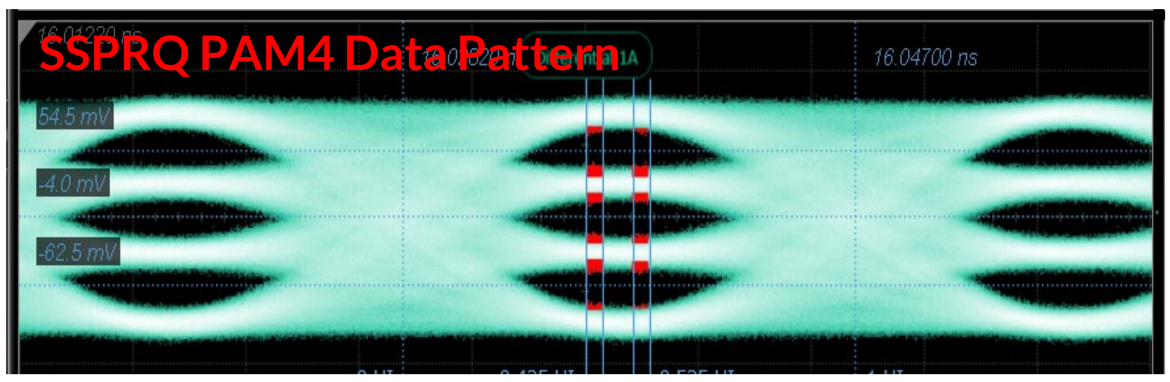



**IL : -7.17 dB @ 28GHz for 112Gbps PAM4**

**Figure 3: S-parameter measure results from 10MHz to 110GHz for the SP9000e BERT board to the breakout test fixture.**




| Parameters | 112Gbps PRBS16 Data Pattern | 112Gbps SSPRQ Data Pattern |
|---|---|---|
| Level 0/1 EW/EH | 6.195ps / 23.90mV | 6.530ps / 24.55mV |
| Level 1/2 EW/EH | 7.955ps / 25.85mV | 7.915ps / 24.55mV |
| Level 2/3 EW/EH | 5.985ps / 24.56mV | 6.655ps / 23.25mV |
| Amplitude (Pk-Pk) | 189.30mV | 190.60mV |
| Outer OMA | 168.55mV | 170.60mV |
| TDECQ, dB | 0.84dB | 0.44dB |

**Figure 4: Eye diagram and TDECQ measurement for 112Gbps PAM4 signal from the SP9000e BERT board to the test fixture.**

## Conclusion

- **OE die level test enables functional at-speed and multi temperature KGD test.**
- **The OPB8201 + SP9000e system is an OE die-level KGD test solution for HVM, featuring 4-site parallel testing with support up to 112Gbps.**

## Ongoing Work

- **Ongoing development to enable 224Gbps data rates using PCB routing and high-bandwidth connector integration.**