SWTEST 2026 CONFERENCE

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Next generation Thermal Chuck for Improved Temperature Control of Singulated Die Testing

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Introduction: Singulated Die Sort/Test - SDx

- At Intel Foundry, we have developed the SDx platform for singulated die testing
  - Testing at singulated die level is essential for chiplet-based design of complex packages where a single bad die can lead to a scrap of the entire multi-chip package
  - Active Thermal Control (ATC) is the highlight of the SDx capability. SDx utilizes ATC to maintain the target die temperature by removing excessive heat through the **thermal chuck**
  - SDx enables full final test content of individual dies, multi-chip packages, and stress test at sort
    - High Thermal stress to catch latent defects
    - High Electrical stress (high voltage, frequency) to screen defective die

SDx platform

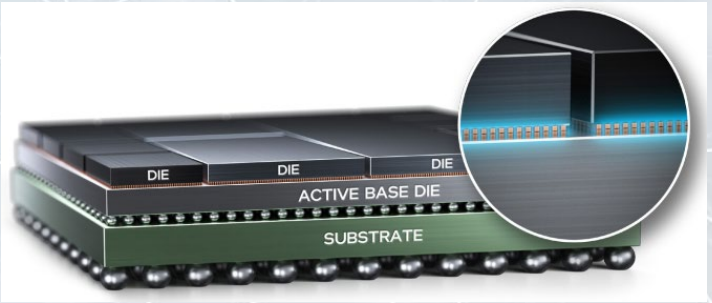
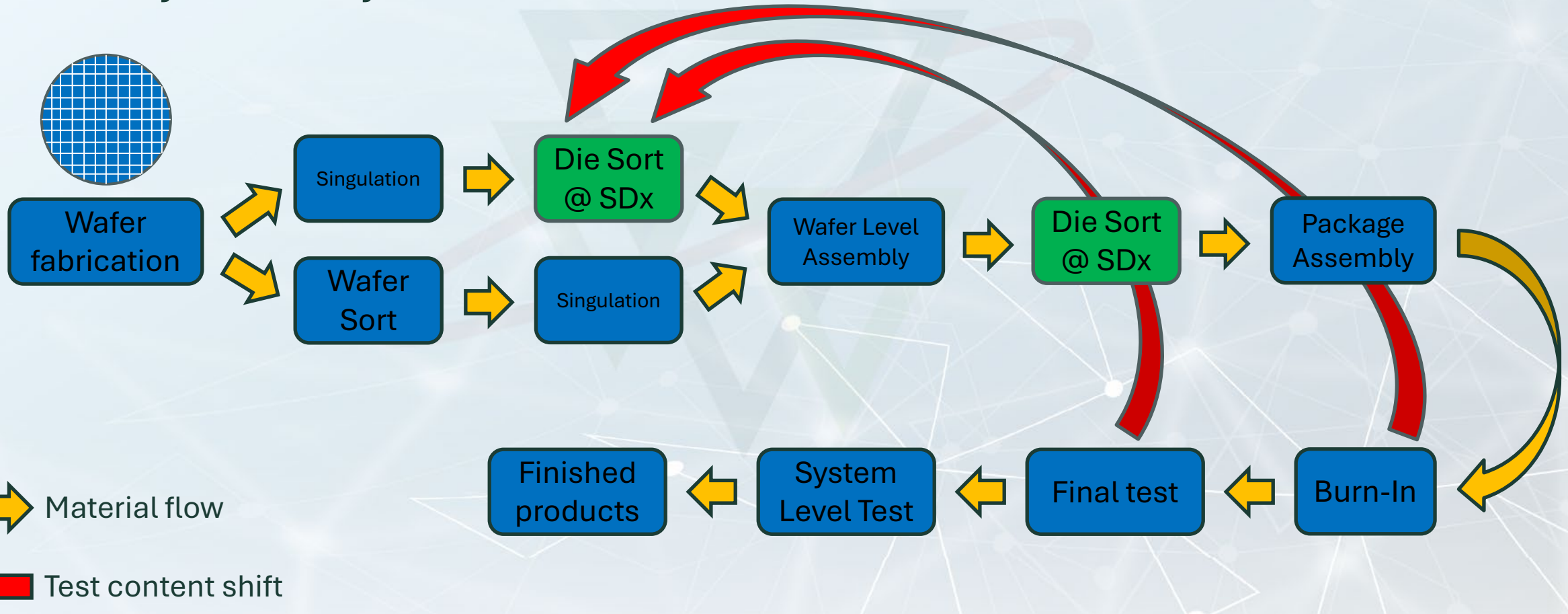


Illustration of a stacked die on a substrate

A place for Die Sort in the test flow

- Enabling the Known Good Die concept
- Necessity of ATC system at die sort



Encountered challenges and limitations

- First generation of thermal chuck provides excellent performance in maintaining die target temperature in the -40C to 125C range.
- In addition to wafer sort testing content, additional content was enabled that was historically evaluated at Burn-In and Class test modules.
  - Test content with high input magnitudes can generate sufficient heat to exceed the conductivity at the die to chuck interface (R_{jh}) and chuck to coolant interface (R_{hf}).
  - Excess heat led to the die increasing in temperature, thermal runaway condition, test failure, and potential hardware damage.

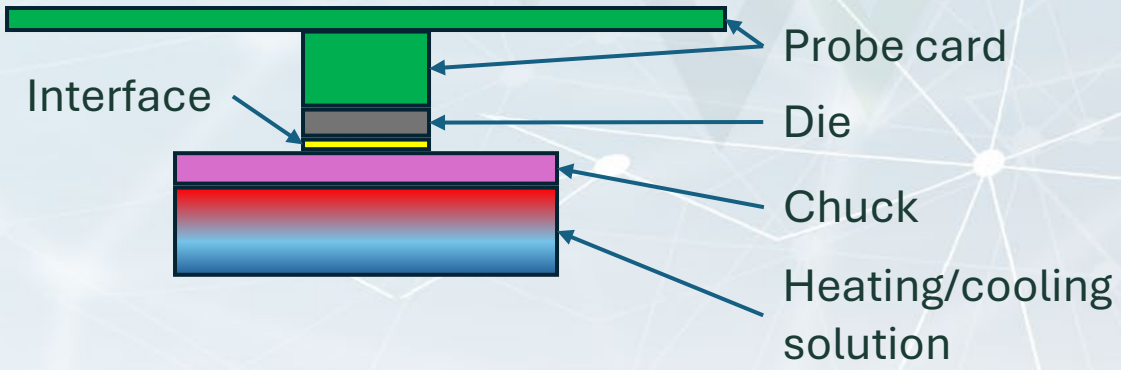
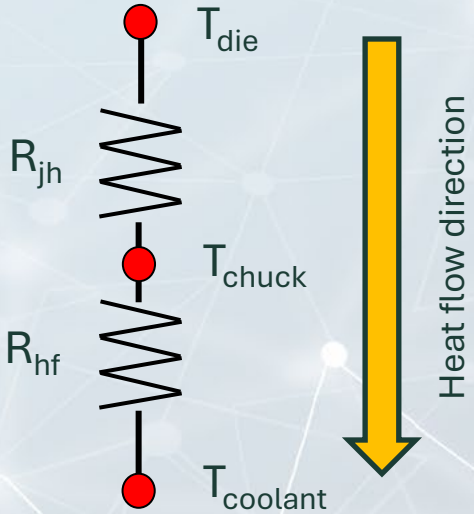


Illustration of SDx test stack

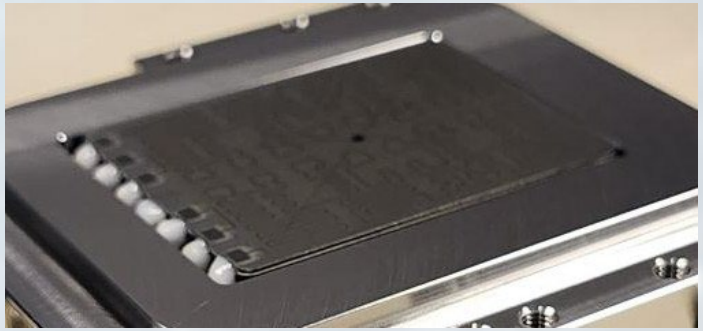


Schematic of heat flow path

Intel/Technoprobe solution

- To address the limitation of the heat transfer, we have partnered with **Technoprobe** in development and fabrication of the next generation of thermal chuck
  - Next generation chuck brings the improvement in heat spreader and heating/cooling capabilities
  - Under static conditions, measured heat flux exceeded >250 W/cm2
  - Thermal chuck temperature ramp up and down capability was measured >200 °C/s

SDx thermal solution	1st gen	→	Next gen
Chuck	Ceramic	→	CVD diamond
Heating	Embedded heater trace	→	Optimized trace shape for improved heating uniformity
Cooling	Coolant channels	→	Redesigned microchannels for enhanced heat exchange



Next Generation thermal chuck

Case study summary

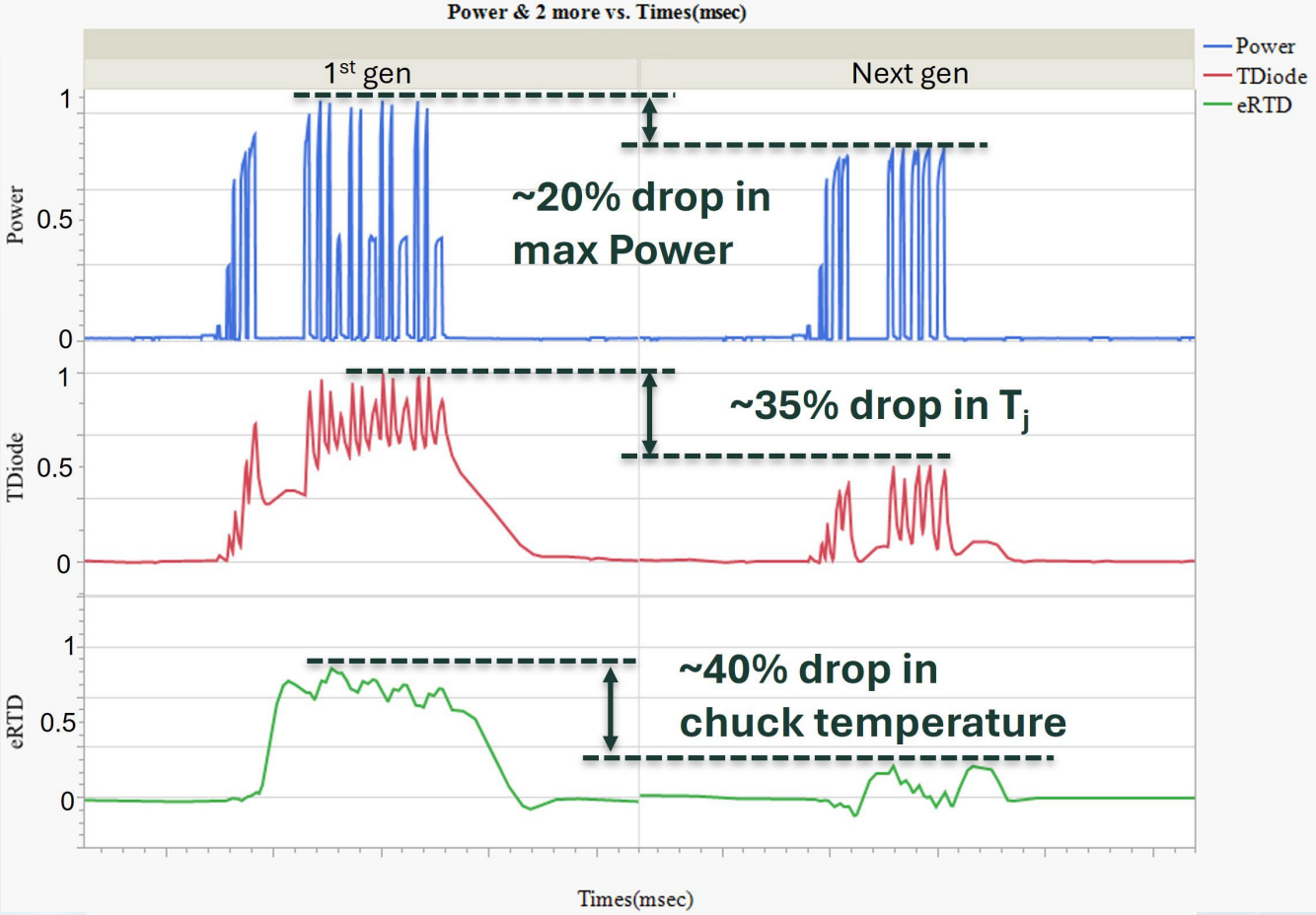
- Performance of the next generation chuck was evaluated against 1st generation under most challenging conditions using small and large dies

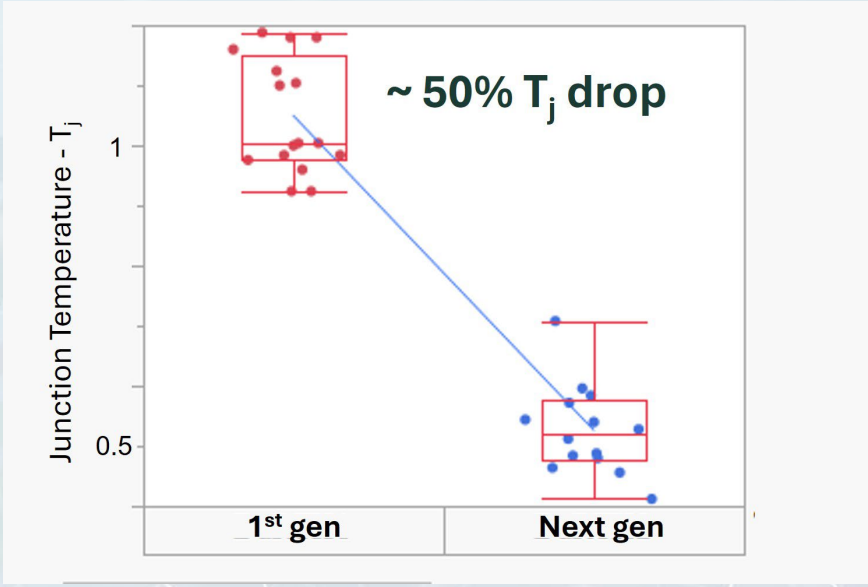
Evaluation	Die size	Power level	Test duration
Case study 1	Small	**High power**	Short repetitive bursts
Case study 2	Small	**High power**	Single extended event and a series of moderate bursts
Case study 3	Large	**Mixed power levels**	Mixed duration of the test content

- eRTD – embedded Resistive Thermal Detector located in the chuck
- TDiode/TD – Thermal sensor located in the die
- Power – normalized measured power delivered to the die
- Heater/Coolant – magnitude as a percentage of maximum

Case study 1

- Thermal log comparison between 1st gen and Next gen thermal chuck during short bursts of high power



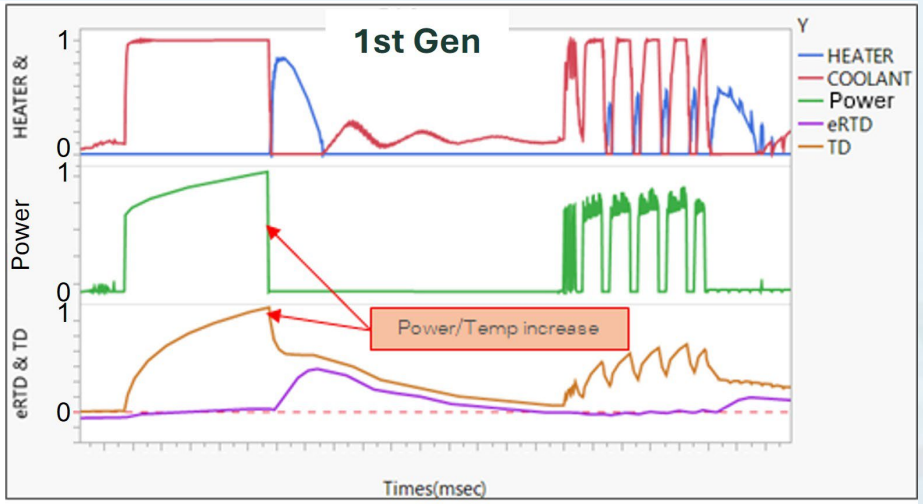


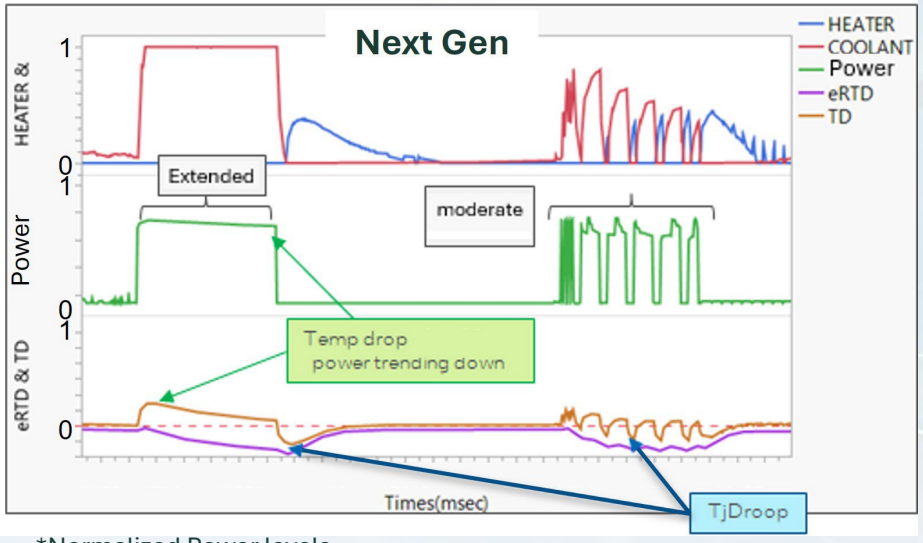
- With optimized test content flow, T_j was reduced by ~56% on 1st generation thermal chuck
- T_j of the same content dropped additional 50% when Next generation chuck was evaluated

- Next generation thermal chuck prevented thermal runaway conditions that caused the test failures at defined conditions

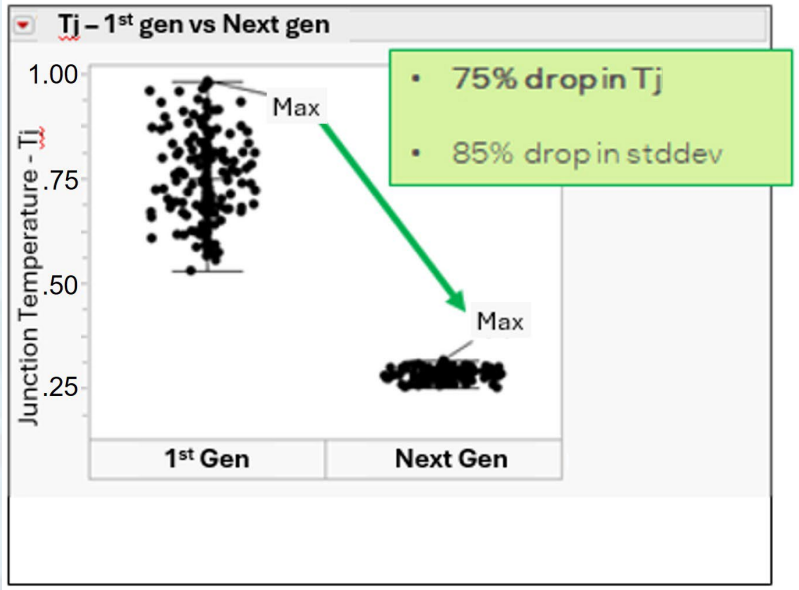
Case study 2

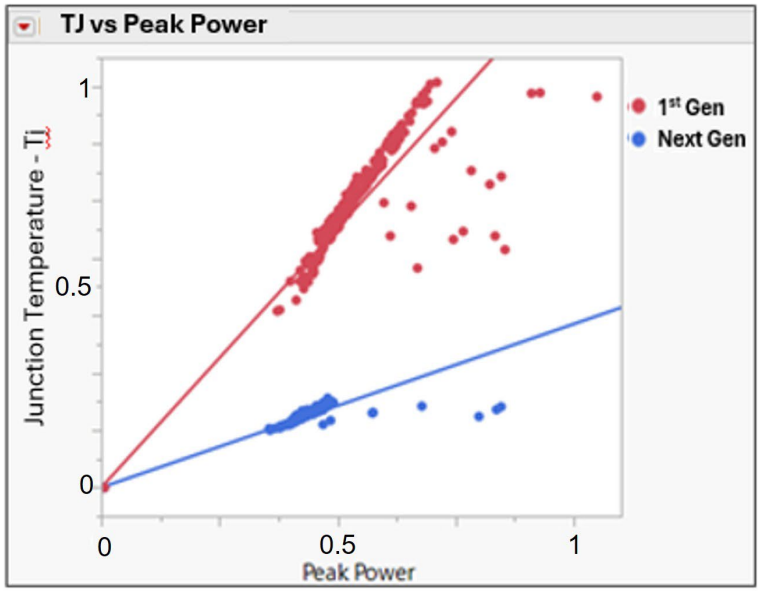
- Thermal log comparison, 1st gen vs Next gen thermal chuck, under extended and moderate bursts of high power





*Normalized Power levels

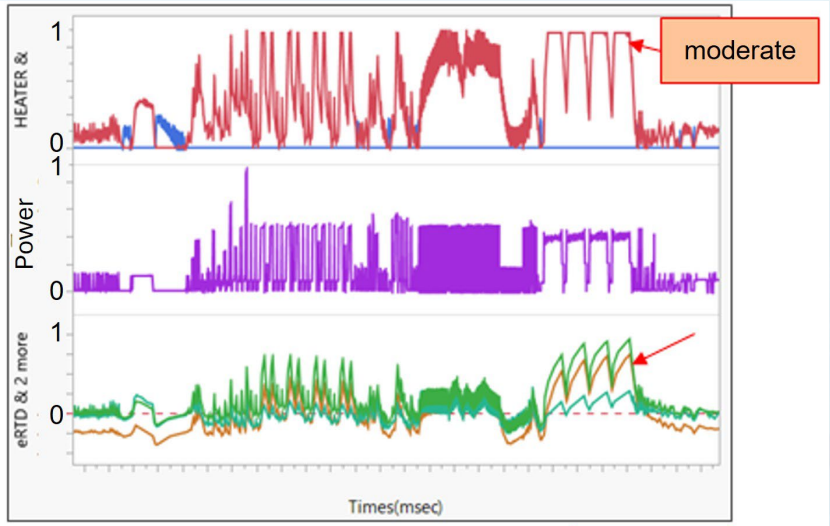


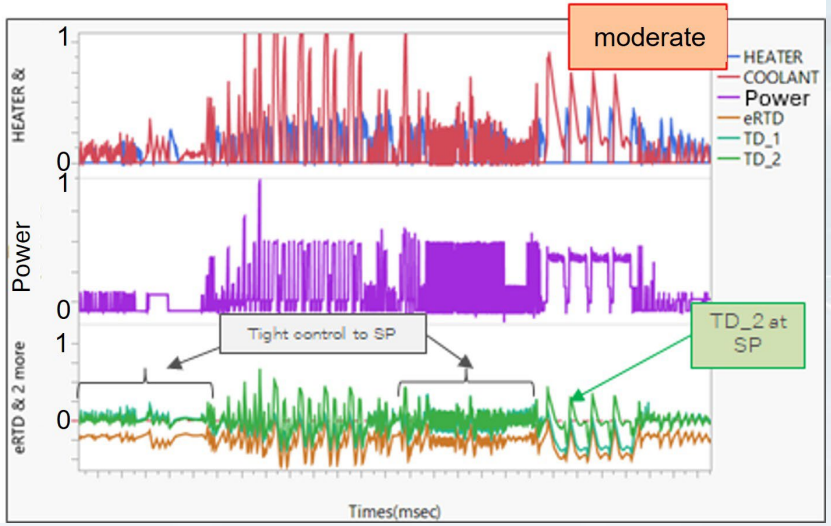


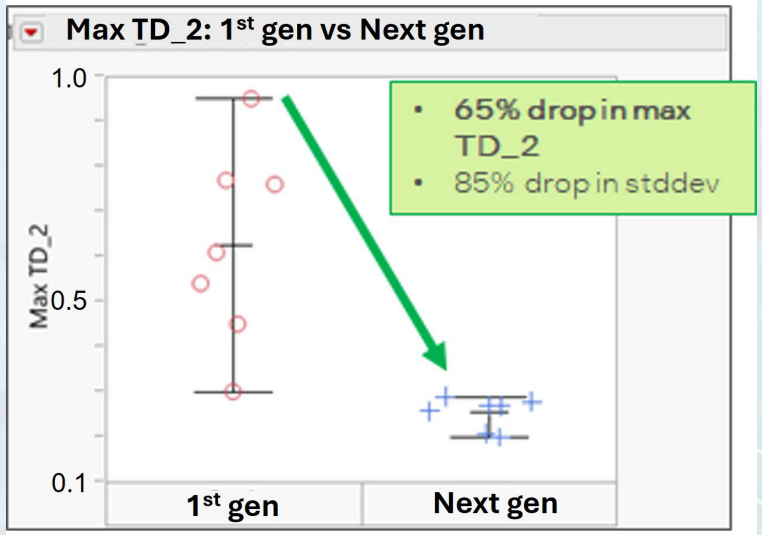
- **Next generation thermal chuck reduces the magnitude and variation of die temperature during the test, under the same input conditions:**
  - Reduced peak and average junction temperature by 75%
- **Thermal runaway events are mitigated through optimized heat extraction**

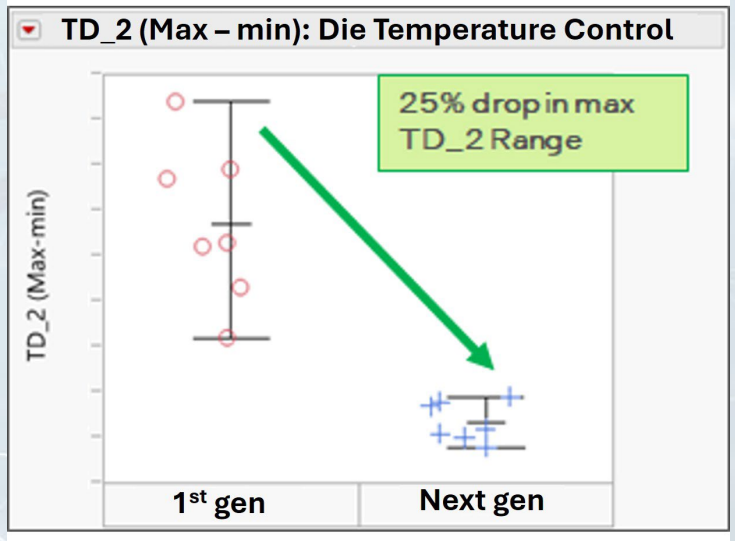
Case study 3

- Thermal log comparison, 1st gen vs Next gen thermal chuck, under a variety of test conditions in both magnitude and duration









- **For the identical test content, next generation chuck:**
  - Reduced peak temperature by 65%
- **Thermal runaway conditions are precluded when next generation thermal chuck is used**

*Normalized power levels

Summary / Conclusion

- A collaborative effort between **Intel** and **Technoprobe** brought up the next generation of thermal chuck to SDx platform and pushed out the observed thermal constraints reached with test content that is commonly executed at the post-package testing;
- Limitations in heat exchange at the die/chuck interface, and chuck/coolant interface were mitigated out by the introduction of innovative materials, manufacturing techniques and optimization of the design;
- In the present and future of disaggregated semiconductor products, early detection of defects at SDx further drives the concept of a Known Good Die moving into assembly and package flows and reduces losses at post-assembly and post-packaging testing.

Thank you!

Acknowledgement

We express our gratitude to all the teams from Intel Foundry USA and Technoprobe ITALY for their valuable contribution in bringing the next generation of SDx thermal chuck from concept to high volume manufacturing reality.

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