SWTEST 2026 CONFERENCE

35th ANNIVERSARY

Recommendation on Increasing Test Productivity

Three new effective ways for AI Chip testing

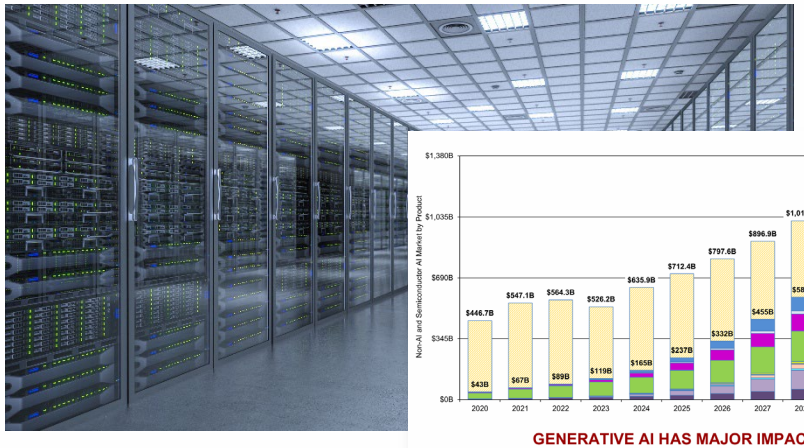
Shoun Yu

SEMICS

Dilemma in AI Era

More chips to test → More space and higher cost

Exploding AI chip test demand



Stricter quality expectations → Longer test time

Ultra-high reliability requirements

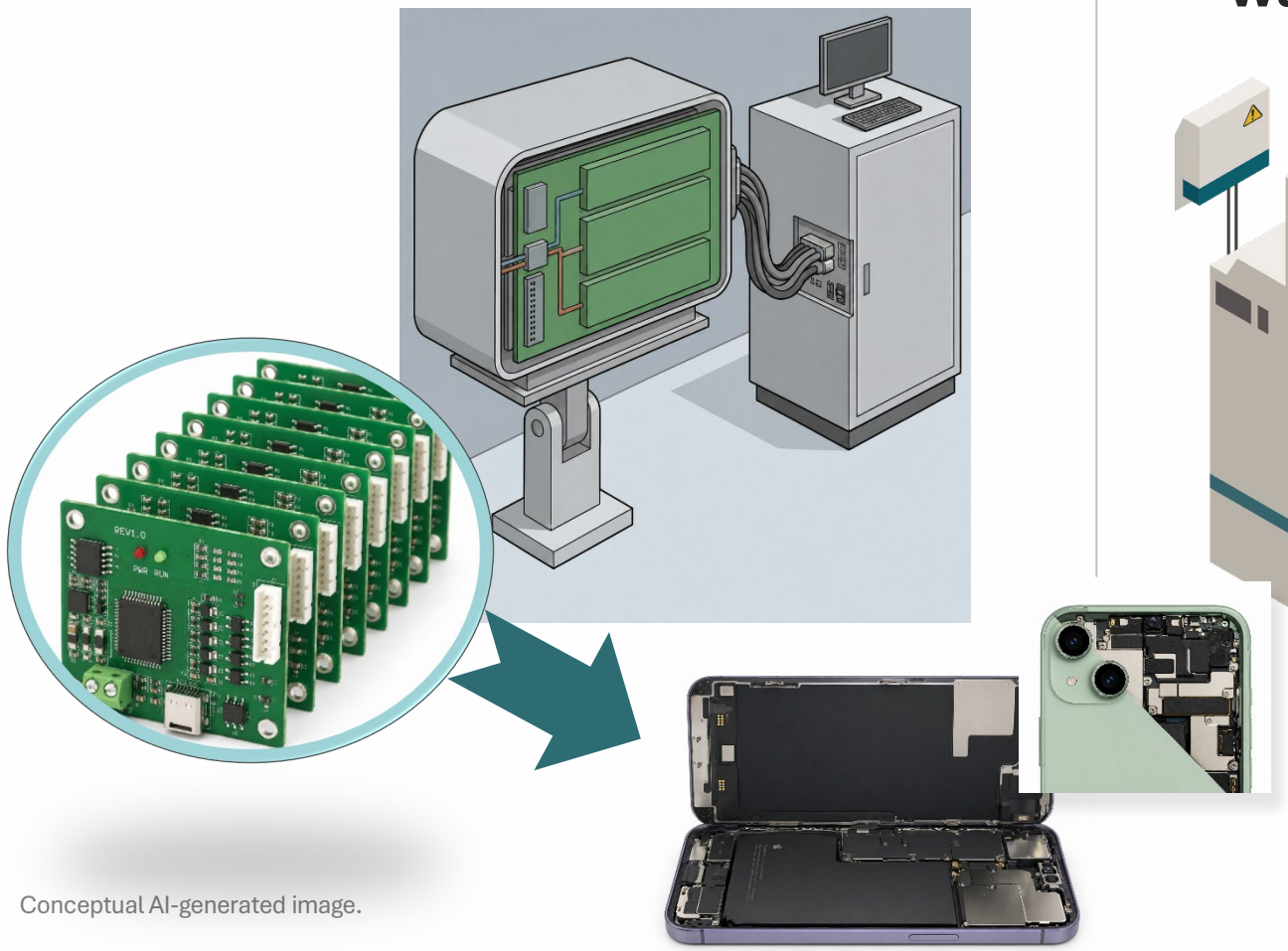
CONFICT

Space & Cost Reduction

Achieving Perfect Testing

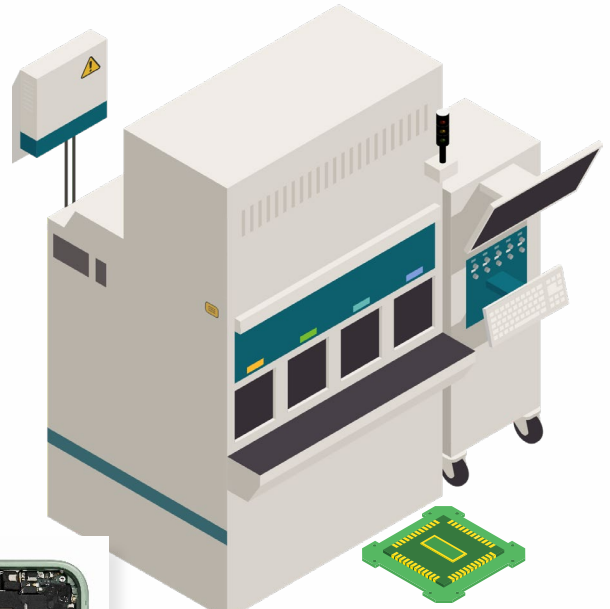
Reality in testing field – They are too bulky

Testers are as big as Refrigerators



Conceptual AI-generated image.

Quite Big Tools handle only One wafer or one chip carrier at a time



So reducing test time has large value

However,

what about Test perfection?

Sacrificing Perfect testing has been justified

01 Omitting test items

Can ✖ Imagin sl ✖ o like a ✖ ? I slept ✖ a ✖ last night

02 Virtual burn-in instead of real burn-in with the risk of overkill

Why? **Space cost is too high!**

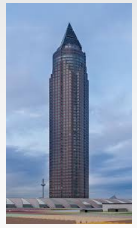
New measure on testing efficiency

01 → In case space matters → 02 → In case test perfection matters → 03

Productivity
= (# of chips) / (time)

: Typical Measure

+



Space Productivity
= (# of chips) / (time x space)

: Better Measure

+

Test Productivity
= (# of chips) x (degree of test perfection)/ (time x space)

: Best Measure

New testing mission = Optimizing Test Productivity
(# of chips) x (degree of test perfection)/ (time x space)

Three recommendations for wise test

Optimizing Test Productivity

((# of chips) / (time x space))x (degree of test perfection)

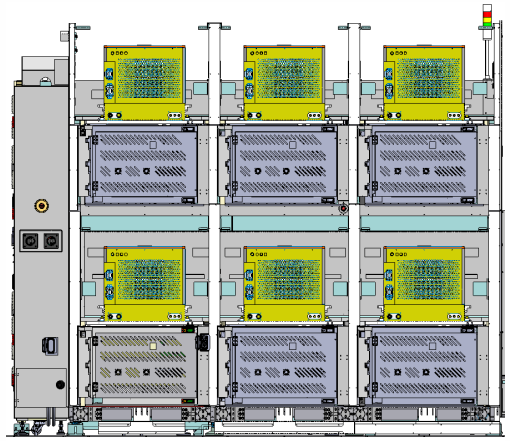
1. Go to Group testing
2. Make compact testers

3. Use the saved resource (time x space) for perfect testing

1 2 3 : Three new effective ways for AI Chip testing

Maximize Test Productivity with Group Testing

Group testing



Compact testers

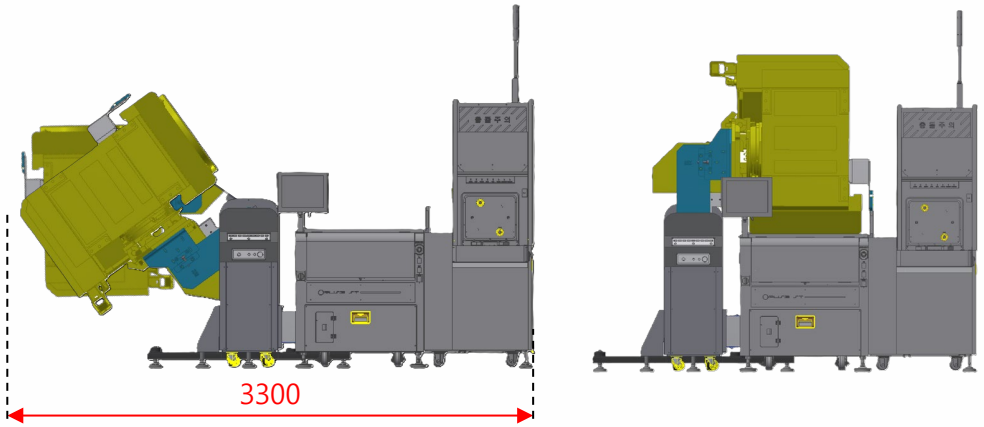
Earn Money

With the earned Money

Spend for
Perfect testing

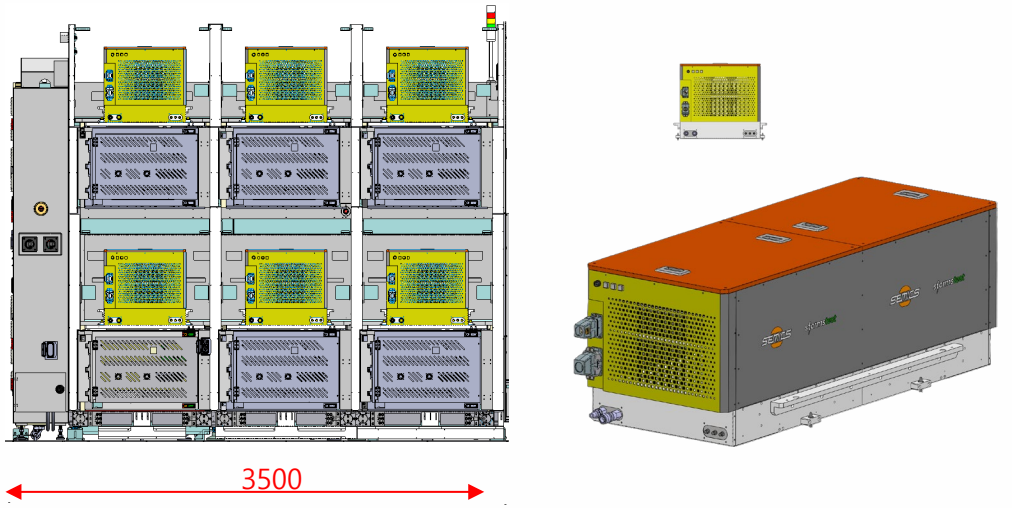
Compact testers need compact machines

Compact tester with bulky handler!



Non sense!!!

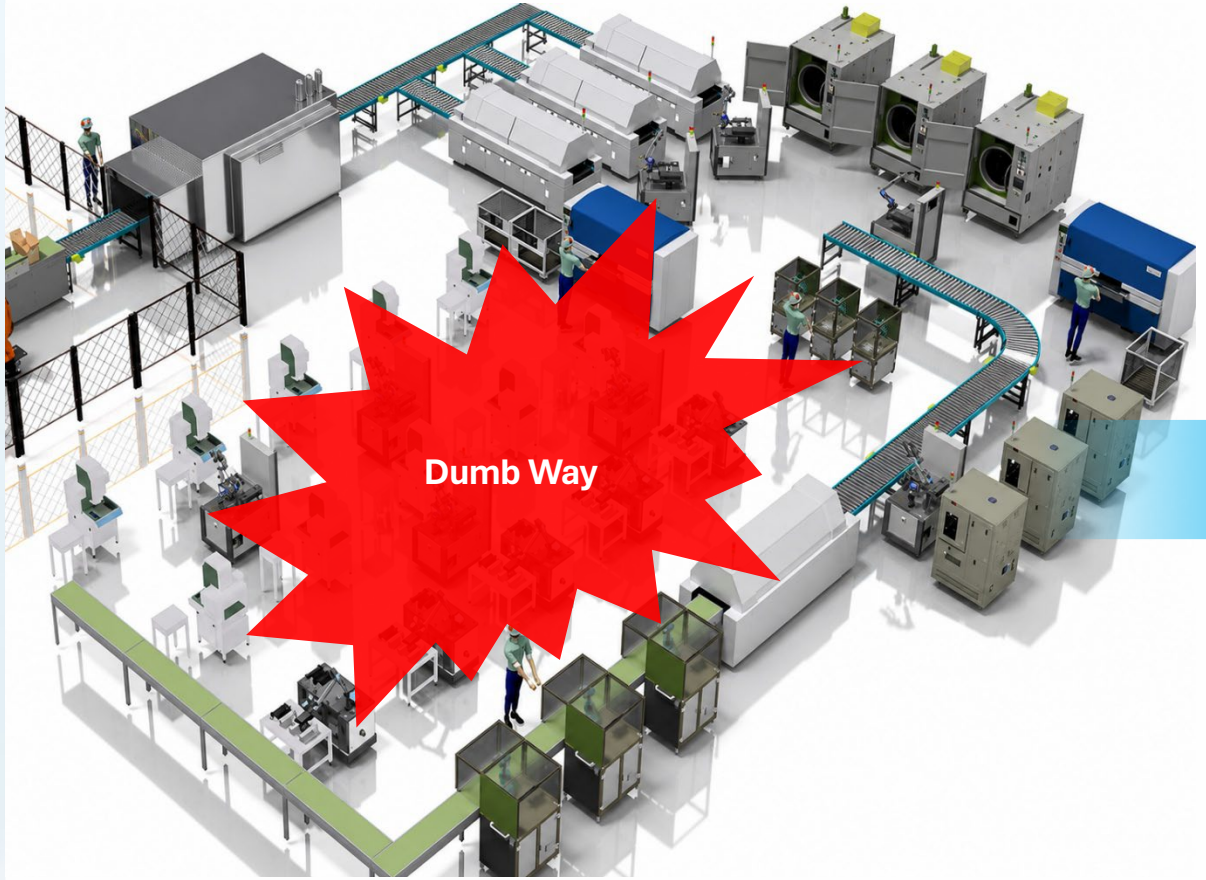
Compact testers with group testing tools!



Make sense!!!

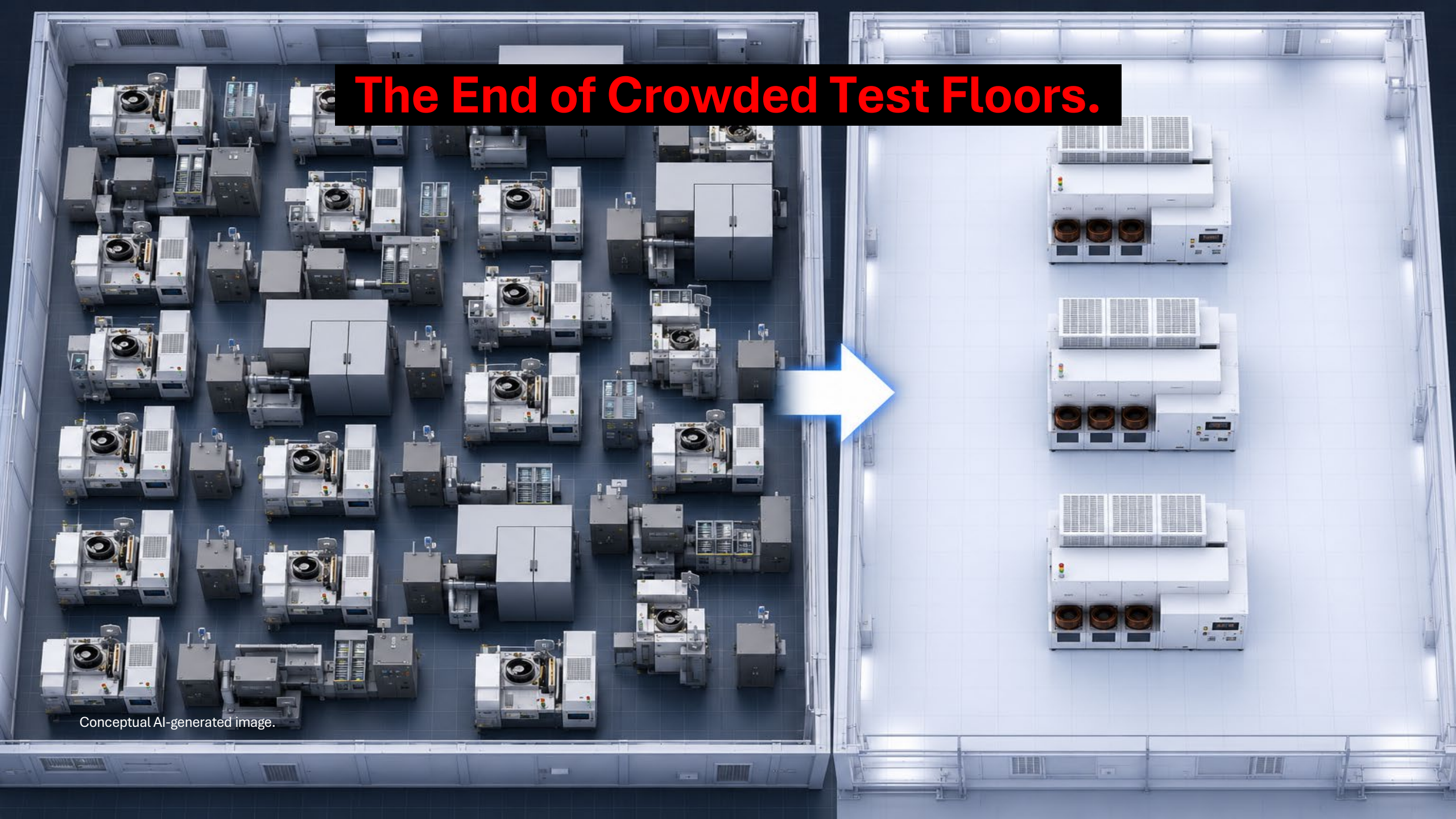
Single Prober: Still the Right Fit?

Save the space for perfect testing!



Smart Way!

Conceptual AI-generated image.

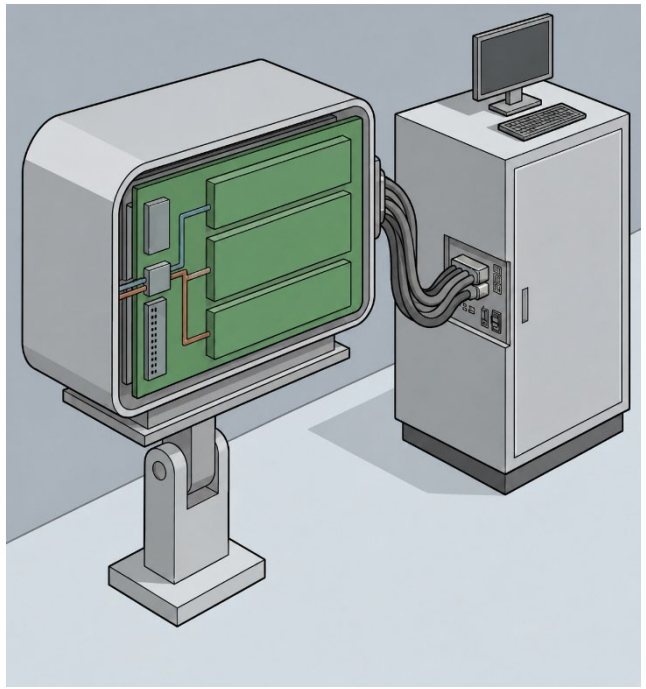

The End of Crowded Test Floors.
Conceptual AI-generated image.

Testers can be far more compact

if you are creative enough

2Gbps x 10000 channel tester

→ 20Tb/s



Conceptual AI-generated image.

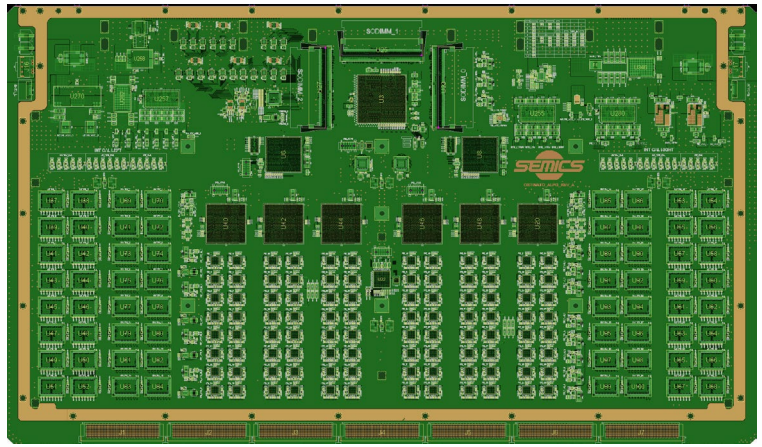
HBM4

→ 3.3TB/ =26.4Tb/s

Making ATE very compact

Strategy1 :

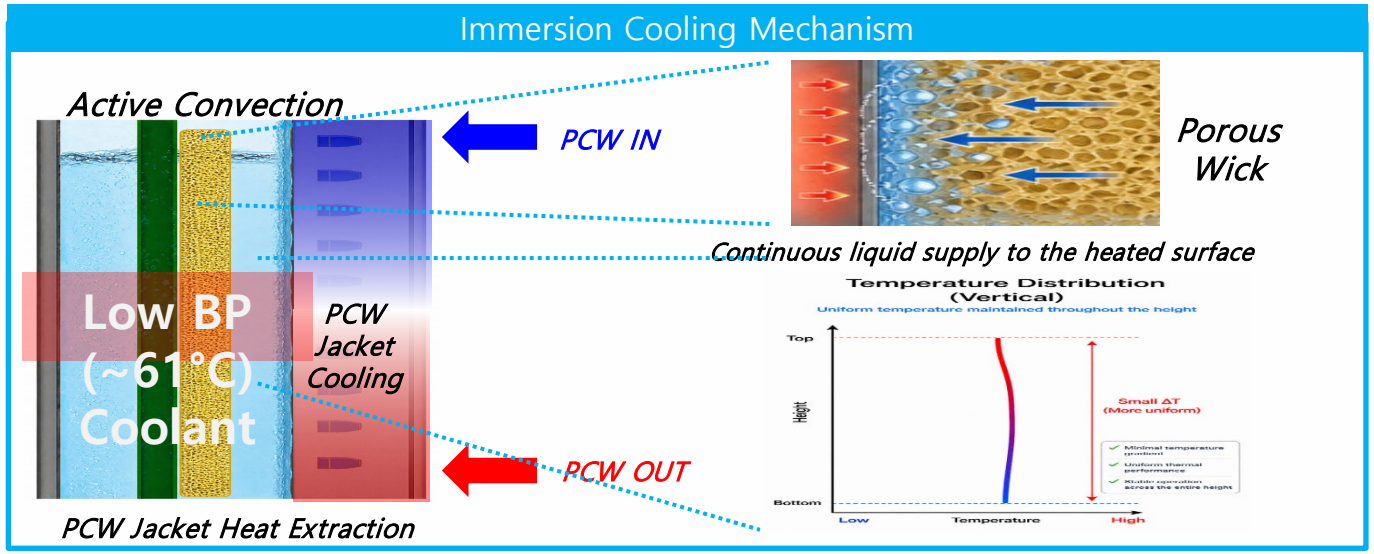
Putting as many chips as possible into the board



Conceptual AI-generated image.

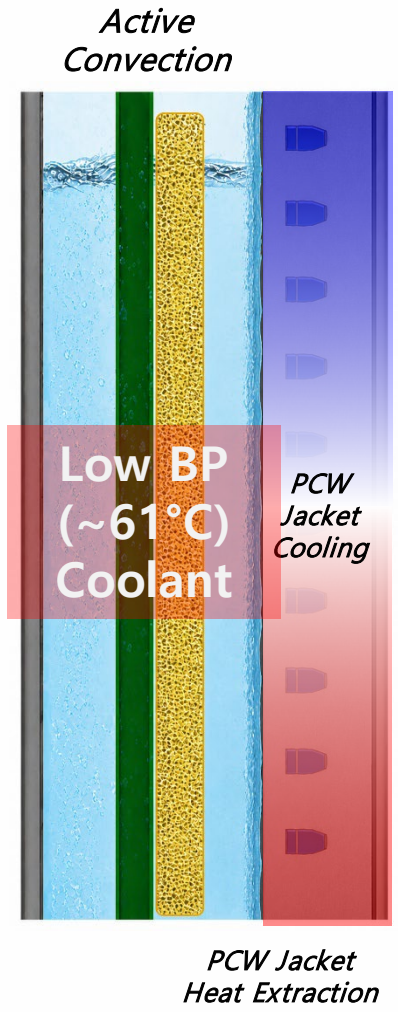
Strategy2 :

Heat dissipation is the key



Smart Immersion cooling of our own - no Chiller

Smart Immersion Cooling Mechanism



Heat exchange happen inside

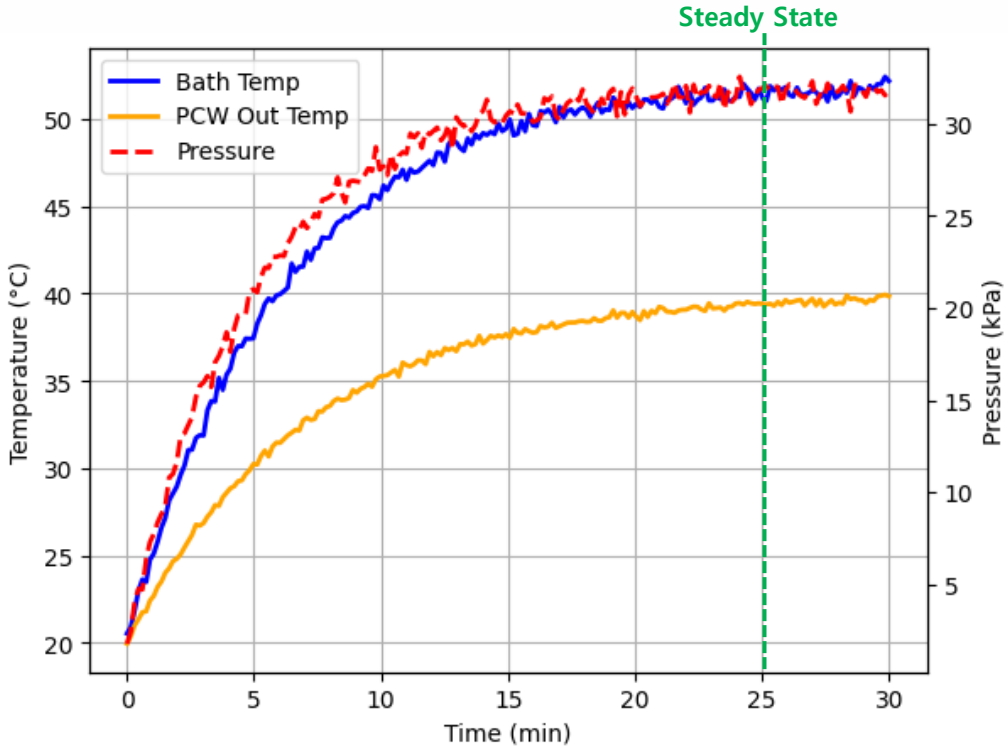
Using low boiling point coolant

Much better performance

Heat exchange ∝ Coolant Heat capacity

Stable Operation Maintained at 3000W Heat Load

Coolant < 55 °C , Pressure < 35 kPa

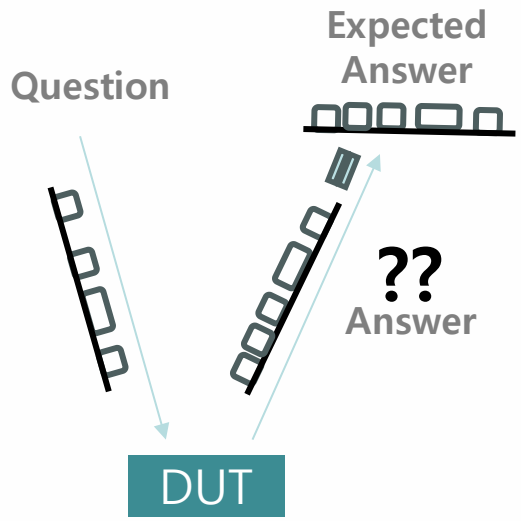


- High-Load Stability
- No Pressure Spike
- Uniform Temperature

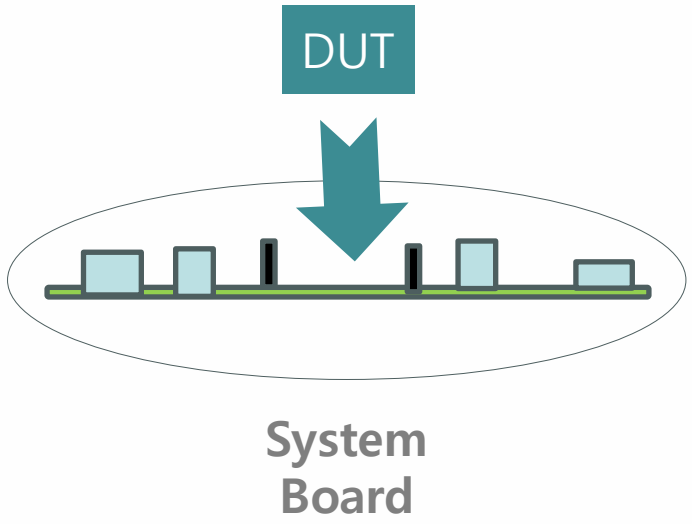
Three possible ways of testing chips

Long term vision: Getting out of ATE

ATE



SLT



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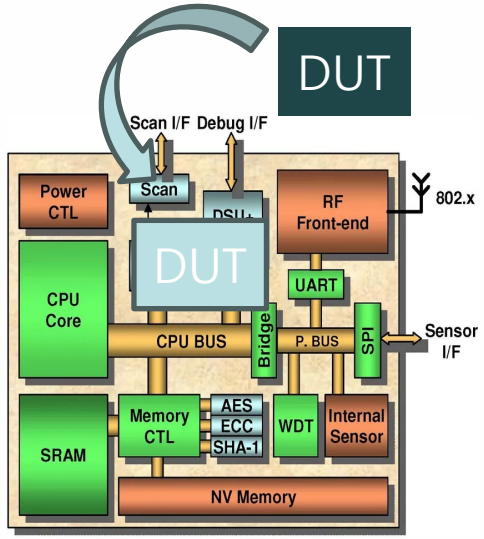


Circuit Designed for test

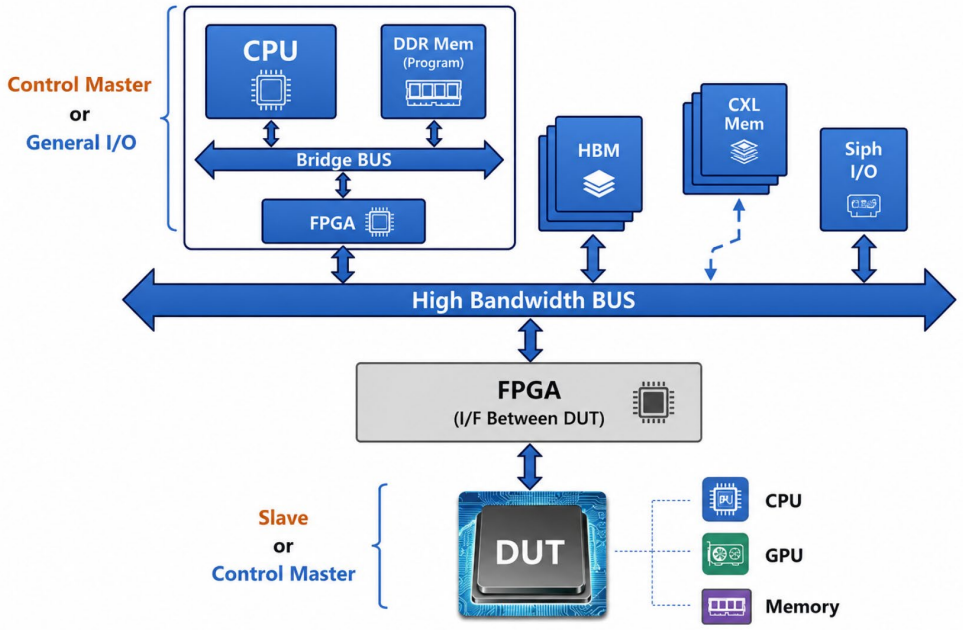
We call it

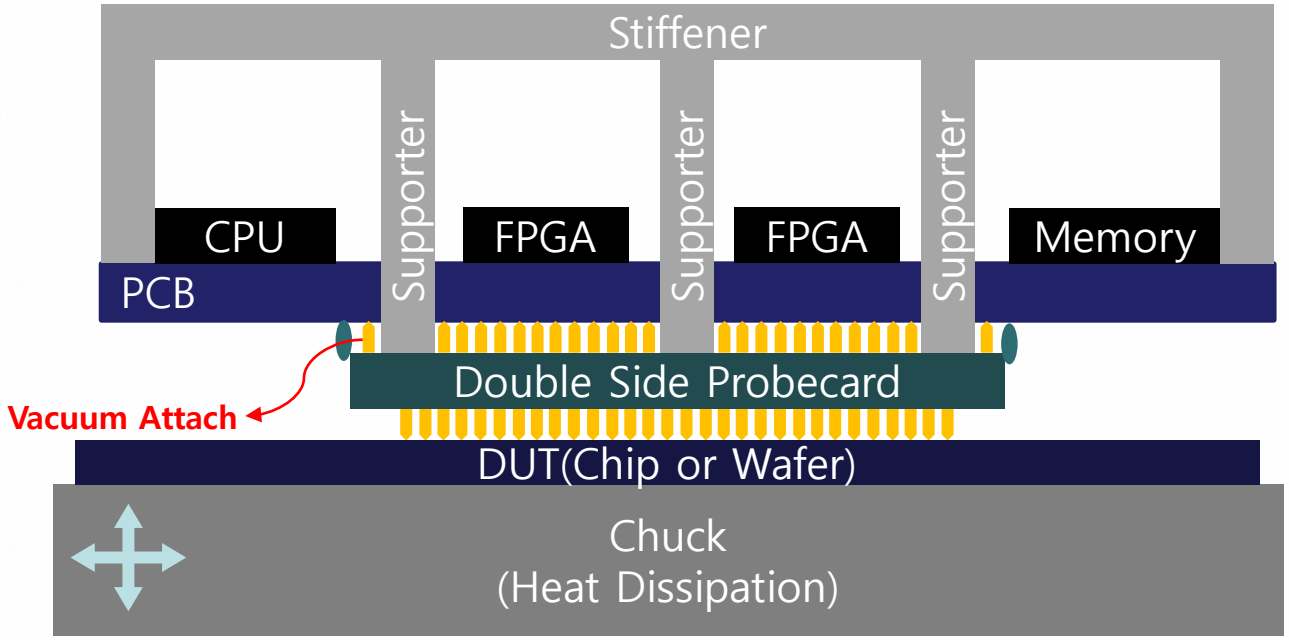
GTC (General test circuit)

Testing with GTC

Long term vision: Getting out of ATE

ATE or SLT? They are not the only options for function testing. We can also Test DUT with specially designed
GTC (General purpose testing circuit)





Ultimate Wafer & Die Level Burn-In Solution

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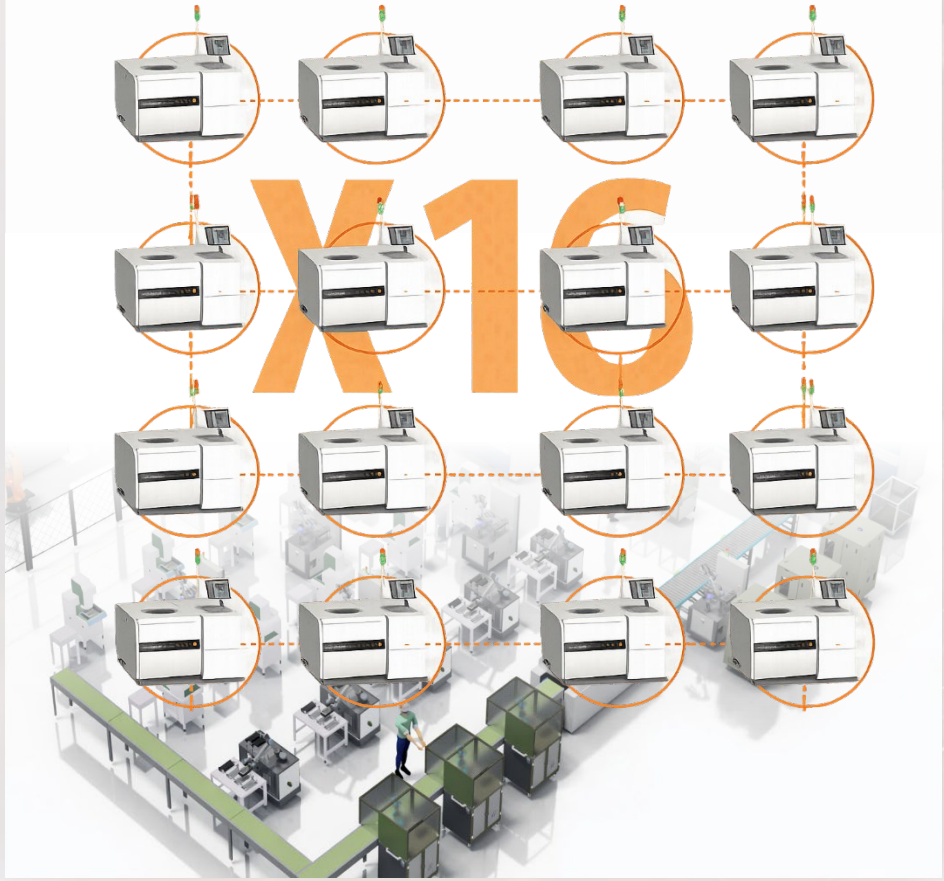
SINGLE 16 sets



Conceptual AI-generated image.

OSTINATO

Space efficiency!

Productivity improvement!

OSTINATO

Fully Automated Burn-In | Fast Changeover Operation | Space Efficient Design | High Density Test Solution

OSTIBUFFA

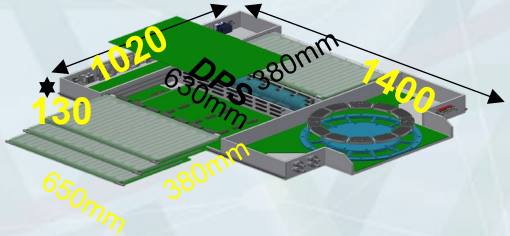
Low Cost of Ownership | Simple Floor Planning | Smart Factory Ready | Modular & Scalable System

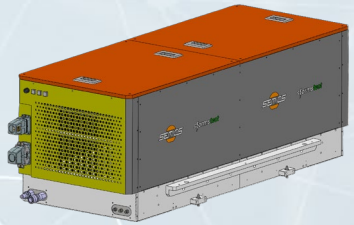
Three recommendations on AI chip testing

01 **Go to group testing**



02 **Make compact testers**



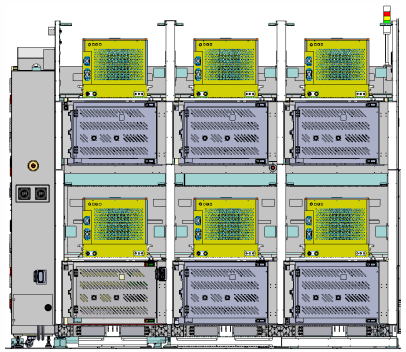


03 **Take time do not rush for burn-in with the perfect testing. Save overkill cost**




Summary

Group Test Solution



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Compact Test Solution

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Fantastic Testing Line

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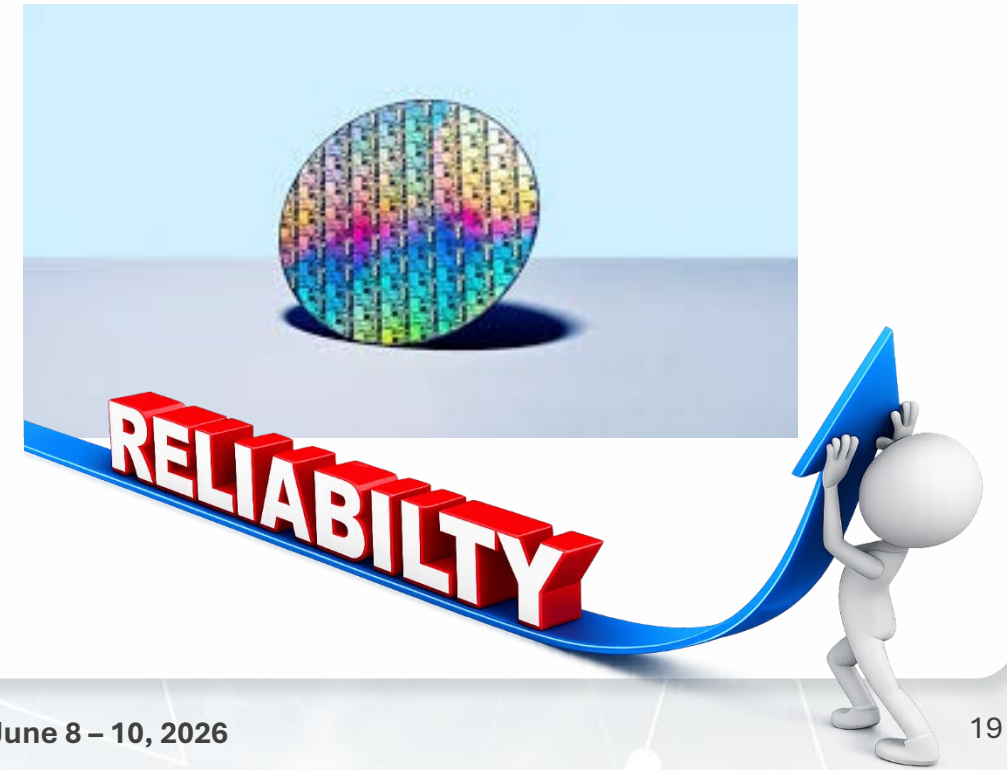
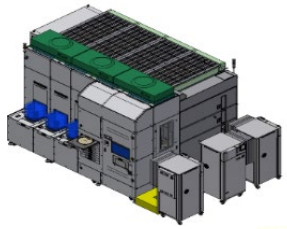


Conceptual AI-generated image.

GTE: The Greatest Test Empire

Ever



SEMICS(GTE)