SWTEST 2026 CONFERENCE

35th ANNIVERSARY

Mapping the Invisible: Dynamic Path Resistance De-embedding and Spatial Analytics

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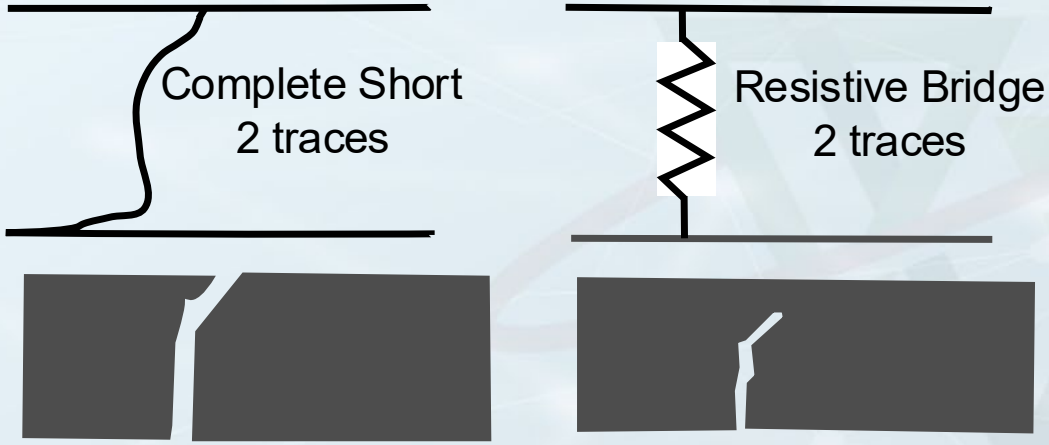
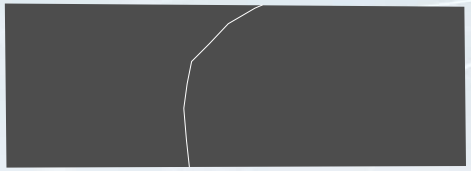
Noise Masks Real Defects

- **The Goal: Screen true defects without sacrificing yield.**
  - The Reality: Parametric and functional tests are highly sensitive to contact between probe needle to die pad. Relaxed HVM test limits **mask critical defects**.



Complete Open of metal line
Functional Fail

Resistive Open of metal line
Possible Parametric Fail



Small Crack in metal line Possible Speed failure
Sometimes called a Tunneling Defect

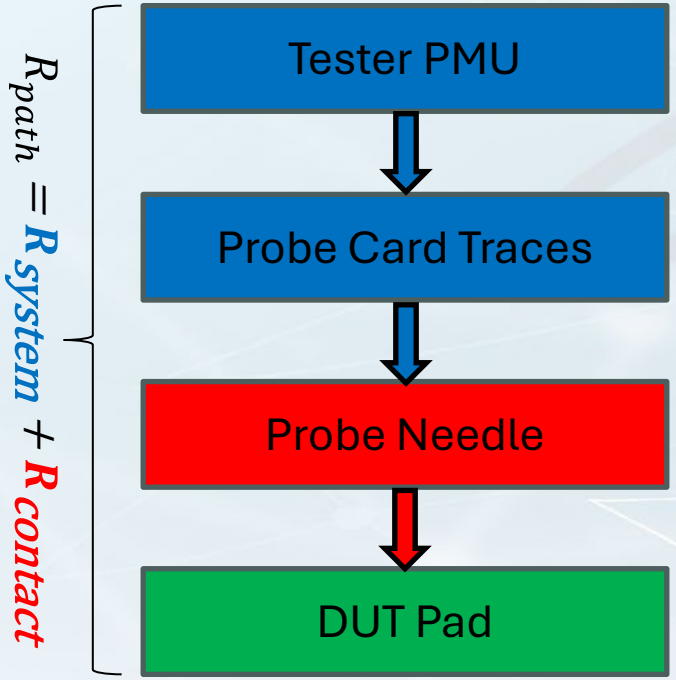
R_{path} Noise → Limit Relaxation → Masking → Defect Escapement

Prevents yield loss but increases defect escapement.

Hides resistive opens and tunneling-related leakage under widened guard-bands.

The Villain (Dynamic Path Resistance R_{path})

Total Path (R_{path}) = Static Tester Setup (R_{system}) + Dynamic Contact Resistance ($R_{contact}$). The dominant source of measurement drift in production is $R_{contact}$.



- R_{system} is static, but $R_{contact}$ fluctuates with every touchdown even tens of milliohms to ohms.
- $R_{contact}$ fluctuations are unpredictable due to poor contact from thermal drift and physical debris.

The Inadequacy of Standard Calibration

- ATE calibration fixes R_{system}— the real drift lives in $R_{contact}$
  - Dynamic $R_{contact}$ is completely ignored

Resistance Component	Classification	Type	Standard ATE Calibration Status
Tester PMU (R_{pmu})	Static (R_{static})	Tester dependent	✅ Compensated (Offline DC/TDR)
Loadboard & Probe Card (R_{trace})	Static (R_{static})	Hardware dependent	✅ Compensated (Shorting Blocks)
Probe Needle to Pad Interface ($R_{contact}$)	**Dynamic ($R_{dynamic}$)**	**Environment dependent**	**❌ UNCOMPENSATED (The Blind Spot)**

Brute Force Damages Hardware — It Does Not Fix the Data

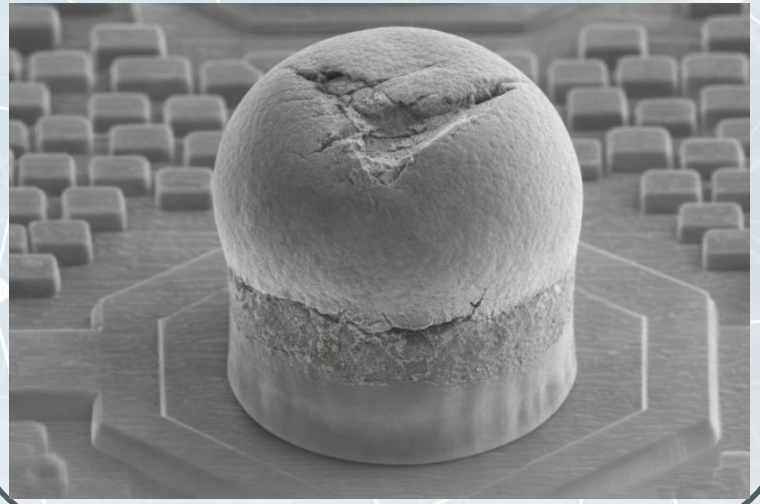
- Aggressive cleaning accelerates needle wear and shortens probe card life.
- Excessive overdrive damages bumps and increases downstream assembly risk.
- Without dynamic electrical compensation, cost rises while data integrity remains compromised.

Aggressive Cleaning

The Result of Lacking Dynamic Electrical Compensation

probe card lifespan ↓
capex ↑

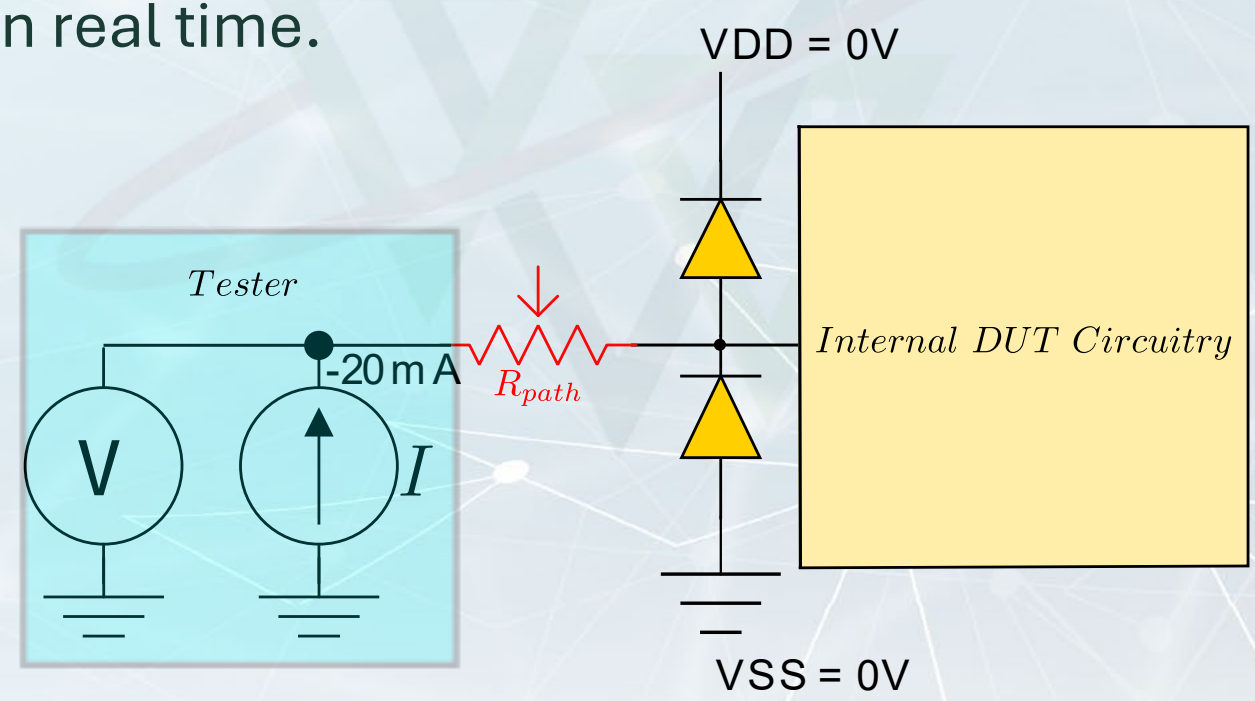
Excessive Overdrive



Mechanical mitigation treats the symptom, not the contact interface.

The Paradigm Shift: Measure the Interface Electrically

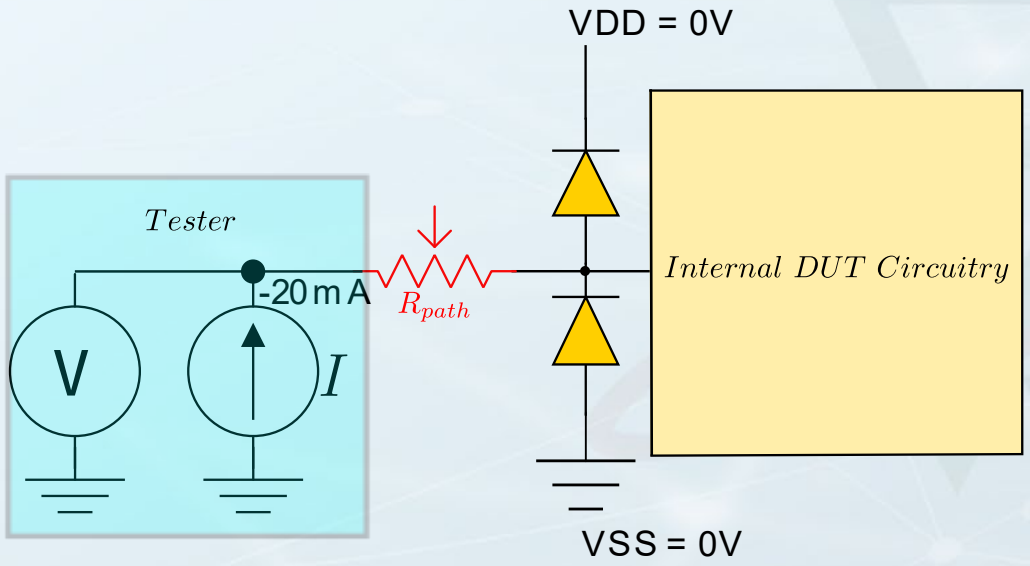
- Leverage existing ESD diodes already present in every IO.
- No dummy pads. No extra tester resources. No hardware redesign.
- Extract R_{path} in parallel for all IO with per pin measurement unit and compensate it in real time.



The contact interface becomes observable, controllable, and production-ready.

The FIMV Extraction Architecture

- **Force $-20mA$ (FIMV mode) across all pads in parallel.**



Step 1 **Force Current:** Inject $I_{force} = -20mA$* to forward-bias diode connected to VSS.

Step 2 **Measure Voltage:** Record V_{meas} at the tester PMU.

Step 3 **Isolate Path:** Subtract known V_{diode} drop from spice model (> 99 % accurate).

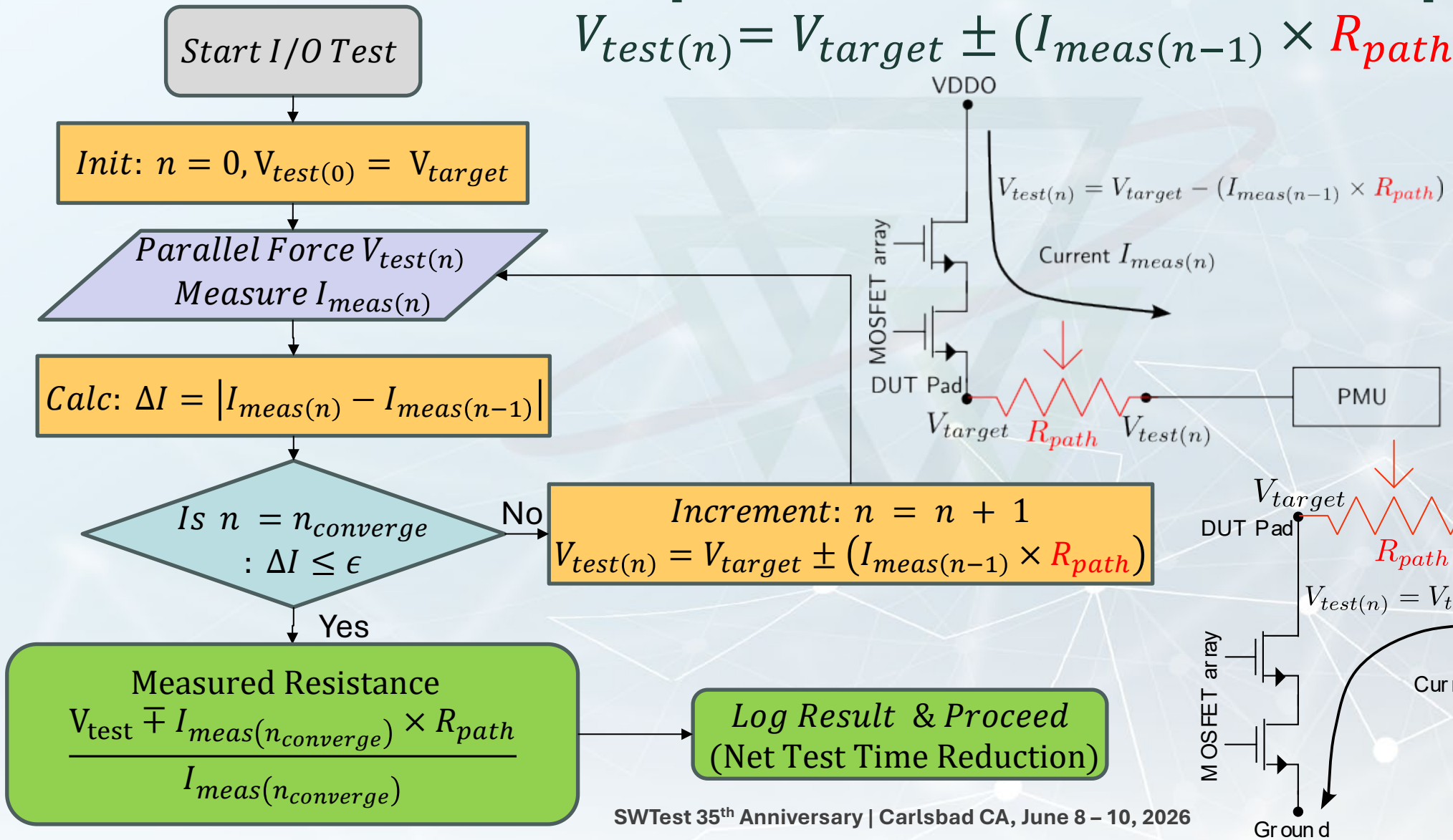
$$R_{path} = \frac{V_{meas} - V_{diode}}{I_{force}}$$

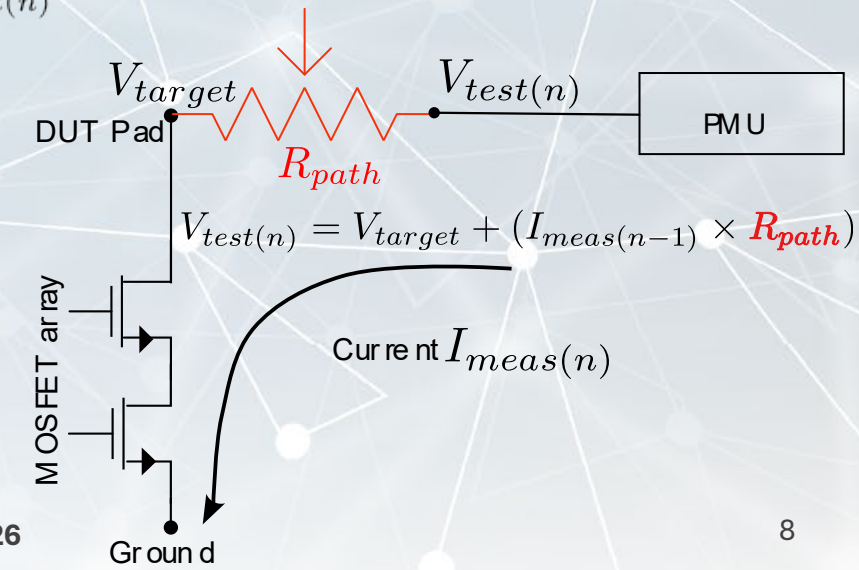
***Note:**

- Negative current -> Utilize Ground Plane as sink.
- Large 20mA to operate at diode linear region well within PMU spec of 50mA

Dynamic Compensation: Model-Independent Real-Time Loop.

$$V_{test(n)} = V_{target} \pm (I_{meas(n-1)} \times R_{path})$$

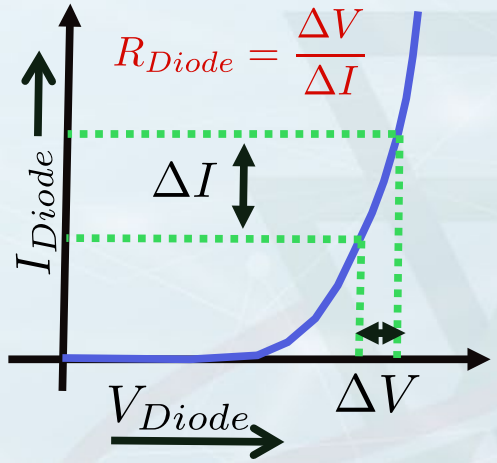




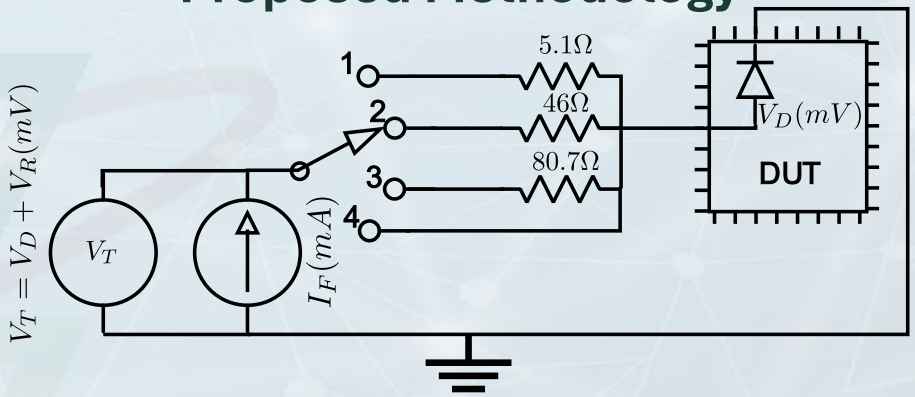
Lab Validation (Precision Analysis): Traditional Inaccuracy vs. Proposed Method

Conventional Delta-Slope Method

- Fails due to diode non-linearity
- Error rates render data useless for HVM



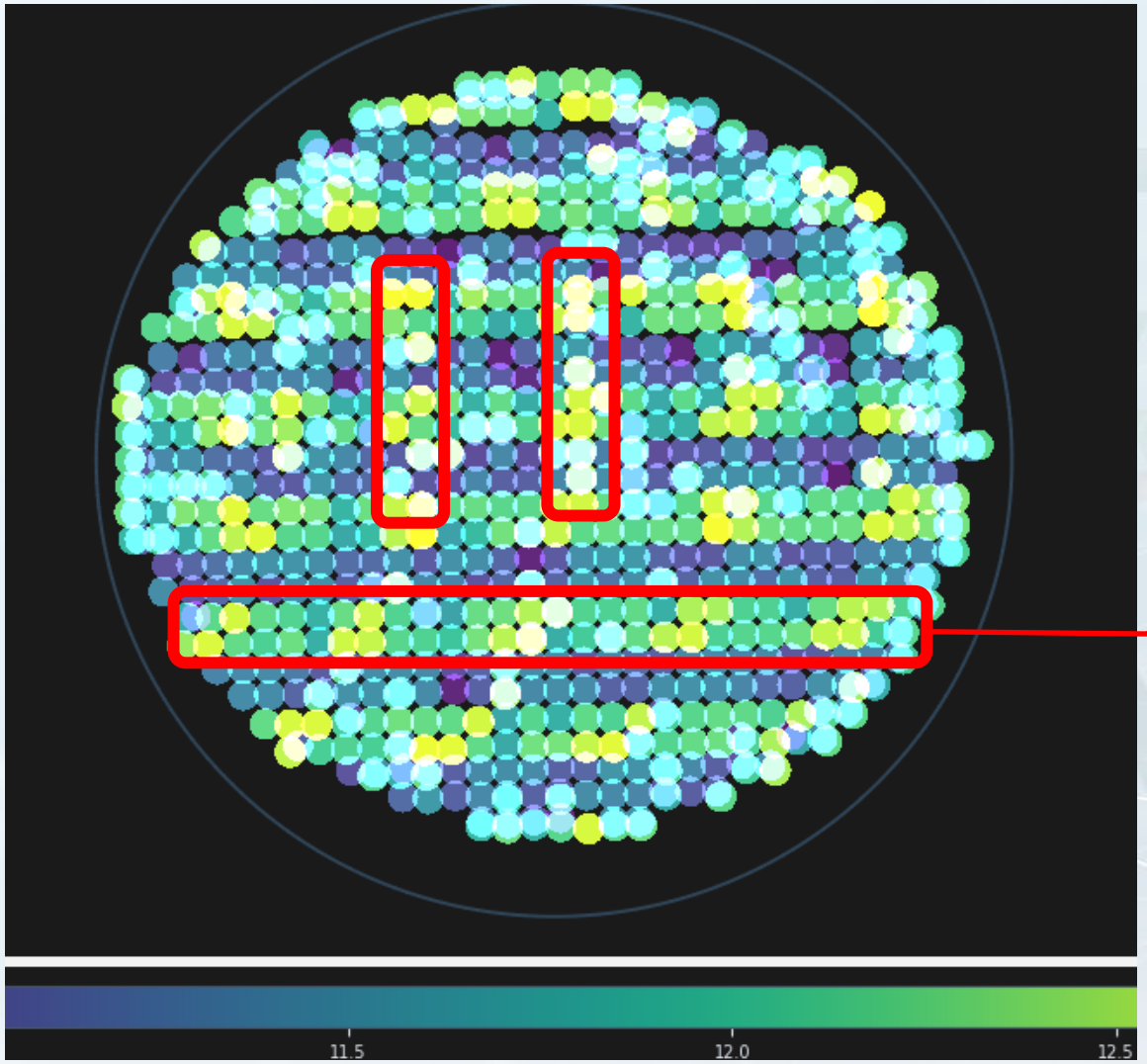
Proposed Methodology



- Spice Correlated Extraction
- Consistent accuracy across all resistance ranges

$Actual\ Resistor(R_A)$	$Conv.Slope\ Method(R_S)$	$Proposed\ Method(R_M)$	$Proposed\ Accuracy\ (A\%)$
5.1 Ω	41.5 Ω	4.86 Ω	−4.76%
46.0 Ω	83.0 Ω	46.14 Ω	+0.13%
80.7 Ω	**118.0 Ω**	**80.71 Ω**	**+0.02%**

Spatial Structure, Not Random Noise

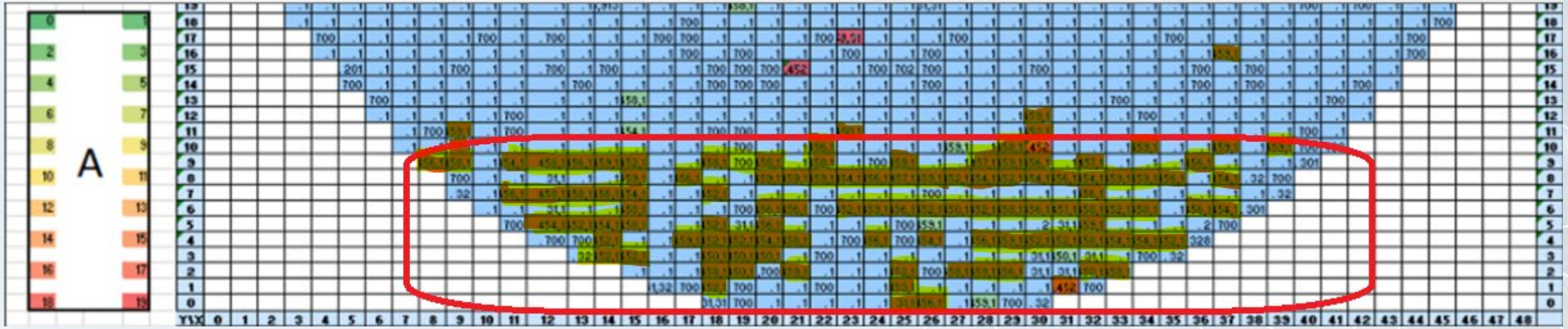


Spatial R_{path} mapping turns variation into insight

- Visible banding confirms non-random variation
- Hotspots indicate systematic contact effects
- Spatial mapping enables diagnostic insight

Spatial Diagnostics: Mapping the Invisible

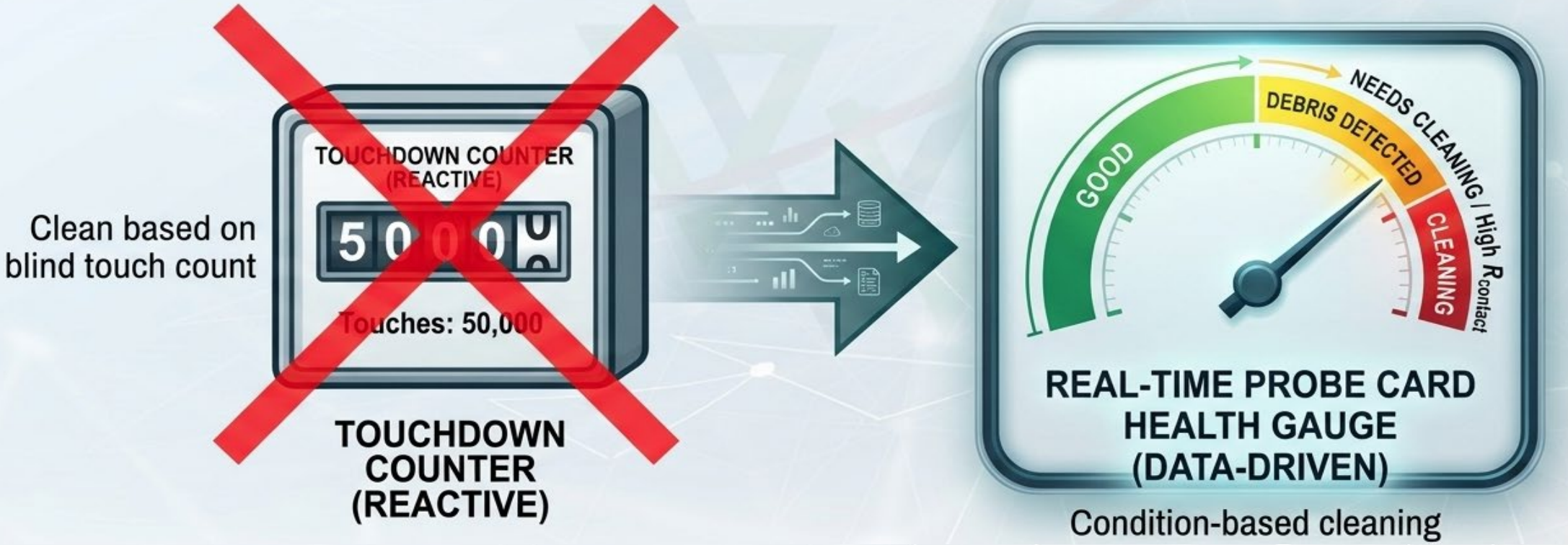
- Aggregated R_{path} heatmaps convert electrical variation into a spatial signature.
- Structured patterns expose systematic contact behavior across the wafer.
- In this lot, the map highlighted a planarity-related signature aligned with functional-test failure.



Left: Probe Card site array (A). Right: What once looked like noise becomes a diagnostic sensor for hardware state.

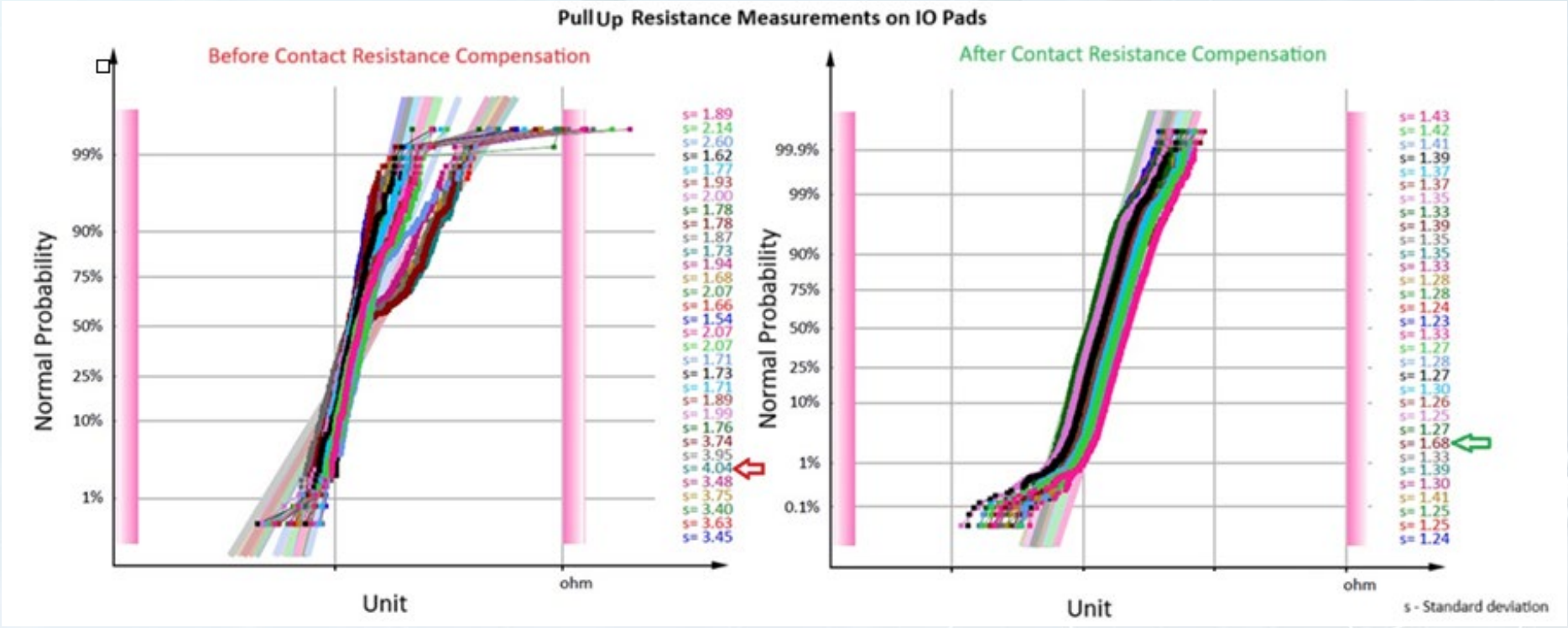
Predictive Maintenance

- **From blind touchdown cleaning……to data-driven predictive condition-based hardware maintenance.**
  - Trigger cleaning when R_{path} drift exceeds threshold



ROI

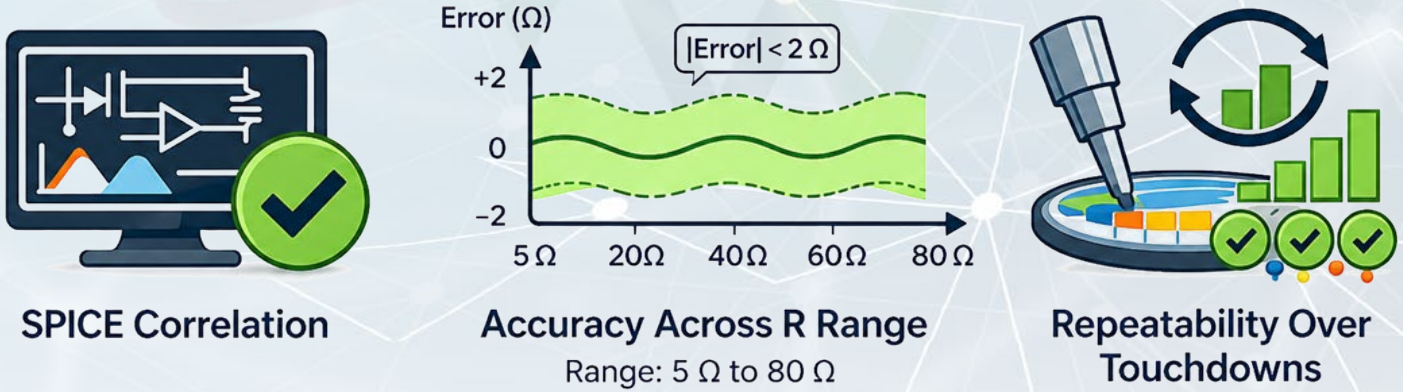
Probe Card/HW State	First Pass Yield (improvement)	Net Test Time Reduction	Probe Card Lifetime
Pristine (Optimal)	≥ 10 %	~3.5 %	+16 % extension
Degraded (Marginal)	~70 %	~25 %	+112 % extension



The above distribution is based on production data using optimal HW setup

Conclusion

- We de-embed dynamic R_{path} in real time (no new hardware).
- We prevent false fail/guard band-driven defect escapement with lab-validated accuracy.
- We convert R_{path} into a spatial diagnostic for failure analysis and predictive maintenance.



Thank You
Q&A

Summary of Impact

- **Accuracy:** Dynamically de-embedded R_{path} isolates true silicon performance.
- **Efficiency:** Net test time reduction and throughput increase with parallel extraction and compensation.
- **Intelligence:** Spatial mapping enables predictive, data-driven hardware maintenance.