SWTEST 2026 CONFERENCE

35th ANNIVERSARY

HIGH-THROUGHPUT SIC KGD TESTING: ENABLING MASS PRODUCTION VIA DUAL-DIE HANDLER ARCHITECTURE

Marcus Kontorowitz (Nexustest Pte Ltd)
Jiawei Lin (Nexustest Pte Ltd)
Allen Zhang (Nexustest Pte Ltd)
Yishen Zhang (Nexustest Pte Ltd)

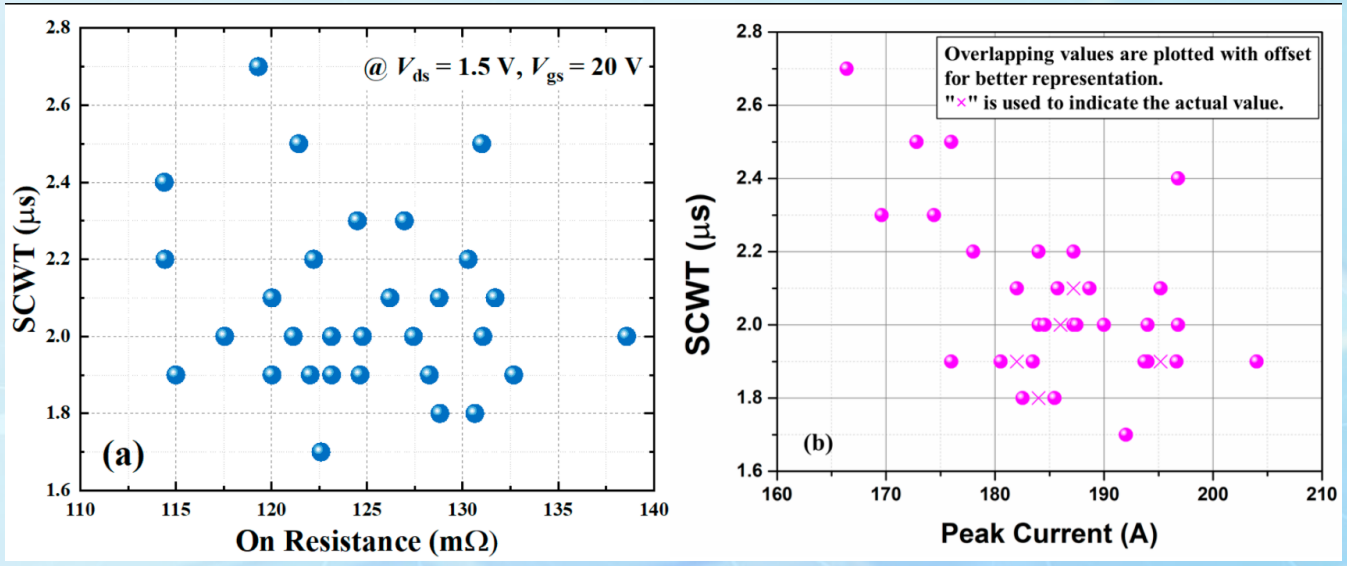
NEXUSTEST

Table of Content

- Introduction and Background
- Objective
- Methodes
- Results
- Summary

Static DC Tests ≠ Short-Circuit Survival

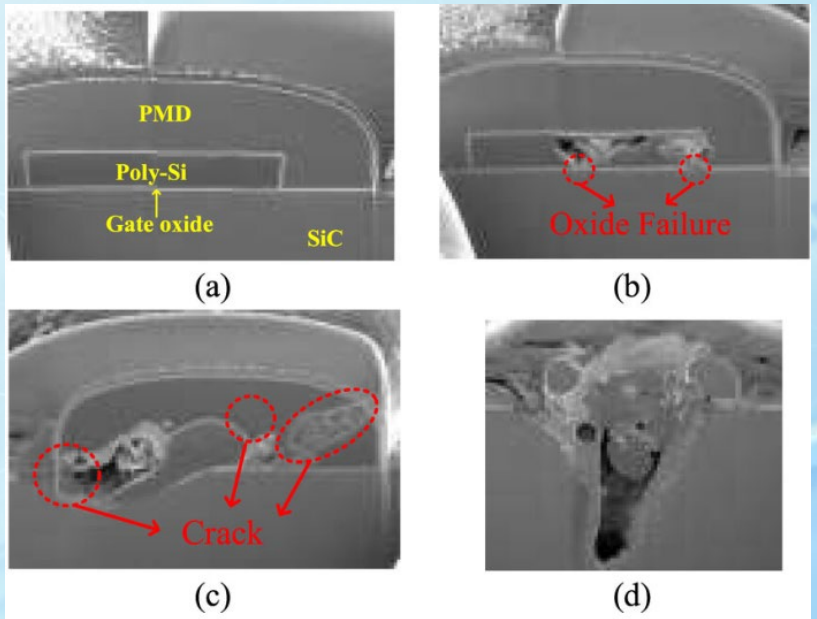
- **Detection Gap:** Wafer-level Vth and RDS(on) miss sub-micron L_ch variations.
- **Fabrication Impact:** A 10% L_ch misalignment reduces SCWT by 0.5µs.
- **Economic Loss:** Screening bare dies avoids 3x packaging cost multipliers.
- **Automotive Mandate:** Dynamic testing eliminates 2% to 3% EV inverter field failures.



Source: Nayak, S., et al. (2025). "Short Circuit Withstand Time Screening of 1.2 kV Commercial SiC MOSFETs: A Non-Destructive Approach." *Electronics*.

Microsecond Failure Mechanics

- **Compressed Window:** High power densities limit SiC survival to only 2 to 7µs.
- **Thermal Runaway:** JFET hotspots exceed 1500K, triggering uncontrollable current runaway.
- **Oxide Rupture:** Extreme heat and fields (2 to 3 MV/cm) cause immediate gate dielectric breakdown.
- **Mechanical Cracking:** Thermo-mechanical stress fractures the interlayer dielectric, causing gate-source shorts.
- **Parasitic BJT:** High temperatures activate the internal NPN structure, leading to total device burnout



SEM images of cross-section (a) undamaged cell, (b) DUT-1 with tw = 8 µs: GOX and Poly failure, (c) DUT-2 with tw = 8.5 µs: GOX, Poly, and PMD are damaged, (d) DUT-2 with tw = 8.5 µs: another cell with more severe damage to both gate and SiC epitaxial layers.

Source: Yao, Y., et al. (2025). "Gate failure process and mechanism of SiC MOSFETs under the effect of multiphysics field during short-circuit transients." *Semiconductor Science and Technology*.

Throughput Evolution: 1.5k vs. 4.0k UPH

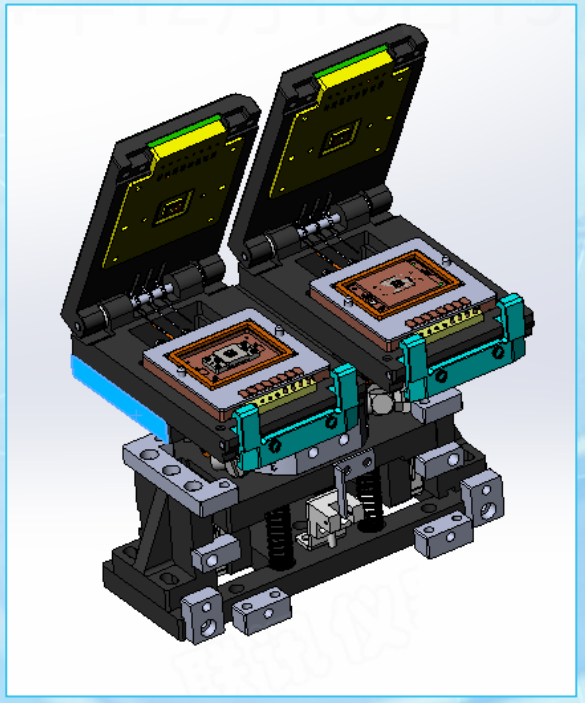
- **Last Generation:** Single-die turret capped at ~1,500 UPH by serial mechanical limits.
- **Next-Gen Hybrid:** Dual-die, 6-site parallel design scales throughput past 4,000 UPH.

High-Throughput Parallel Handler Architectures

- **6-Die Parallel Testing:** Dual-die sockets across multiple stations shift throughput to high-volume manufacturing.
- **Hard-Docking:** Rigid tester-to-handler docking minimizes stray inductance (<40 nH) for fast short-circuit protection.
- **Arcing Prevention:** Sealed, nitrogen-purged sockets eliminate electrical arcing during bare-die high-voltage sweeps.
- **Station Decoupling:** Separating loading/unloading from the test cycle prevents mechanical handling bottlenecks.

High-Parallelism Dual-Die Architecture

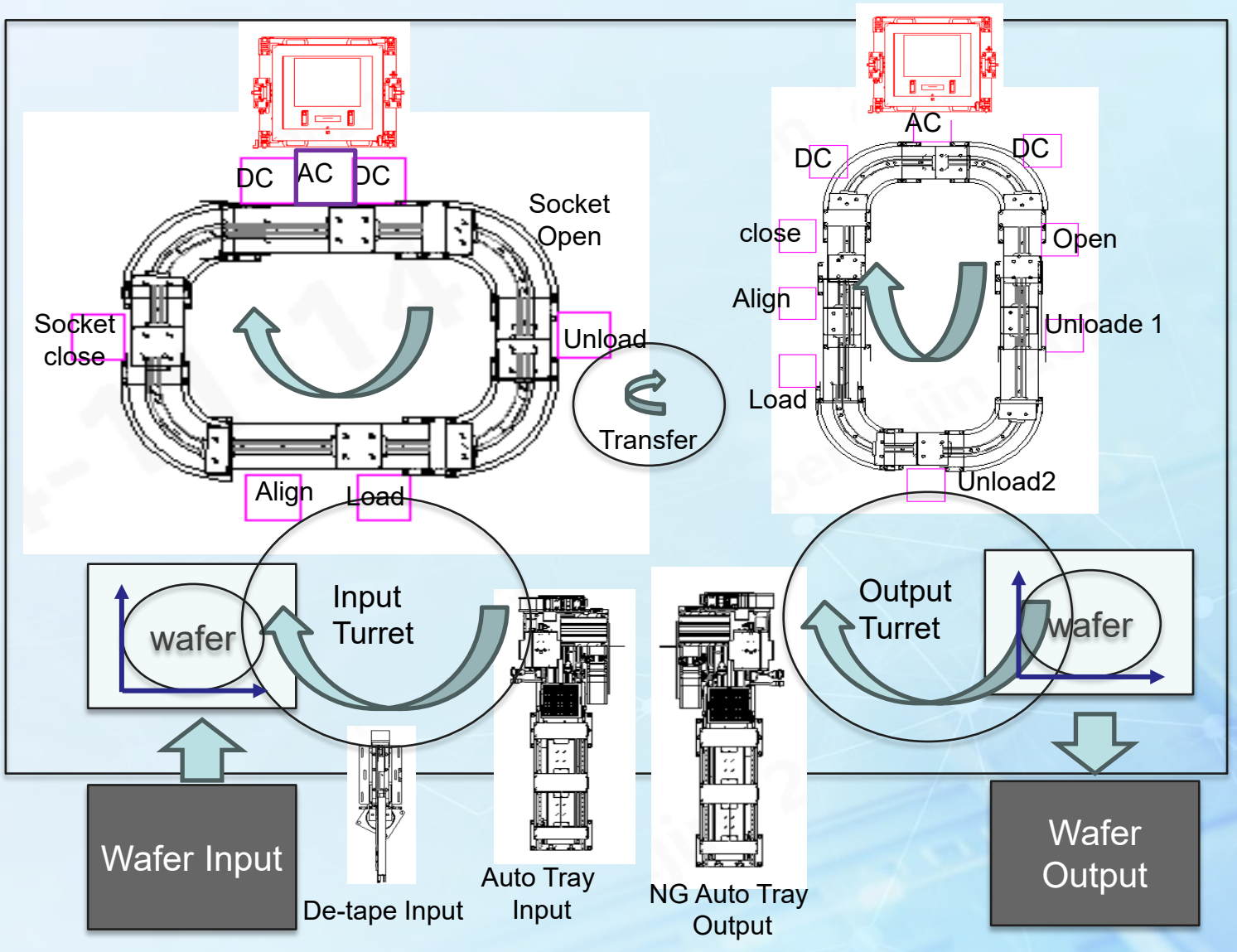
- **Throughput Scaling:** Two dies per touchdown across parallel stations enables >4000 UPH.
- **Resource Efficiency:** Shares common tester instrumentation while maintaining independent, per-channel device monitoring.
- **Index Parallel Advantage:** Synchronous indexing minimizes mechanical "dead time" to maximize dynamic stress test coverage.
- **TCO Reduction:** Shifting from single-site probing to multi-site dual-die architecture is the primary lever to lower SiC manufacturing costs.



Rationale for Hybrid Turret-Track Design

- **Handling Decoupling:** Turrets manage loading/binning; Tracks drive high-speed testing.
- **Thermal Soak:** Linear tracks ensure full thermal equilibrium before electrical testing.
- **I/O Flexibility:** Seamless integration with diverse media (Wafer, Tape & Reel, Tray).
- **Vibration Control:** Fast rotational motion from test contacts.
- **Flow Optimization:** Decouples thermal processes from electrical characterization to prevent throughput bottlenecks.

Hybrid Turret-Track Design



Technical Logic of Hard-Docking Interfaces

- **Parasitic Inductance:** Rigid interfaces eliminate cable loops, maintaining the ultra-low inductance required for reliable SCT.
- **Voltage Overshoot:** Minimized loop area prevents destructive drain-source spikes during fast switching transients.
- **Signal Integrity:** Tight coupling of ground and power planes preserves high-speed waveform accuracy.
- **Active Safety:** Stable electrical paths enable precise, high-speed protection to prevent "die burst" or probe damage.
- **Measurement Repeatability:** Mechanical rigidity ensures consistent contact force and alignment across all test sites.

Nitrogen-Purged Sockets: Eliminating HV Arcing

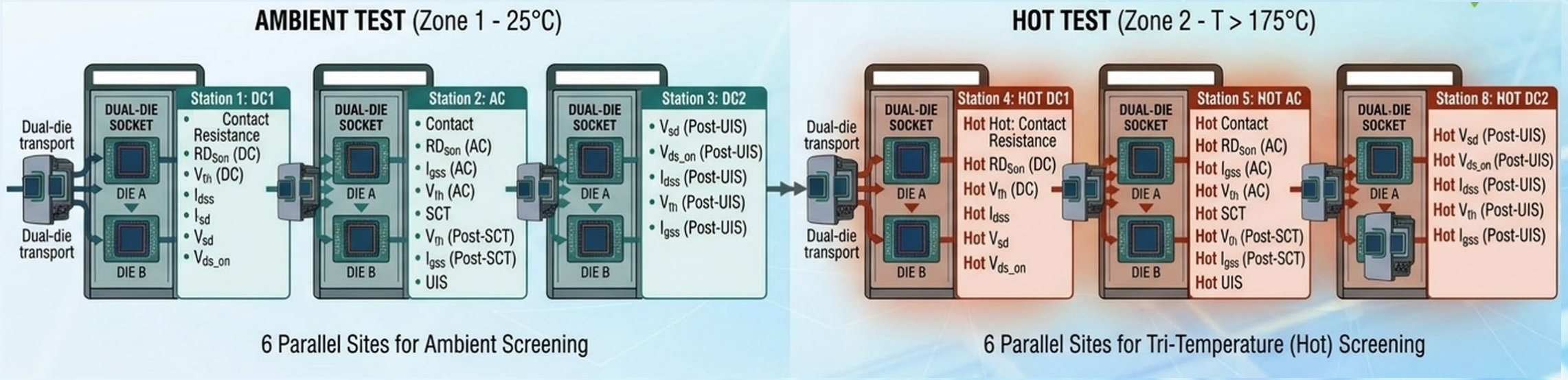
- **Arcing Mitigation:** High-voltage testing of bare dies triggers electrical discharge; nitrogen (N2) gas increases the breakdown threshold to suppress this.
- **Zero-Residue:** Unlike dielectric liquids, N2 is dry and non-conductive, eliminating the need for solvent cleaning and reducing probe contamination.
- **Environmental Edge:** N2 is a non-toxic, zero-GWP alternative to SF6.

SiC KGD Throughput: 4,000 UPH

Breaking the 3k Ceiling: Holistic system optimization surpasses the limitations of simple dual-die integration.

6-Site Parallelism: Unified configuration enables simultaneous, independent screening to reach 4,000 UPH at 0.7s test time.

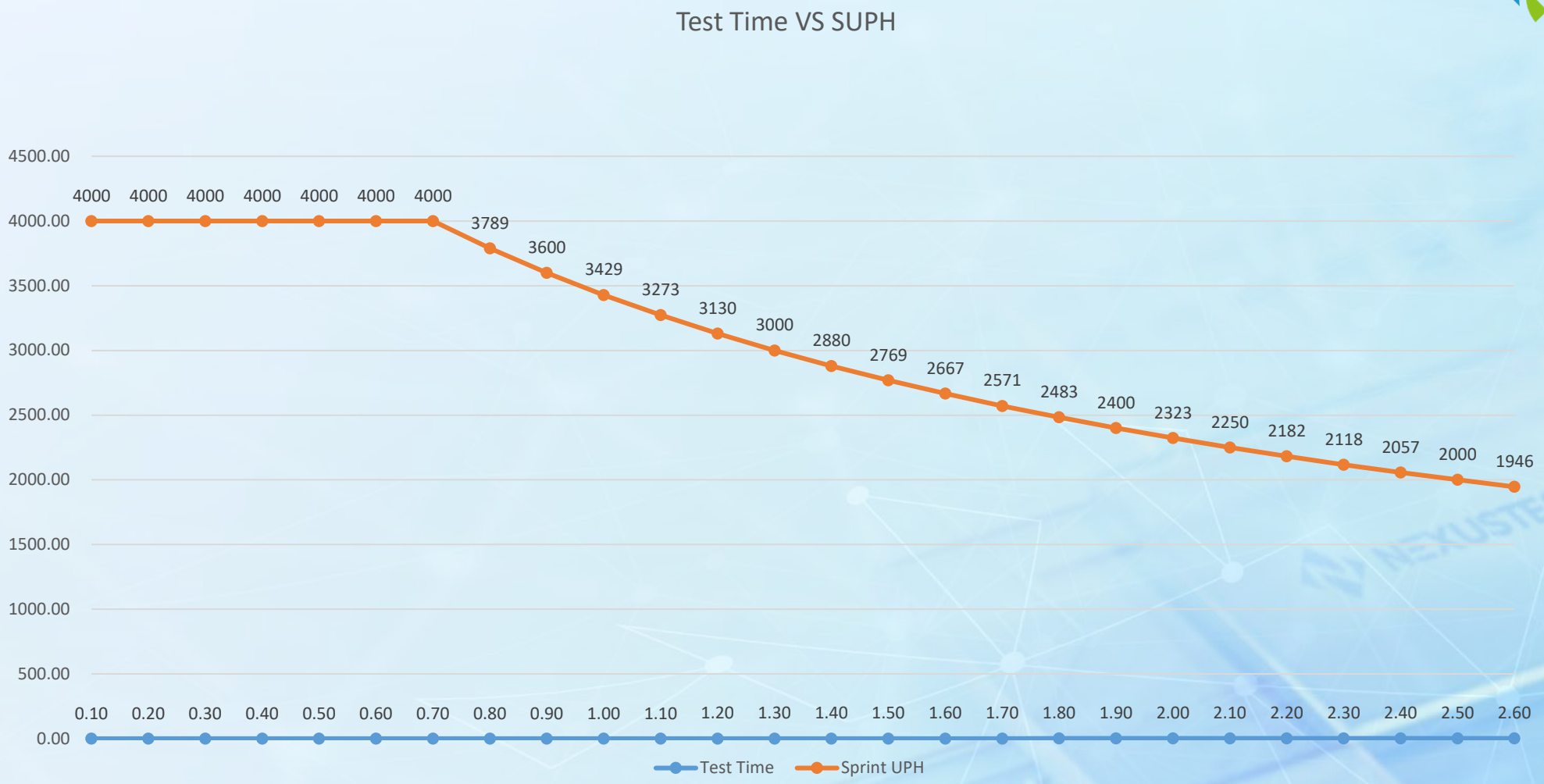
Decoupled Cycles: Separating high-speed indexing from long stress-dwells (SCT/UIS) eliminates handler idle time and stabilizes throughput.



Cycle Time Breakdown

Movement	Time [s]
Input/ Output Module	
Die positioning	0.14
Nozzle pickup	0.20
Turret rotate	0.24
Cycle Time (total)	0.58
Test Module	
Socket movement	0.28
Socket contact	0.20
Test time	0.70
Communication	0.10
Cycle Time (total)	1.28

UPH Chart


Test Time VS SUPH
4500.00
4000.00
3500.00
3000.00
2500.00
2000.00
1500.00
1000.00
500.00
0.00
4000 4000 4000 4000 4000 4000 4000 3789 3600 3429 3273 3130 3000 2880 2769 2667 2571 2483 2400 2323 2250 2182 2118 2057 2000 1946
0.10 0.20 0.30 0.40 0.50 0.60 0.70 0.80 0.90 1.00 1.10 1.20 1.30 1.40 1.50 1.60 1.70 1.80 1.90 2.00 2.10 2.20 2.30 2.40 2.50 2.60
Test Time
Sprint UPH

Summary

- **Dual-Die Socket:** Doubles test site density to evaluate 6 dies in parallel, maximizing utilization and reducing test costs.
- **Hard Docking:** Uses rigid interfaces to keep loop inductance below 40nH, suppressing high-power short-circuit transients.
- **Arcing Prevention:** Uses N2-purged micro-environments to eliminate electrical discharge up to 3000V.
- **Hybrid Design:** Combines linear tracks and rotary turrets to isolate mechanical bottlenecks from long electrical stress cycles.
- **4000 UPH Standard:** Breaks the 3000 UPH barrier, establishing a stable, zero-defect-compatible HVM screening standard for EV traction inverters.

Nexustest PB6800 KGD Handler Key Features

Key Features

- Dual Die Testing
- Very low AC stray inductance <40nH (Direct Docking)
- Single contact per Test turret
- Auto Socket cleaning and replacement
- Integrated 6S AOI
- Available with 6x T&R outputs
- Up to 4000 UPH

State of the art KGD handler for highest throuput with integrated AOI and T&R to provide industry leading performance and lowest cost of ownership for our automotive SiC customers

NEXUSTEST

Thank You!