SWTEST 2026 CONFERENCE

35th ANNIVERSARY

Micro Bump Probing: High Volume Experience Driven Capability Demonstration and Direction for Advanced 3D/2.5D Packaging

intel foundry

FormFactor™

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1 - Intel Foundry
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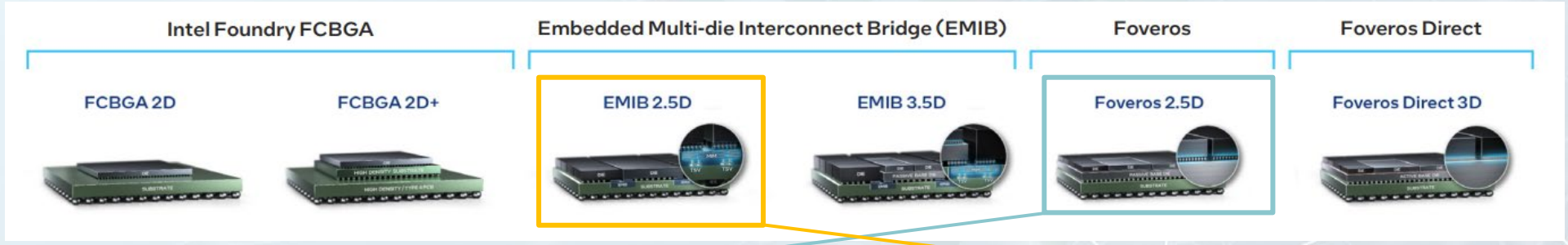
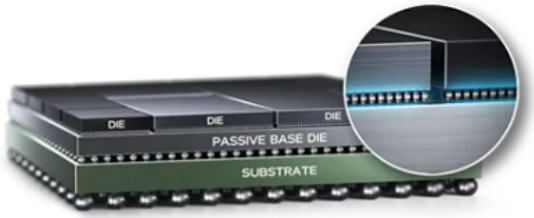
Outline

- Motivation, Background and Challenges w/ µBump probing
- Foveros DOW36 vs. EMIB: Layout and Probing Solutions
- Intel µ-Bump Experience: Qual Strategy, Results and HVM Production Expertise
- Summary and Outlook

Motivation

- **Recent trends drive increasing demand for proven / capable micro-bump probing technologies**
  - Explosive growth of AI workloads; Advanced heterogenous integration across multiple silicon technology nodes; Aggressive interconnect pitch scaling; Known-good die (KGD)
- **Intel has extensive experience with micro-bump probing in <u>High Volume Production</u> through the Foveros product line (HVM starting in 2019) – with plans to enable micro-bump probing on EMIB devices this year**





Foveros-S 2.5D

Next generation package optimized for cost/performance.

- Silicon interposer with 4x reticle.
- Applicable in client applications.
- Ideal for solutions with multiple top die chiplets.
- Production proven: In mass production since 2019 with active base die.

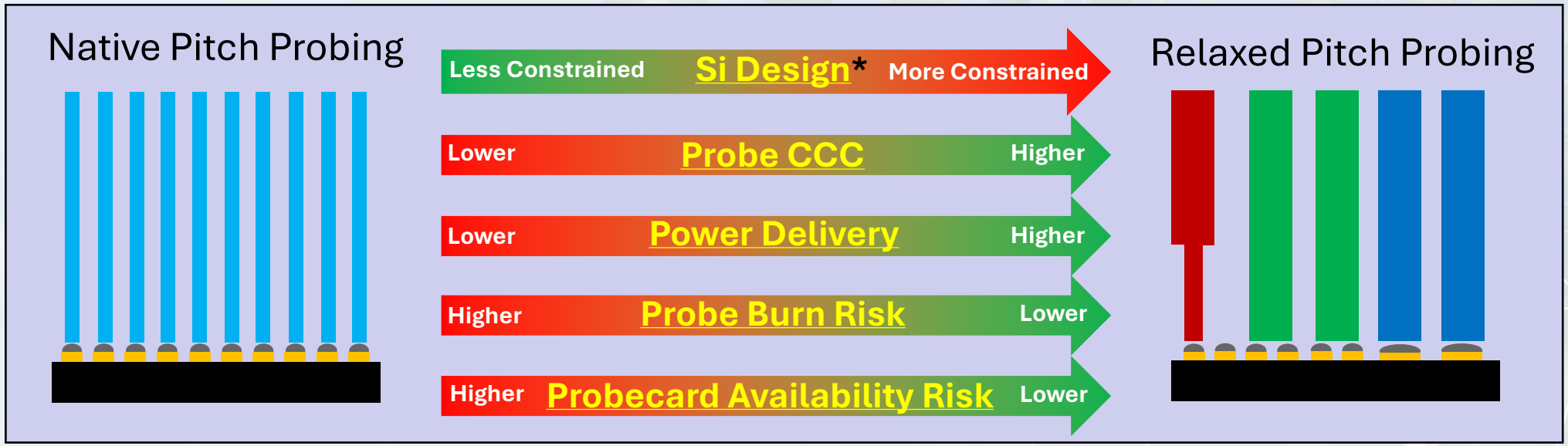
EMIB 2.5D

Embedded Multi-die Interconnect Bridge 2.5D.

- Efficient, cost-effective way to connect multiple complex die.
- 2.5D packaging for logic-logic and logic-high bandwidth memory (HBM).
- EMIB-M features MIM capacitors in the bridge. EMIB-T adds TSVs to the bridge.
- Silicon bridge embedded in package substrate for shoreline-to-shoreline connection.
- EMIB-T can ease the enablement of IP integration from other packaging designs.
- Simplified supply chain and assembly process.
- Production proven: In mass production since 2017 with Intel and external silicon.

General Strategies to Consider

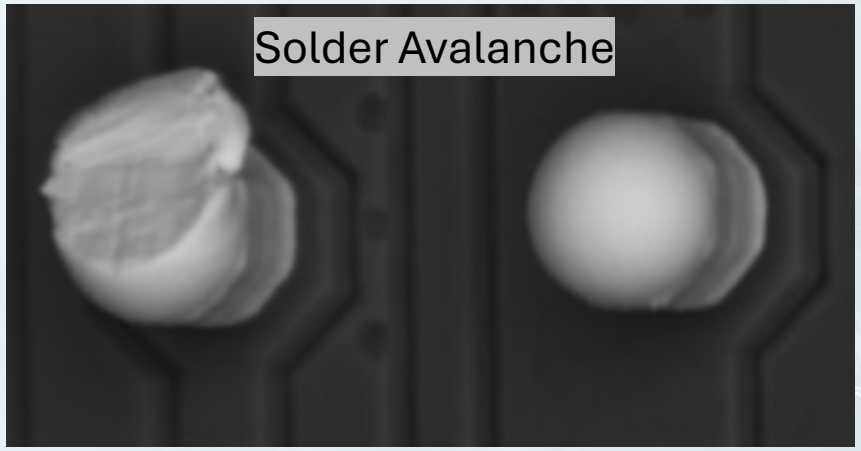
- **Goal to strike balance between**
  - Minimizing design constraints to enable sort/test → **Native pitch probing**
  - Maximizing power delivery at sort, to improve screening efficiency and minimize risks for burns/repairs that lead to probecard availability losses and increase total cost of ownership → **Relaxed pitch probing**

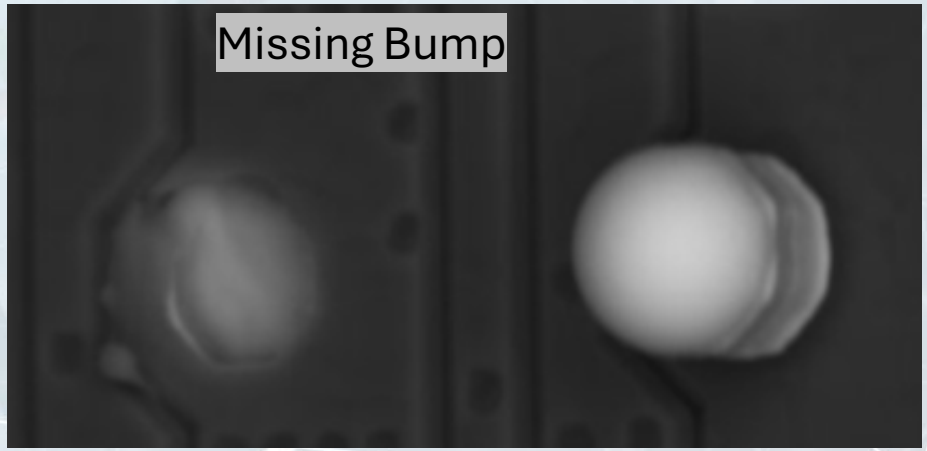


** Upfront planning for bump layout design rules*

Challenges with µBump Probing

- Manage tight radial alignment control across a fleet in mass production
- Stable and uniform electrical contact
- Uniform µBump deformation
- Sort/Probe induced defect modes and yield losses
- Downstream risks at assembly and reliability requiring integrated qual strategies



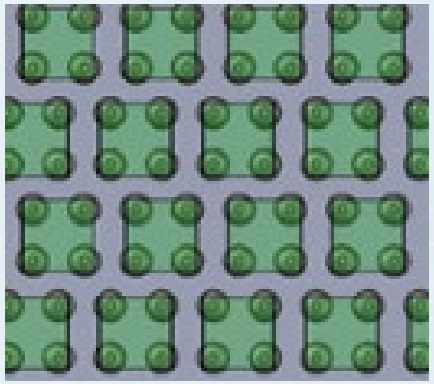


- **Significant and synergized efforts across Intel Foundry and FormFactor, to co-optimize probe architecture and probing process, to enable high-volume manufacturing**

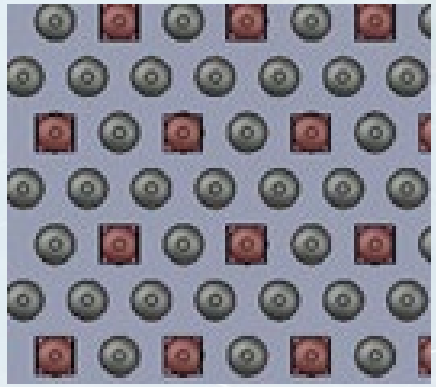
Foveros-S DOW36 vs EMIB Technology

- Foveros DOW36
- Full field µ-bumps
- 18µm CD
- 36µm min bump pitch

Quad clusters (70µm min probe pitch)



Singles (skip-bump, 90µm min probe pitch by rule)

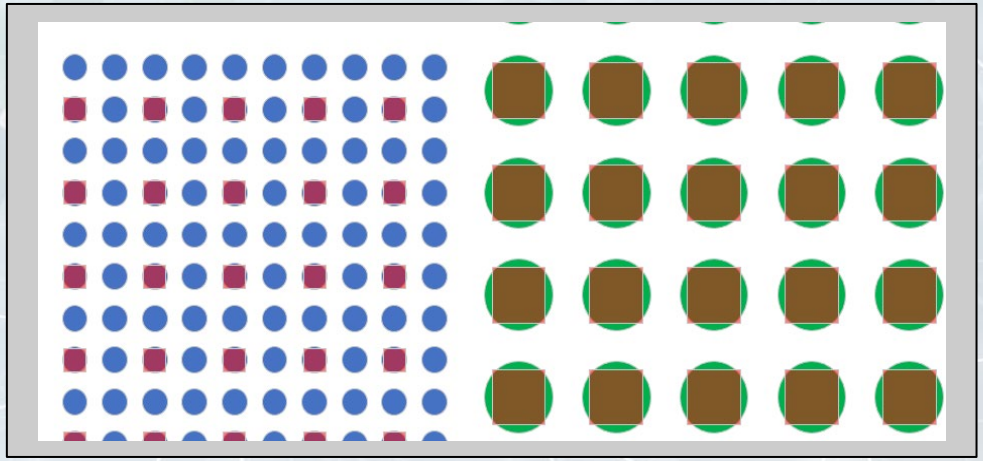


Quad Probing (Intel) – US Patent No. 12,163,982

- EMIB45µm
- Core bumps: 65-70µm CD; 100µm min pitch
- Bridge µ-bumps: 23-28µm CD; 45µm min pitch

µ-bump (skip-bump, 90µm min probe pitch)

Core bump (100µm min probe pitch)



Both architectures require hybrid probe solutions with tight radial alignment control

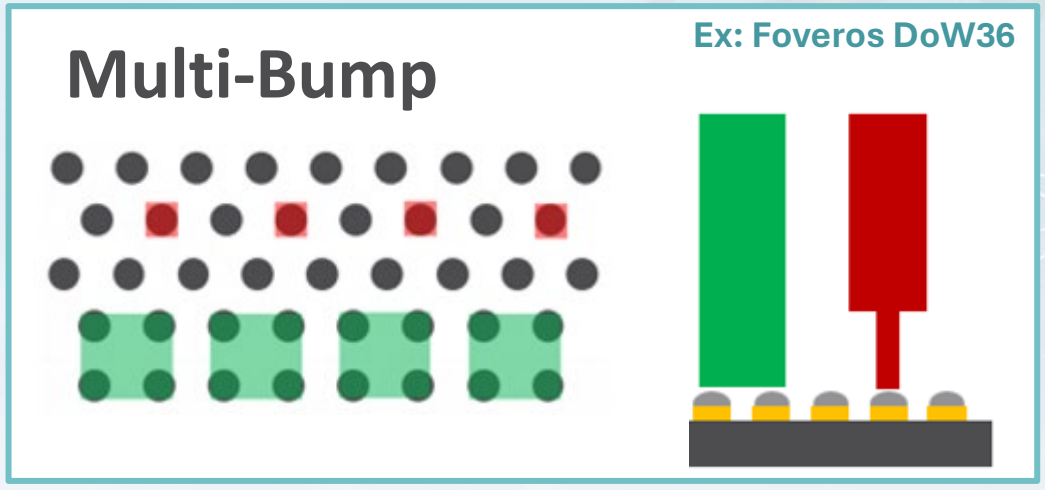
µ-Bump Probing Solutions

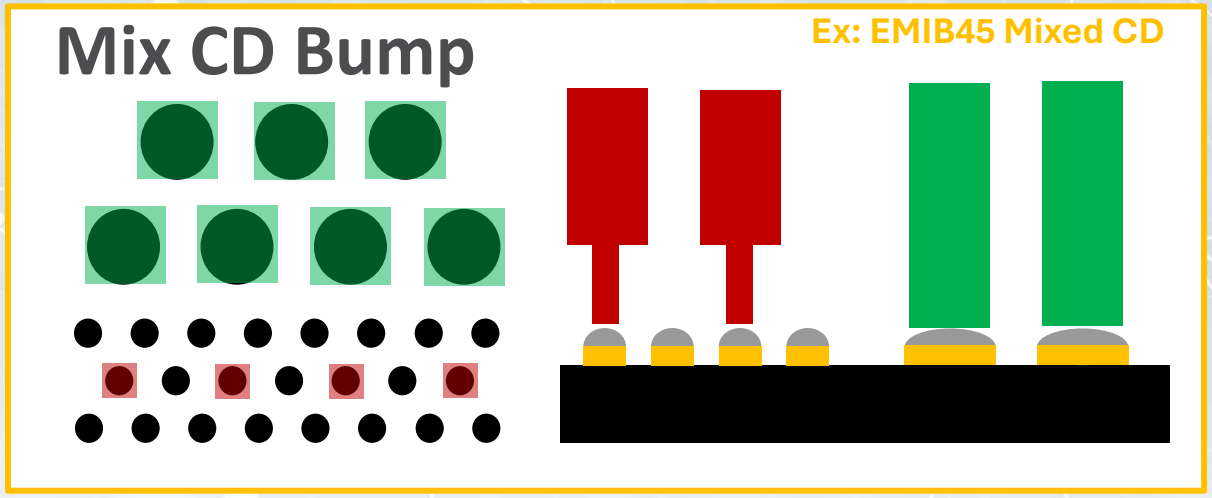
Probe	Min Square Pitch	Tip Size	CCC*	Probe Force	Alignment	Hybrid Option
Single-IO-70	72x62µm	28x28µm	0.6A	0.8gf	≤7 µm (build) ≤10 µm (accept)	Yes
QUAD-70-A	72x67µm	47x47µm	0.7A	1.3gf		
QUAD-70-B				2.7gf		
Bridge-IO	*78x78µm*	*28x28µm*	*1.1A*	*1.3gf*	≤10 µm (accept)	Yes
Core-90	78x78µm	50x56µm	1.3A	2.2gf		
Core-110	78x95µm	50x60µm	1.4A	2.5gf		
Core-140	75x125µm	50x60µm	1.7A	2.7gf		

In Qual

Intel Foundry Data

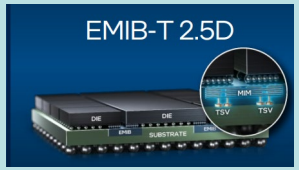
*MeGP is available and increases effective CCC

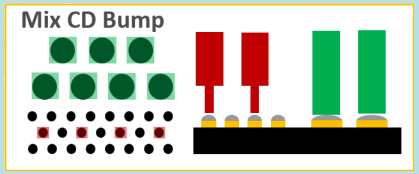




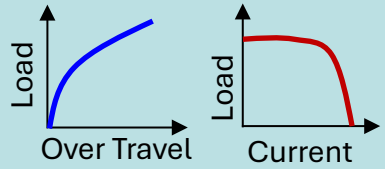
Typical Qualification Plan

Select/develop probe(s) to meet critical sort requirements





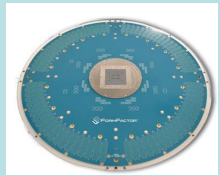
Intel + FFI test coupon characterization → probe finalized



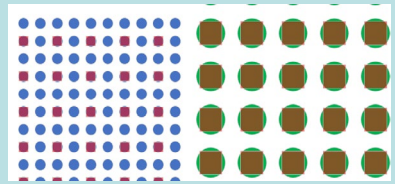
Materials Characterization (SEM, EDS, X-ray)

Build test vehicles (TV) to validate required envelope

TV: Probe card



TV: Si



Assess probing performance at COLD/HOT/MERGED socket

(start at COLD; then switch to HOT for die sort only)

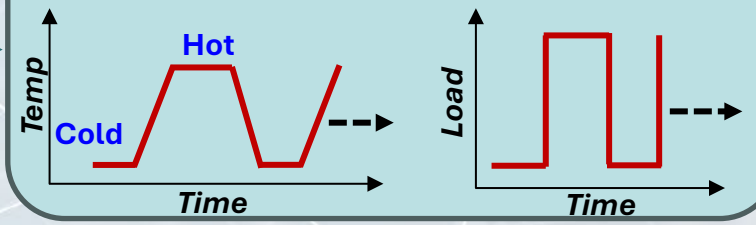
Probe performance validation using baseline recipe for CRES and shorts

Probing Process optimization for high volume readiness

- Clean parameters
- Over-Travel
- Card-to-card variation
- Module to module variation

Iteration, recipe optimization and recipe hardening

Thermomechanical cycling, fatigue test and lifetime

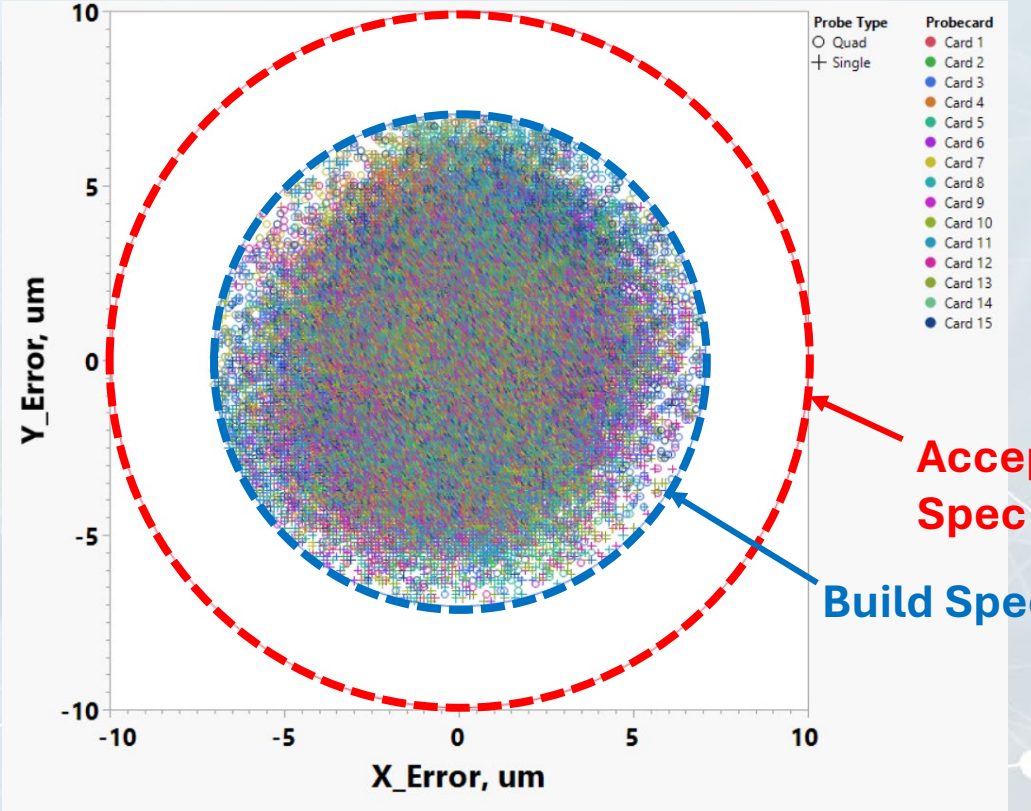


Bump deformation assessments to validate no downstream risks

Saad Ahmed (Intel Foundry), Jeremy Streifer (FormFactor)

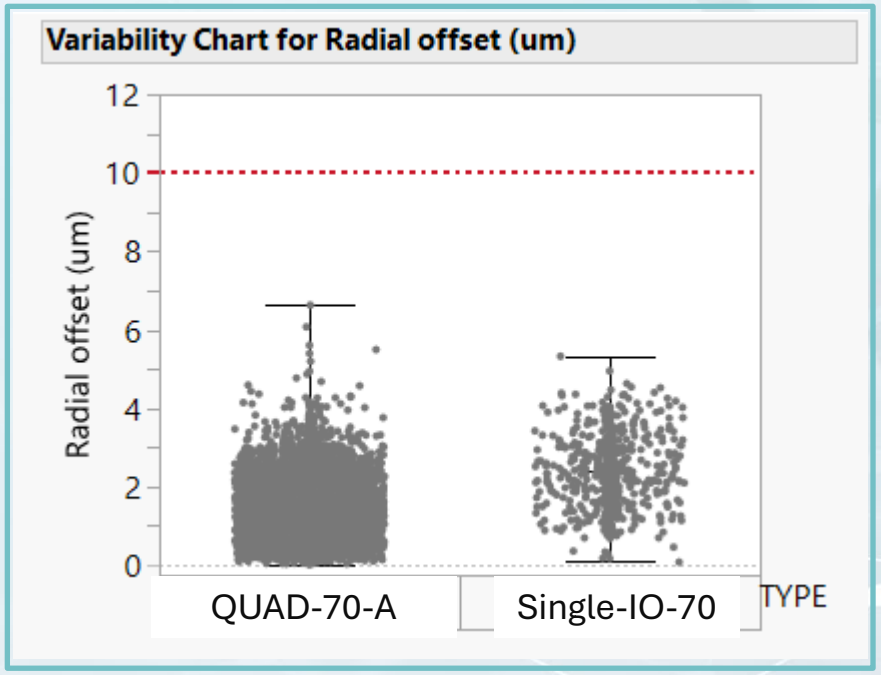
Hybrid Probing Radial Alignment (FFI Outgoing)

- Foveros DOW36 HVM example
- FormFactor outgoing radial alignment from a representative product (Product A)
- 243K springs across 15 cards, including QUAD and Single probe types

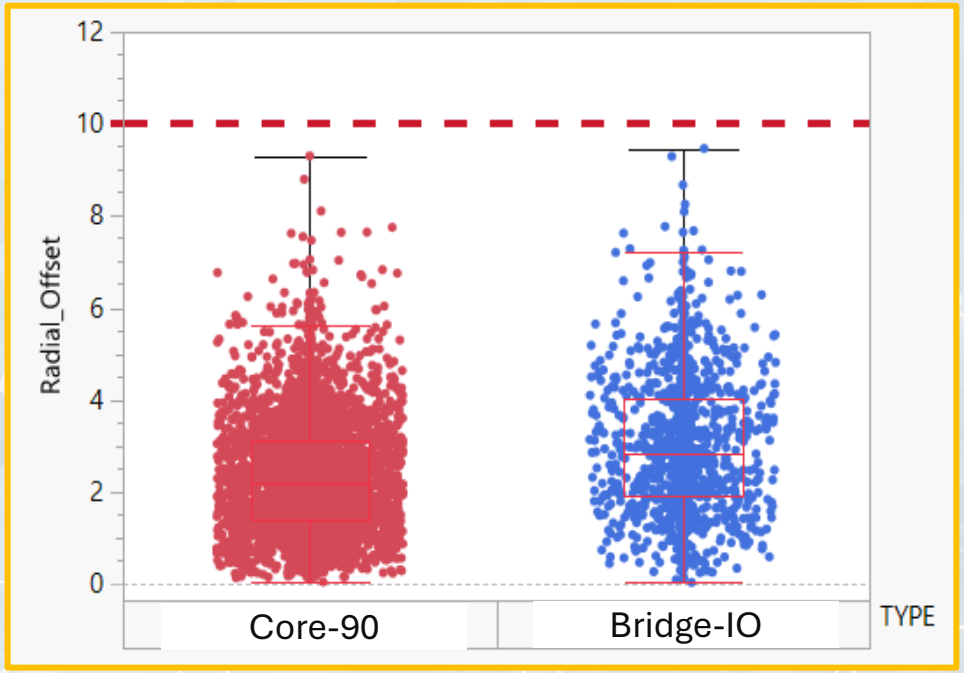


Hybrid Probing Radial Alignment (Intel Foundry Incoming)

Foveros DoW36 – Product B
QUAD-70-A + Single-IO-70 probe alignment
(2 heads, 10k probes)



EMIB45um Mixed Pitch – TV1
Core-90 + Bridge-IO probe alignment
(3 heads, 19k probes, *in development*)



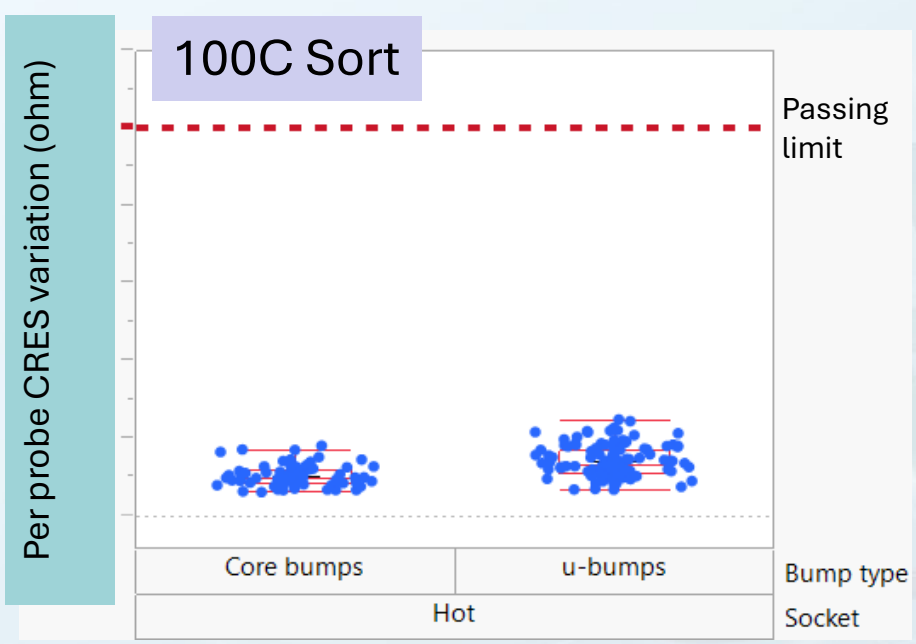
Good radial alignment control demonstrated on many Foveros products in high volume

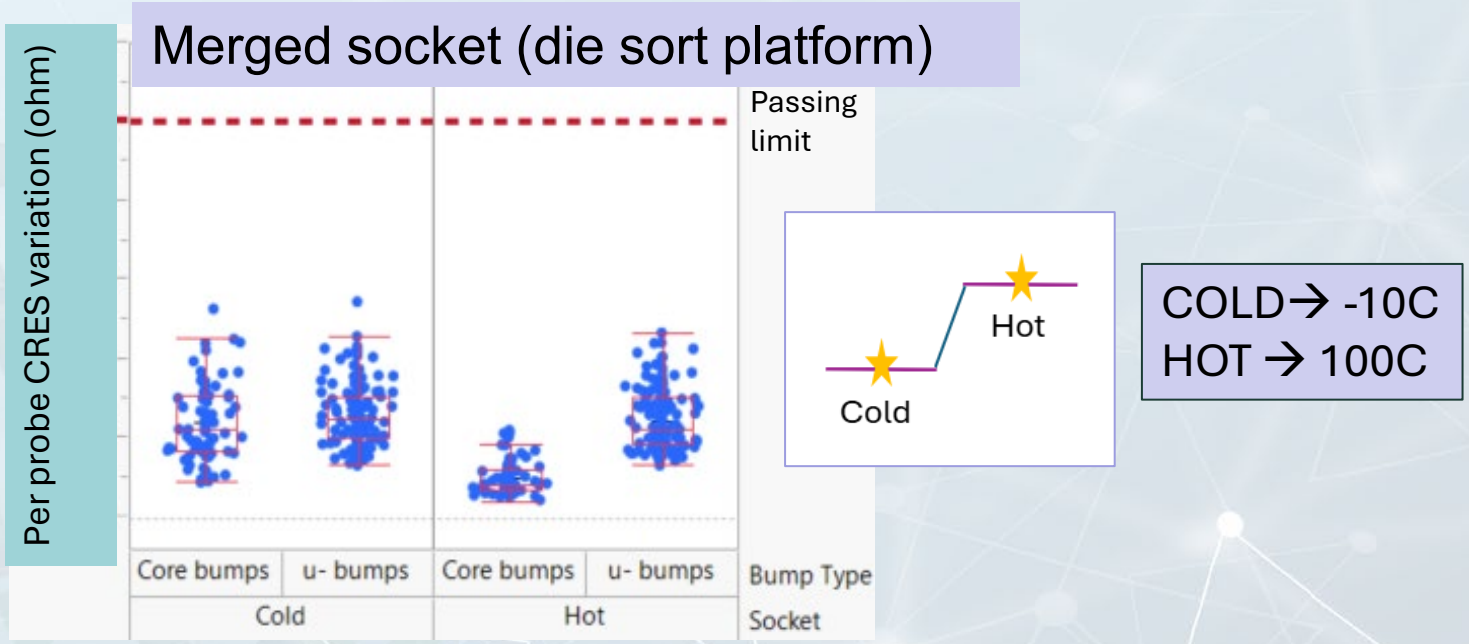
Foveros DOW36 Mass Production Summary vs EMIB Mixed Pitch Probing

	2019 – 2026+	2026 →
Metric	**Foveros DOW36**	**EMIB45 Mixed Pitch Probing**
Bump info	Full field µ-bumps 18µm CD 36µm min pitch	Mixed CD Core bumps: 65-70µm CD; 100µm min pitch Bridge µ-bumps: 23-28µm CD; 45µm min pitch
Probing pitch	Quad clusters (70µm min pitch) Single µBump (90µm min pitch by rule)	Core bumps (100µm min pitch) µ-bumps (90µm min pitch)
Radial Alignment Target	≤10 µm	≤10 µm
Technology Readiness	**In Mass Production since 2019** **Wafer- and Die-Sort**	*Under development* Technology Certification by Q3'26
High Volume Production Experience	**Products: 25+ (multiple sites)** **Wafers: 300K+** **FFI Probe Heads: 1500+**	--
Probe Card Availability	**~ 90% (Average across products)**	--
Probe card Mean Time to Failure (Card returns per 100 wafers)	**1 – 2 for standard probe maintenance** **(Average across products)**	--

Performance on EMIB45 Test Vehicle

- Representative CRES results from EMIB45 Mixed CD TV using hybrid (Core-90+ Bridge-IO) probe card



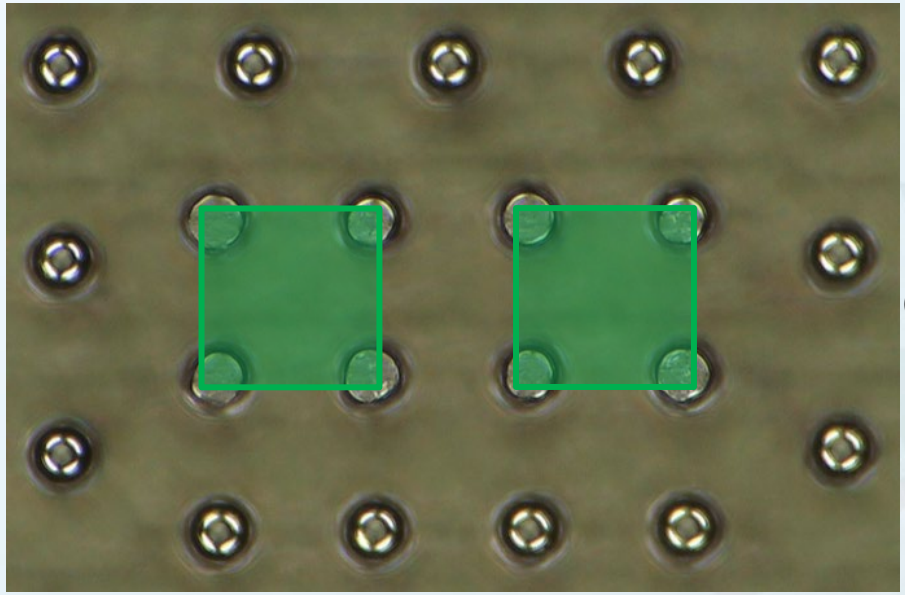


- Methodology:
  - Run wafer(s) multiple times and assess the per-pin CRES stability vs. different process variables (temperature, overtravel, cleaning parameters, etc)
  - Validate no issues with process or probe card induced leakage
  - Freeze the most optimal recipe for mass production

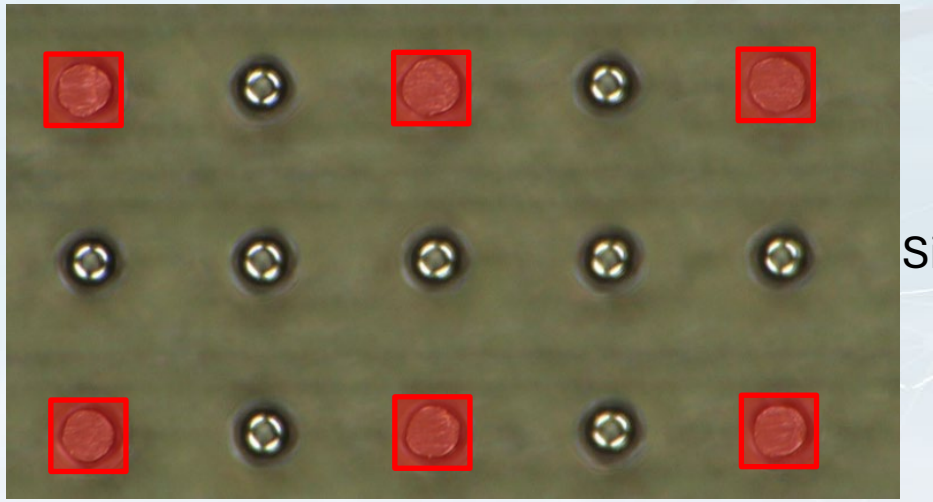
Intel sort performance using FormFactor probes have healthy electrical performance at Cold/Hot & Merged socket test conditions

Bump Deformation Examples

Foveros DoW36

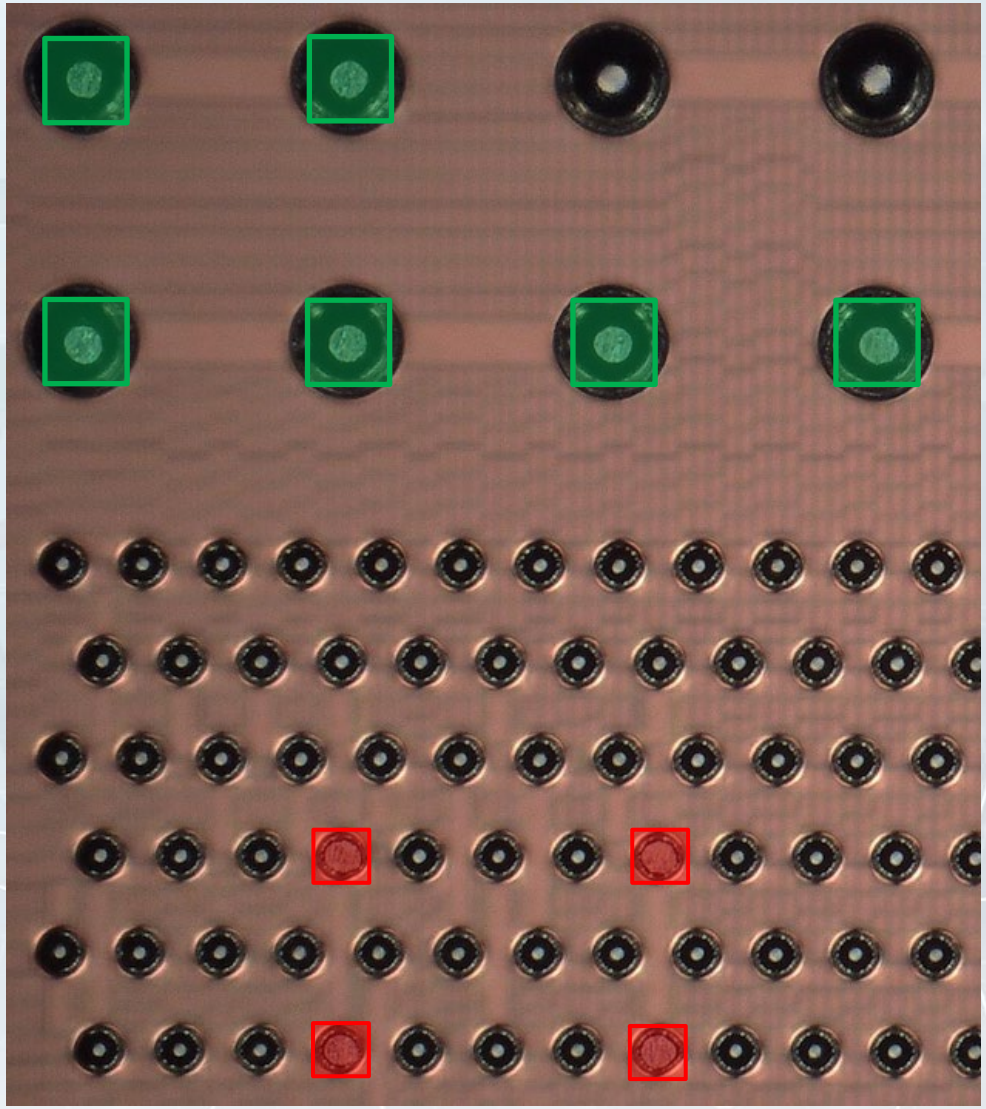


QUAD



Single

EMIB45 Mixed CD



Core

Bridge

Well-centered and symmetric bump contacts with Intel probing process on microbumps

Saad Ahmed (Intel Foundry), Jeremy Streifer (FormFactor)

General Considerations for Overcoming Downstream Risks

- Optimizing probe tip size and force to manage solder bump deformation
- Good radial alignment control to minimize asymmetric bump deformation
- Controlling the maximum die temperature throughout the test
- Optimizing the Test time at HOT
- Managing the number of touchdowns and/or using post sort reflow to preserve the bump coplanarity
- Assembly and reliability DOEs to quantify safe envelope

Summary and Future Outlook

- Intel Foundry has significant µ-bump probing experience that is well established in mass production across multiple sort platforms and factories
- FormFactor is a worldwide leader in probecard supply enabling high volume test on µ-bump interfaces
- The teams are leveraging proven expertise and Foveros DOW36 HVM experience to develop µ-bump capable sort solutions for EMIB-T advanced packaging
- Collaboration as demonstrated here keeps probe technology and packaging developments aligned, helping identify and address probing challenges before they impact yield

Acknowledgements and Questions

- Thank you to Intel Foundry and FormFactor colleagues for all of your contributions

- Questions?