SWTEST 2026 CONFERENCE

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A New 300mm Vertical Probing Solution Enabling Automotive Microcontroller High Volume Manufacturing and Test

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Outline

1. **Introduction**
   - Motivation and scope of the presentation
2. **Device**
   - Characteristics
3. **How to Test the Device: 300mm Probe Card**
   - 300mm vertical probe card architecture & thermal management
   - Vertical probes technology
   - Testing & certification
4. **Probe Card Characterization and Qualification Process**
   - Probing technology validation
   - Qualification process & results
5. **Conclusions and Future Developments**

Introduction

Infineon automotive Microcontroller Unit (MCU) demand:

- **High reliability** on very low ppm-rate to provide **high quality products**
- **High coverage functionality** and **stability** over a **wide temperature** range
- Continuous **test cost reduction**
  - Improved TD-efficiency
  - Reduced test-induced yield loss (TIYL)

Technoprobe probe card solution:

- **High-parallelism** wafer probing over a **wide temperature range**
- **Thermal stability, scrub mark control** and **reduced pad damage**

300mm Vertical Probe Card

Product Requirements

Parameter	Value
Total Probe Count:	30+K
Min Wafer Pad Pitch:	> 100µm
Minimum Pad Size:	60µm x 75µm
Pad Material:	Cu
Test Temperature Range:	- 40°C up to + 150°C
Probe Technology:	Vertical buckling beam
Max Number of Tester Sites:	192
Number of Used Sites:	Up to 190
TDs/wfr for Tester Config:	8
TD-Efficiency:	93.9%

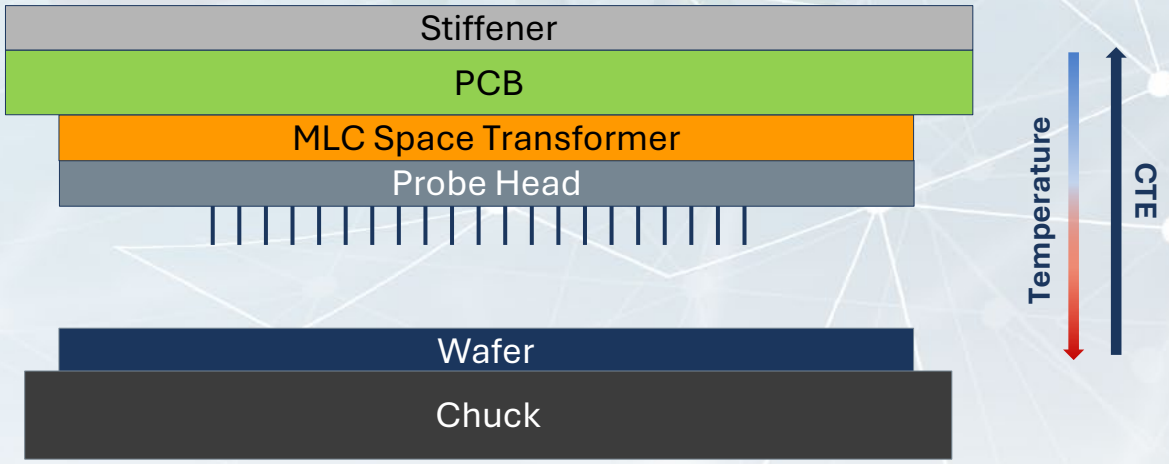
300mm Vertical Probe Card

Key Elements:

1. Customized **Probe Card Architecture** & **Materials Selection**
   - Monolithic MLC (Multi-Layer Ceramic) Space Transformer & optimized Probe Head Plate CTE

2. **“D-MANTIS” Probe Technology**
   - Controlled scrub marks and performance over wide temperature range

3. Dedicated internally-developed **Certification Environment & Probe Card Analyzer**

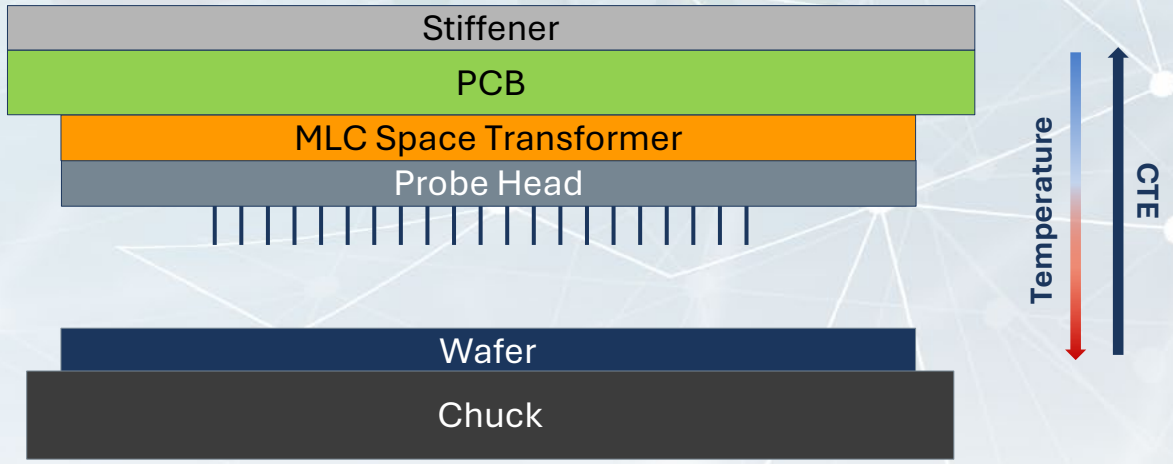


Thermal Management

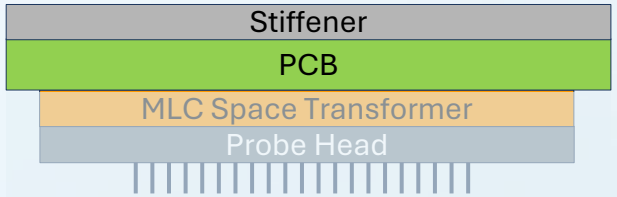
Key Challenges:

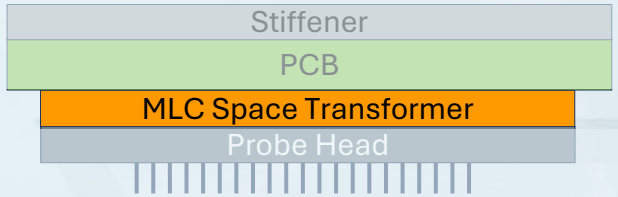
- **Probe to pad alignment for wide temperature** and **large arrays** is critical (see ref. 1)
- Case Study:
  - Working temperature range: **-40°C to +150°C**
  - **Wafer level burn-in included**
  - **PH array: 300mm**

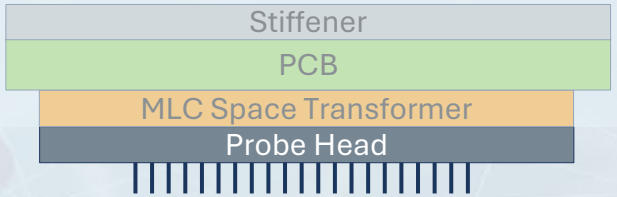
Thermal Management of the Probe Card is essential



Probe Card Architecture

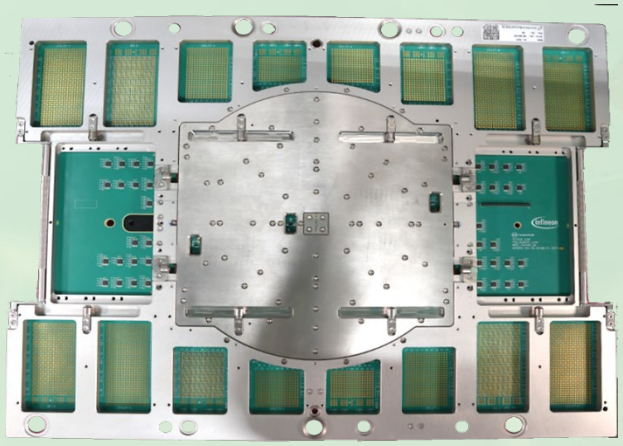






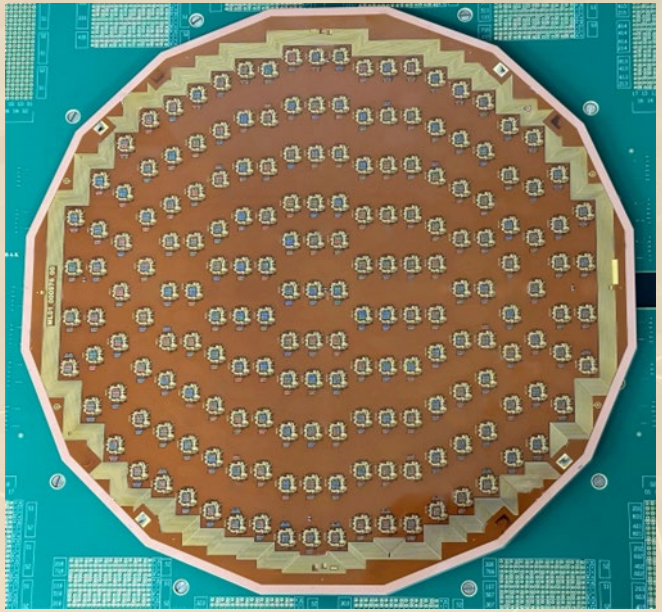
PCB

- **Mechanical Stiffener** materials optimized for CTE matching



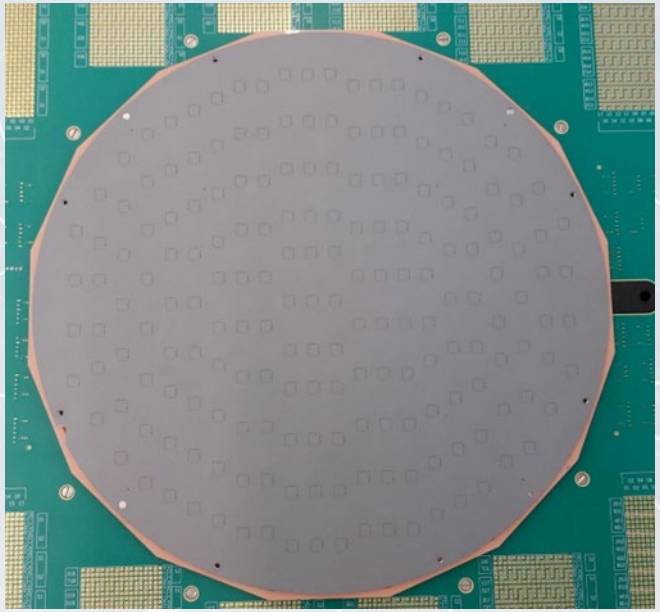
MLC Space Transformer

- **M**ulti-**L**ayer **C**eramic
- **Monolithic 300mm** substrate



PROBE HEAD

- Optimized guide plate CTE
- **Monolithic 300mm** Probe Head



D-MANTIS Probe Technology

- **D-MANTIS** is a new family of vertical probes designed by Technoprobe for 300mm vertical applications

- **AD2** probes are part of the D-MANTIS family: table and next slide refer to AD2 that have been applied in IFX MCU applications

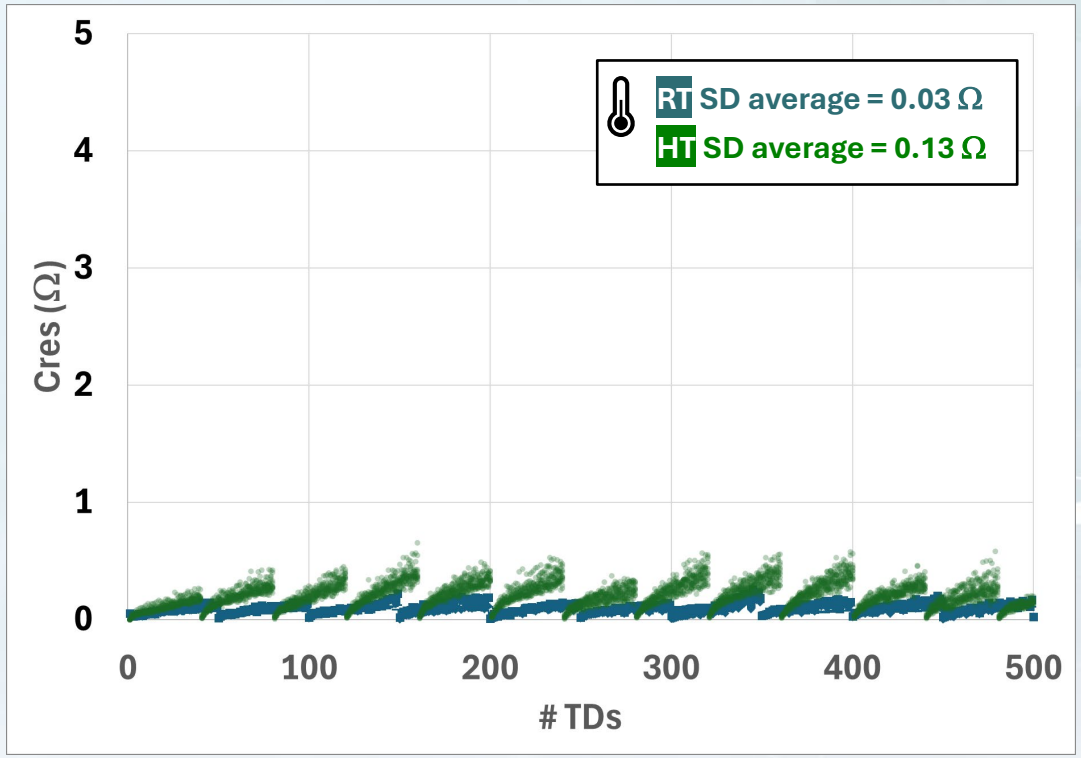
- **AD2** provides **high-parallelism solutions** for large and complex arrays with **wide temperature ranges**

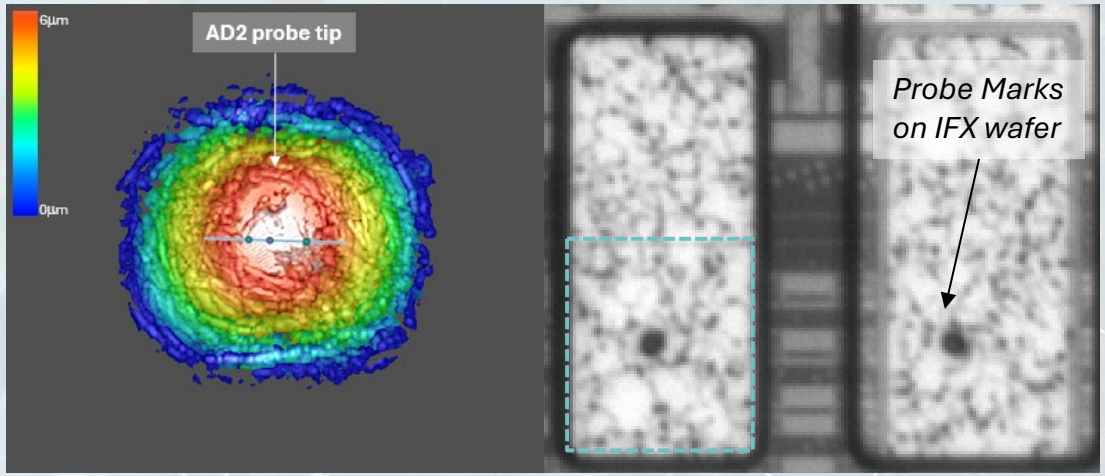
PARAMETER	AD2
Probe Alloy	ASA7 + hard tip
Min Pitch	60 µm
Temperature Range	- 45°C / + 175°C
Pin Current (CCC)	900 mA
Force (AOT 80µm)	2.7 g

D-MANTIS Probe Technology: AD2

- **AD2** minimizes contact resistance (Cres), ensuring optimal performance at low/high temperatures (-45°C to +175°C)

C-Res on Al





AD2 probe confocal profile & probe marks

Probe Card Certification

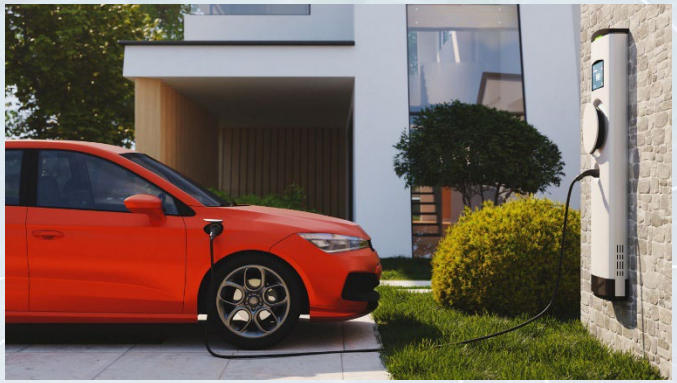
- Technoprobe has **developed a Probe Card Analyzer** (ATHENA) to fully test **300mm Probe Cards** (see ref. 2)

- **100%** Optical & Electrical **Test Coverage**
  - **Optical** X, Y, Z measurements
  - **Cres**
  - **Leakage**
  - **Components**
  - **Loopbacks** through independent probes

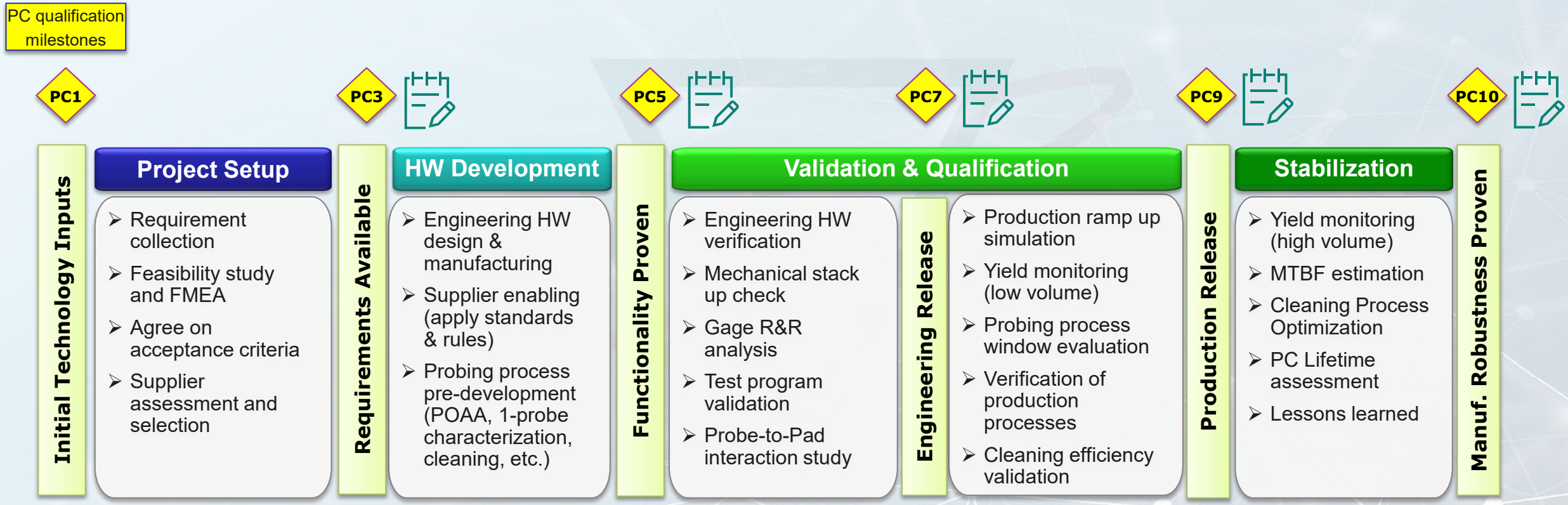
Infineon AURIX™ Microcontrollers

- The Infineon AURIX™ range is a landmark microcontroller, defining years of cutting-edge MCU developments
  - It entered the market in 2012, evolving on previous TriCore™ MCUs like the AUDO (AUtomotive unifieD processOr) range
  - AURIX™ has undergone several upgrades since

- Applications
  - Safety & Security
  - Connectivity
  - Electric Vehicles



Infineon Probe Technology Qualification



Milestone approval and sign off by PJM, probing experts, technology development, test engineers, test operations and quality management

PoAA Robustness and Pad Imprint Study

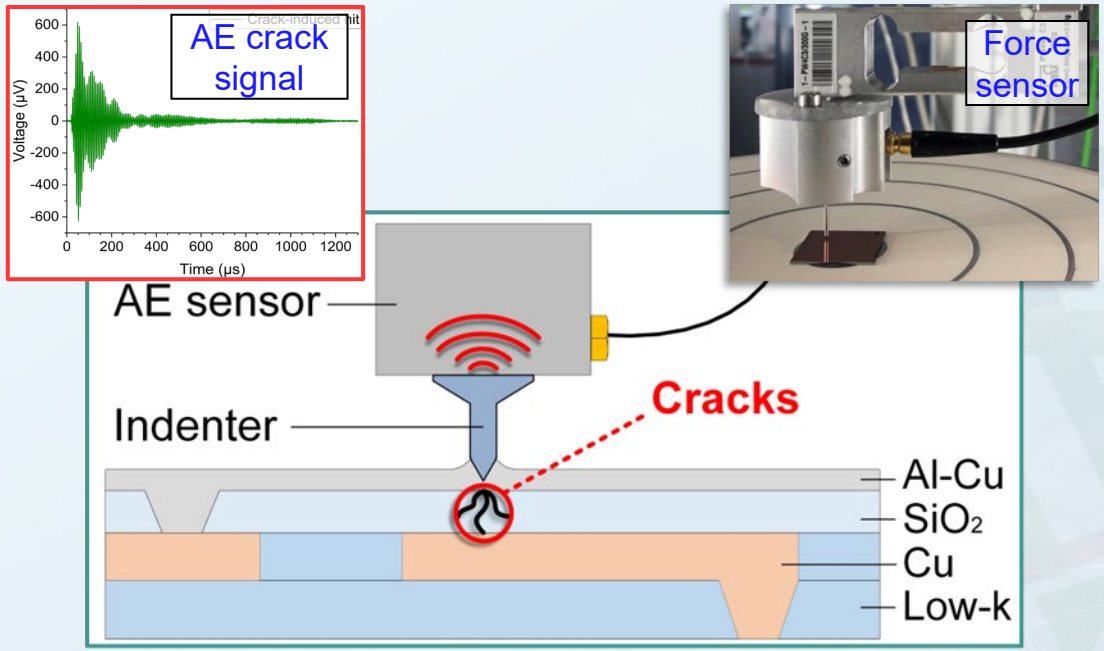
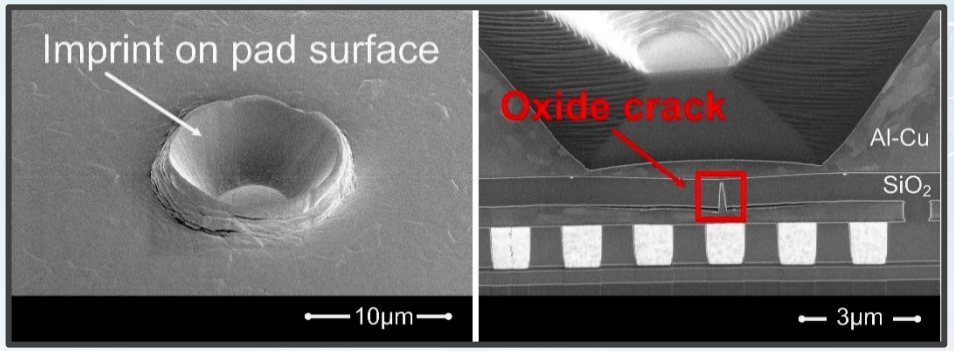


Fig. 1: Acoustic Emission (AE) Test Method for POAA crack risk assessment, see ref. 3 (presented at SW Test 2022)



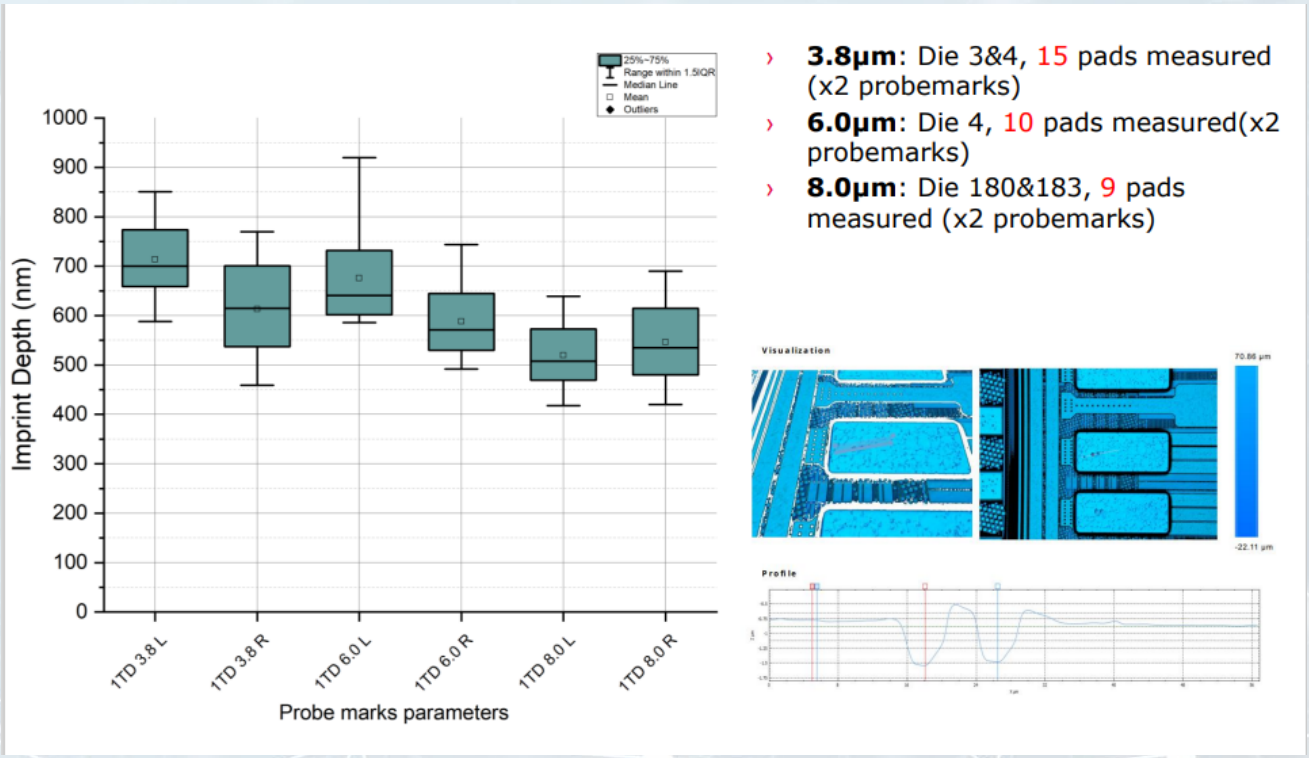


Fig. 2: Optical inspection of probe mark depth for different probe tip diameters

PoAA = Probe over Active Area

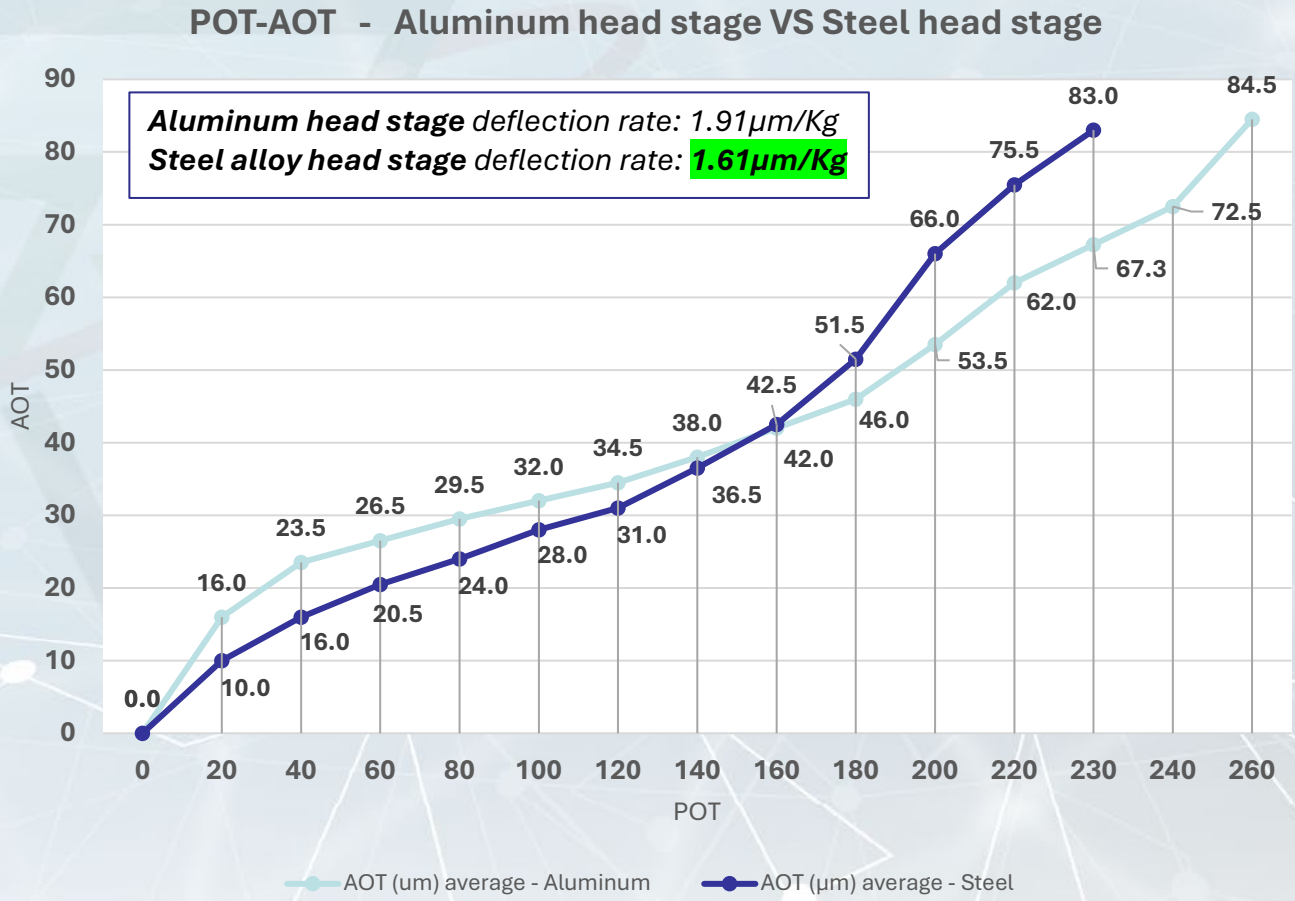
Planarity POT vs AOT Analysis

High total contact force requires POT vs AOT analysis:

- Based on headplate material
- PC-Stiffener construction
- Single probe Gram Force
- Total probe count

Important parameters:

- Deflection rate of headplate (aluminum vs steel)
- POT vs AOT = <1



POT = Programmed Over Travel
AOT = Actual Over Travel

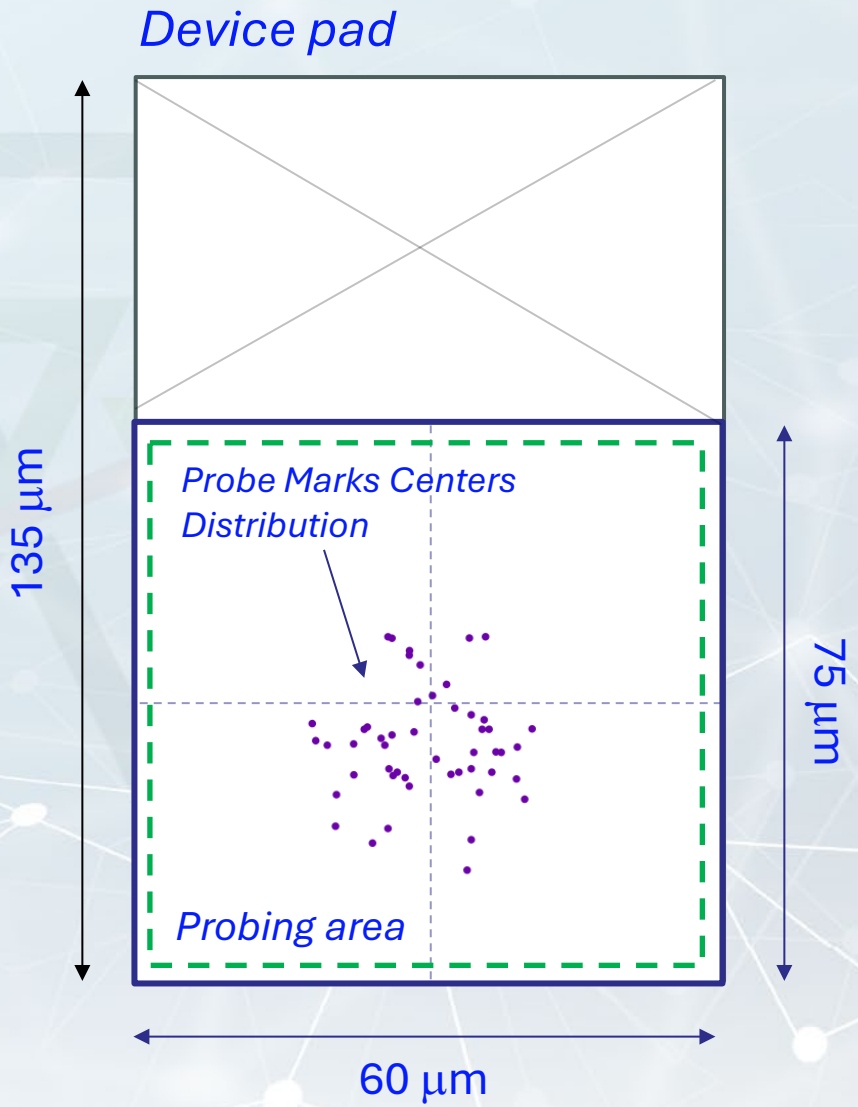
Probe Mark Position Analysis

Probe marks have to ensure a safe position on the pad:

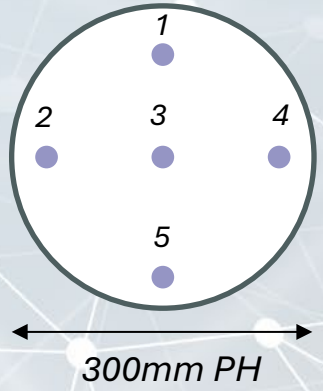
- Full temperature range
- All probes
- Full 300mm array
- Pad size minus safety keepout

Important parameters:

- Wafer CTE
- Ceramic CTE
- PC architecture
- Tip diameter control
- Balanced soak procedure



Probe Marks taken in 5 areas distributed along the 300mm array



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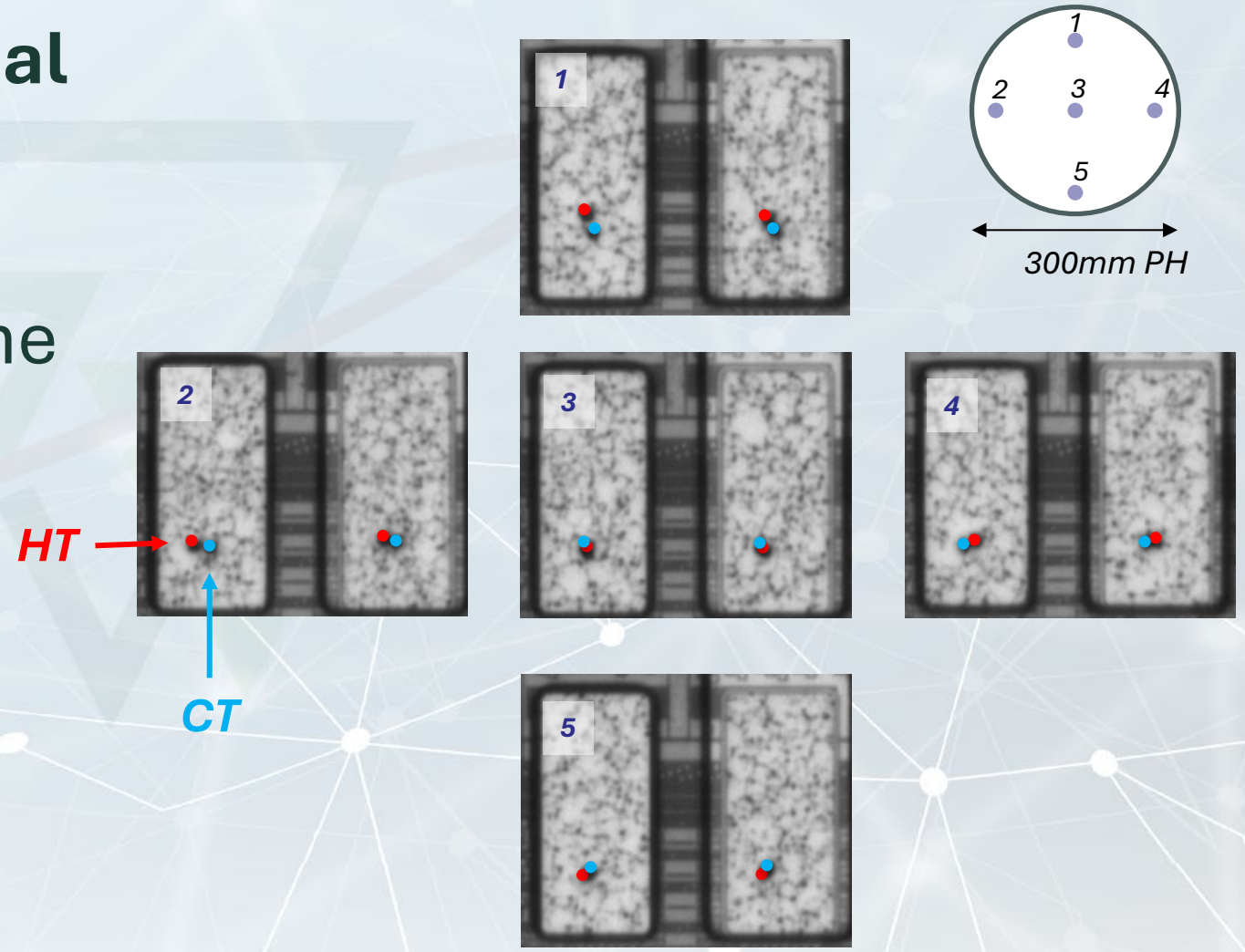
Probe Mark Position Results

- **PC architecture and thermal management** ensure good PM positioning in the whole temperature range across the entire wafer array
- **No soak time** is needed **between** consecutively tested wafers and **after online cleaning**



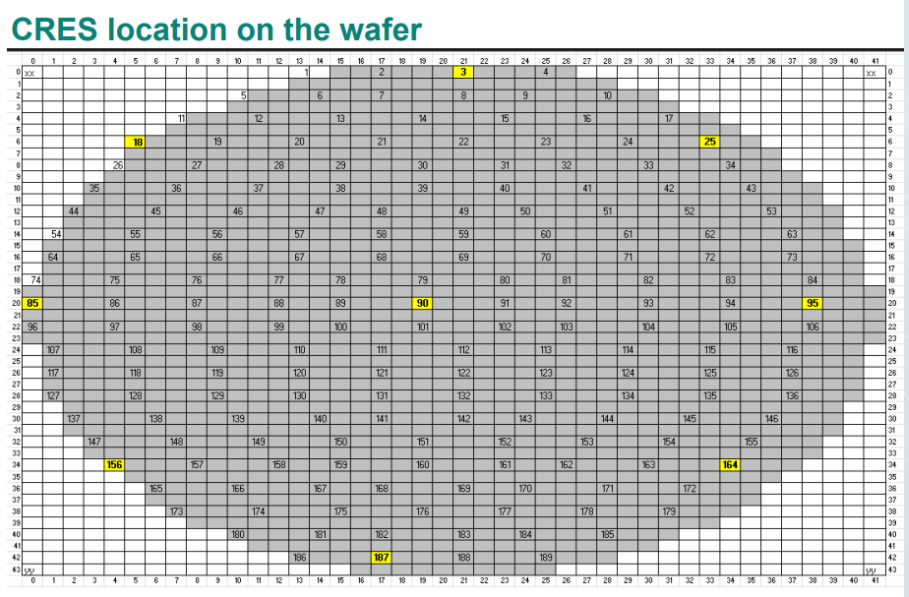
CRes Monitoring

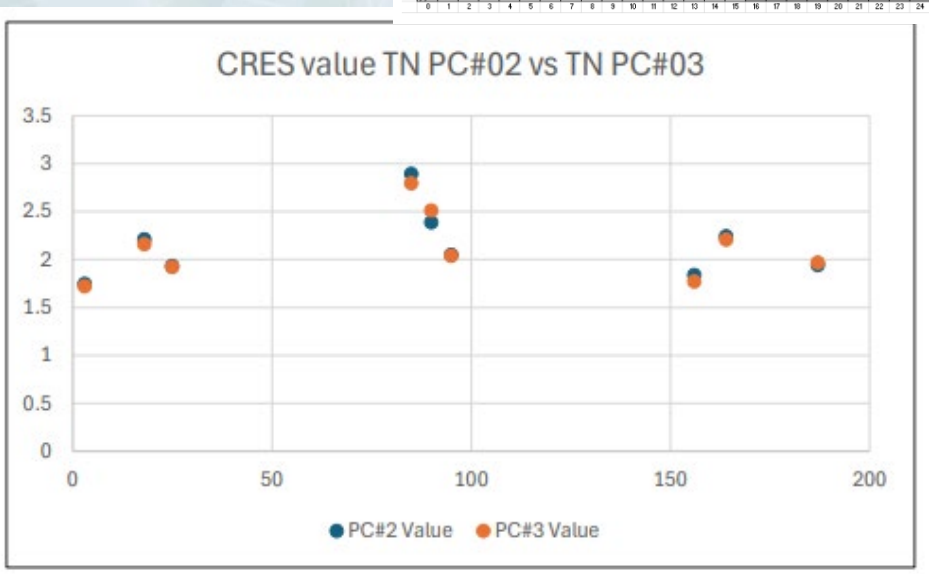
9 selected site were designed for CRes measurement (full path resistance at contact):

- $R_{meas} = R_{needle} + R_{trace} + R_{contact}$
- CRes is derived from R_{meas}

Important parameters:

- Stability over full array
- Stability during lot test

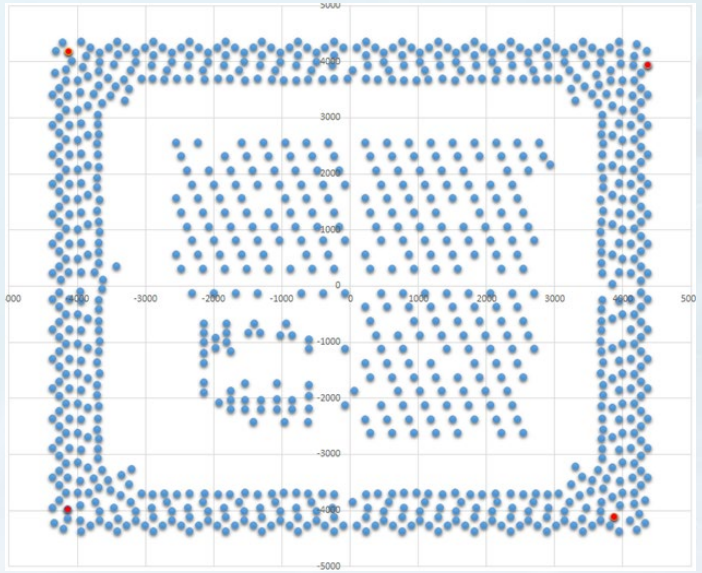




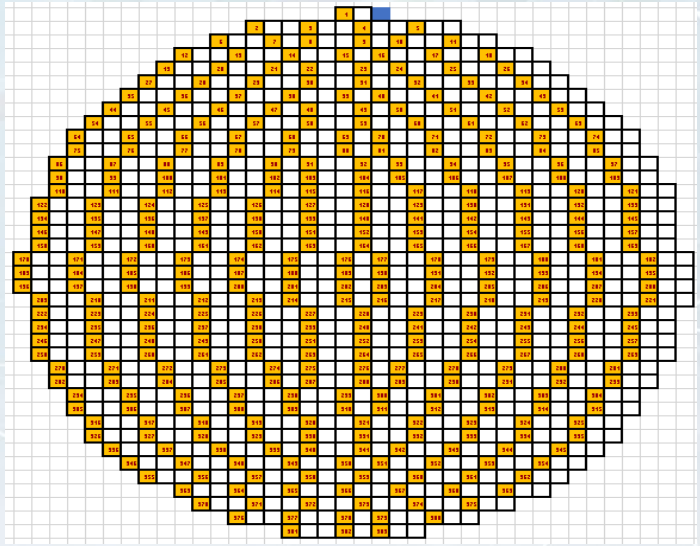
Conclusions

- Technoprobe **new 300 mm Vertical PC solution** has been successfully **qualified** on IFX leading edge, AURIX™ Automotive MCUs
- **Technoprobe vertical technology 300mm probe card advantages**

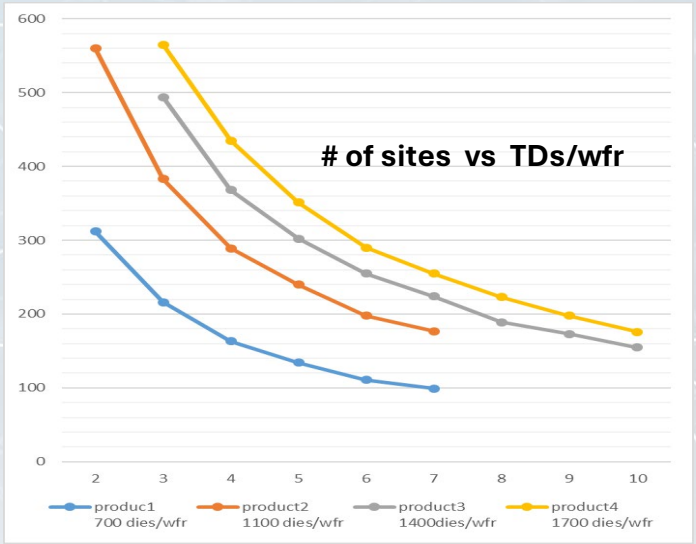
Complex Pad Layouts



High Parallelism



Minimizes TD per wafer



Next Steps

- Roll out the **300mm vertical probe cards** to products with **complex pad distribution**
- **Further reduction of TD's per wafer** is planned by means of increasing the number of sites

Acknowledgements

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- *Tang Dave*
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Technoprobe Team

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- *Greg Medrick*
- *Massimiliano Mosconi*
- *Frank Chen*

References

- *[1]: S. Usai, E. Bertarelli: ““A new generation Probe Card Analyzer for large area and high load devices”, SW Test 2021, Carlsbad*
- *[2]: L. Milazzo, F. Tresoldi, F. Mariani, A. Rinaldi, G. Gedler, D. Appello: “A new generation Probe Card Analyzer for large area and high load devices”, SW Test 2025, Carlsbad*
- *[3]: Dr. O. Nagler, Dr. M. Unterreitmeier: “An Advanced Method for Pad Stack Crack Assessment during Probe-Over-Active-Area”, SW Test 2022, Carlsbad*

Q&A