Automatic Probe Mark Inspection

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Probe Mark Inspection

Problem statement

Electrical test shows good die—
but passivation has been broken

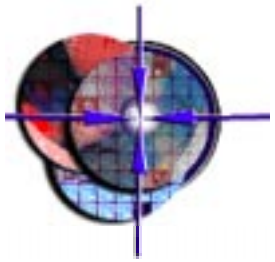
Poor yield due to:

- probe card error
- prober error
- setup error

Probe Mark Inspection

What is PMI?

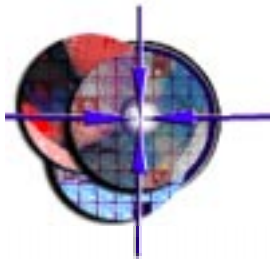
- Visual inspection of probe marks
- Passivation— make sure marks do not touch the glass



Probe Mark Inspection

Why is PMI necessary?

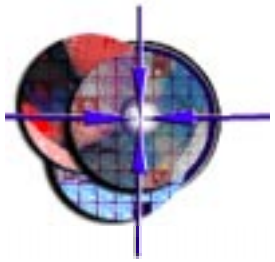
- **Older probers are not accurate enough for new technologies**
- **Manual PTPA (Probe To Pad Alignment) is not optimal (operator setup issue)**
- **Probe cards**
  - — quality
  - — over use



Probe Mark Inspection

Typical PMI process

- **Operator stops auto-probe to inspect first touch down**
  - — Verify Probe to Pad Alignment quality
- **Prober pauses on every nth wafer for manual probe mark inspection**
- **After probing, an offline inspection station inspects probe marks**

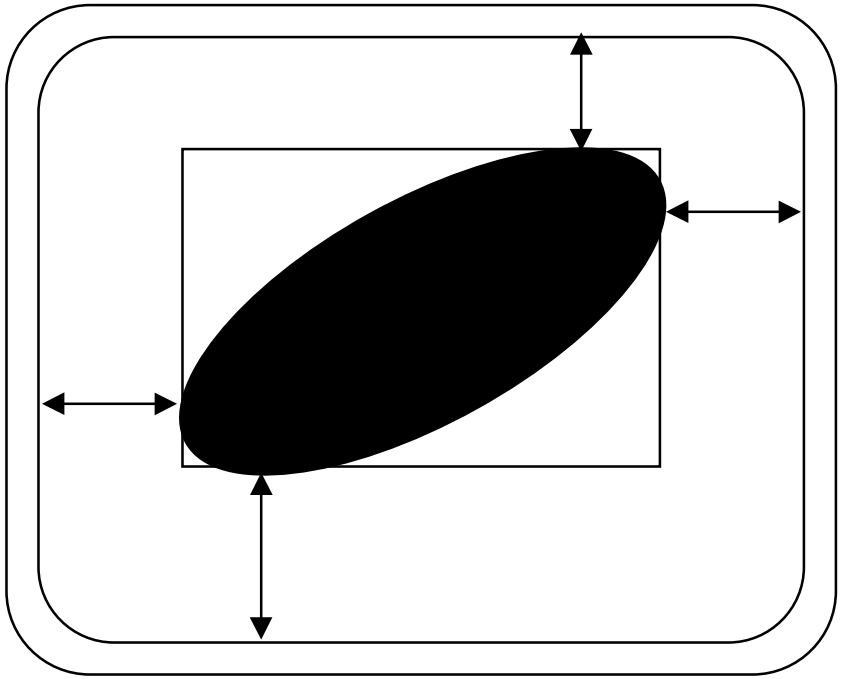


Probe Mark Inspection

- **Advanced Probe Mark Inspection**
- **Fully automatic**
- **Standard vision algorithm for inspection**
- **PMI checks**
  - — drift
  - — mark size
  - — proximity to edge
- **Benefits**
  - — eliminates operator intervention
  - — optimizes probe to pad alignment
  - — post probe process control

Probe Mark Inspection

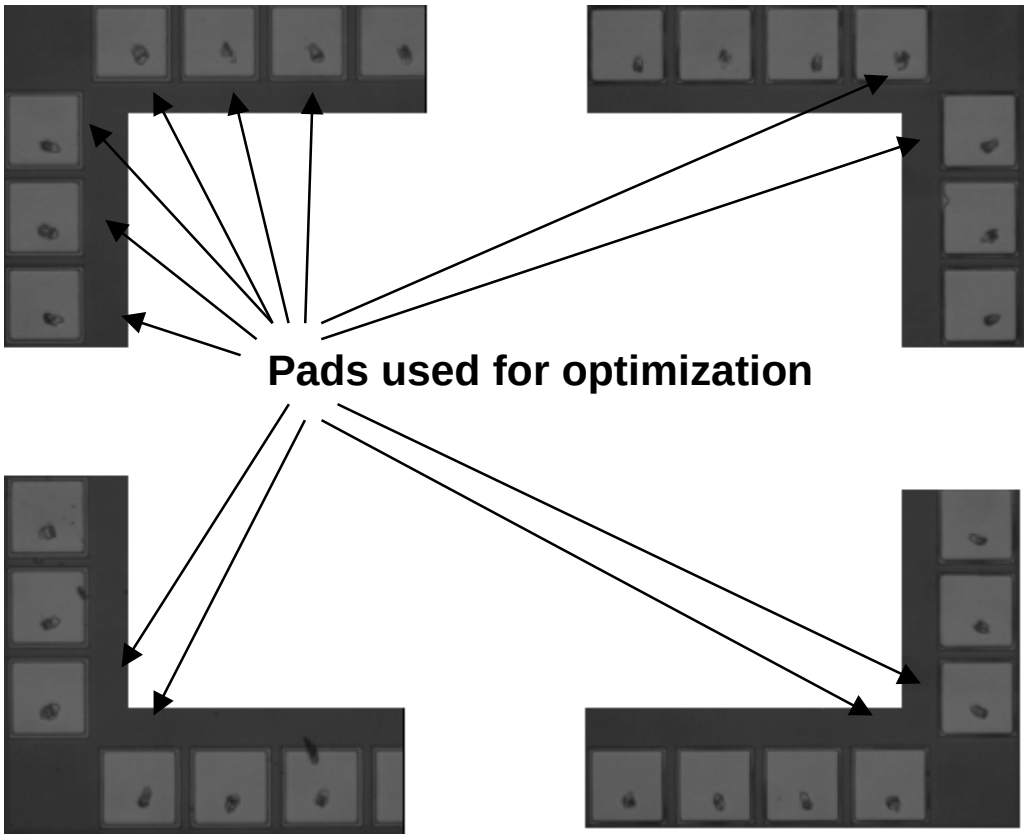
Probe to Pad Optimization (PTPO)



Based on distances from mark boundaries to pad boundaries, we optimize mark placement by maximizing the minimum

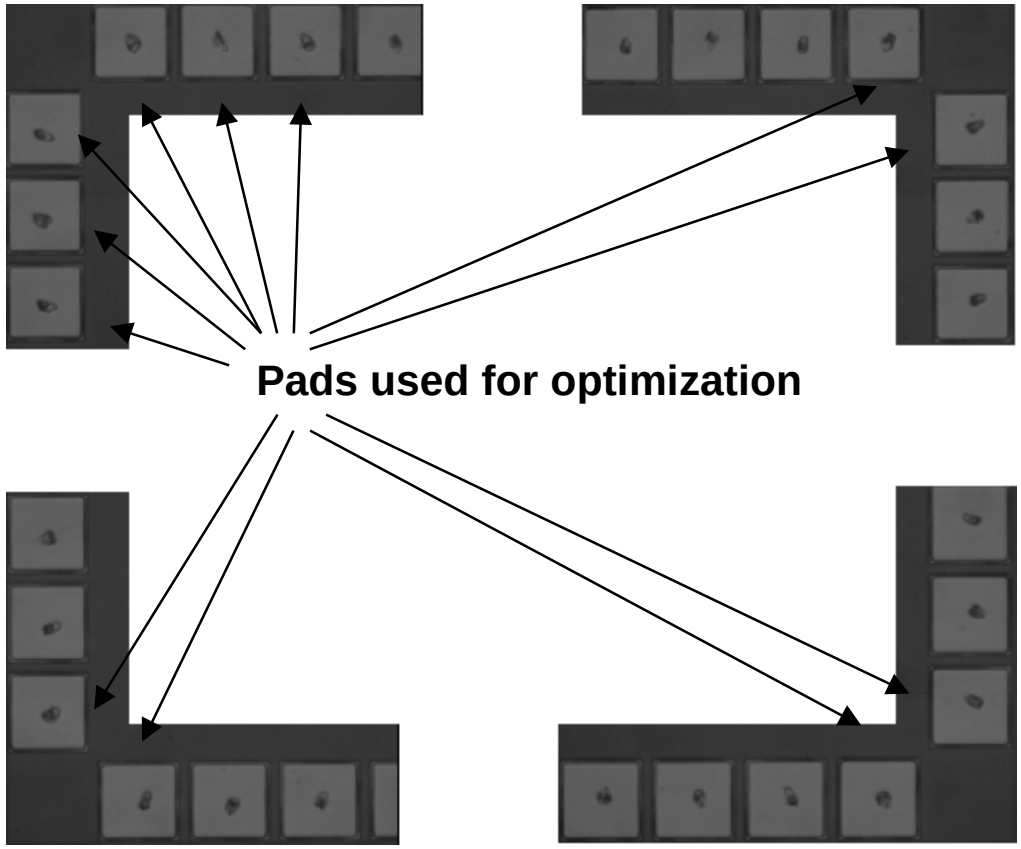
Probe Mark Inspection

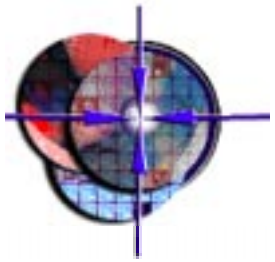
Example of marks pre PTPO



Probe Mark Inspection

Example of marks post PTPO





Probe Mark Inspection

PTPO continued...

- **True close loop feedback**
- **Process monitor**
- **Eliminate operator subjectivity**

Probe Mark Inspection

Sample recipes: #1

‘APTPA
load
profile
AA
probe
PMI on 4 pads on every 50th TD (Touch Down) of every 5th wafer’

Checks for drift

Time added : negligible

Probe Mark Inspection

Sample recipes: # 2

‘APTPA

Load

Profile

AA

Probe

Unload

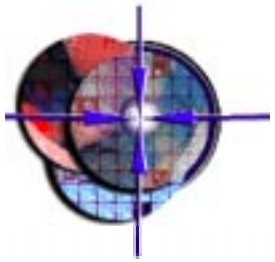
PTPO on first TD of all other wafers

PMI on 4 pads on every 50th TD of all other wafers’

‘Close loop’ process control

Checks for drifts

Time added = 24 minutes



Probe Mark Inspection

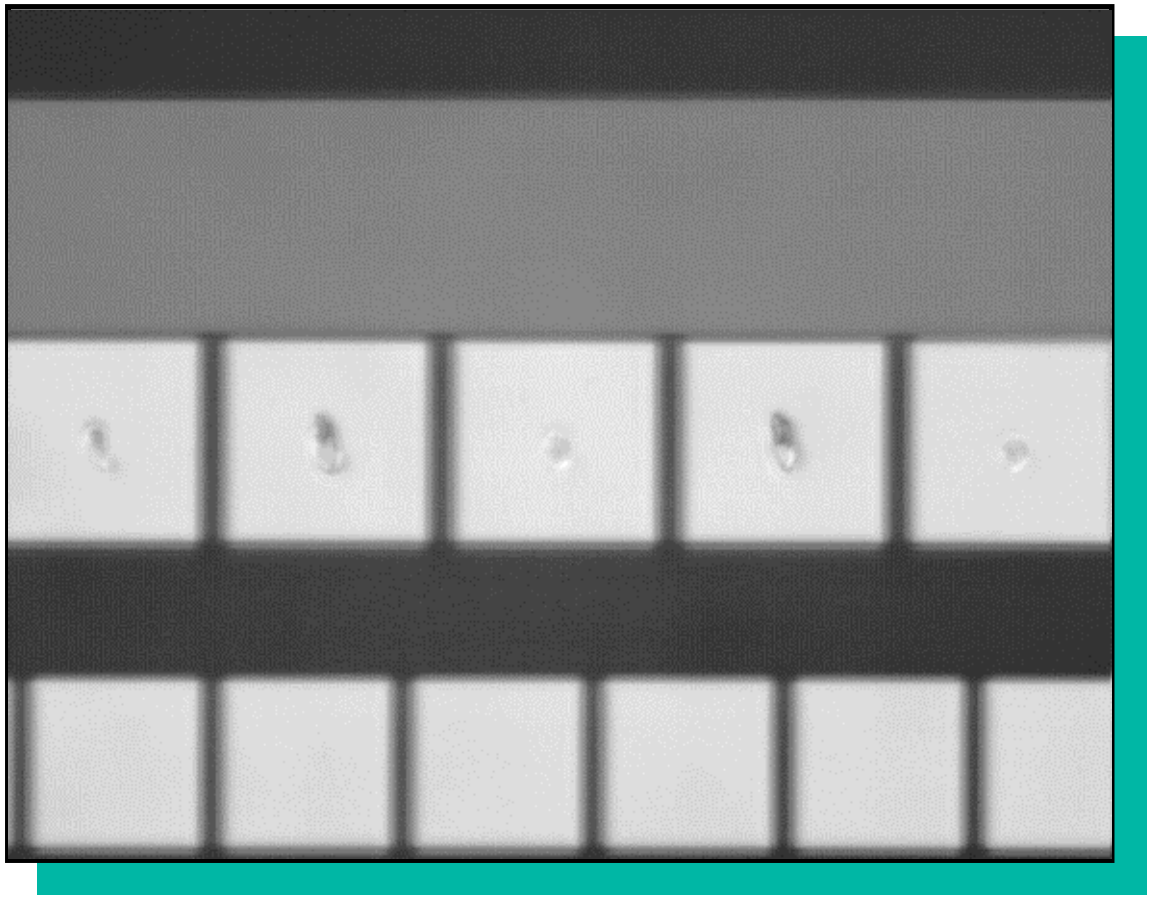
Post probe process control

- **Dedicated prober for PMI**
- **Integrate into the Inspection station**
- **Collect probe mark data to check:**
  - die to die stepping error
  - wafer to wafer alignment error
  - setup to setup variation
  - probe card wear characteristic
  - frequency to clean and repair probe card

Probe Mark Inspection

Challenges

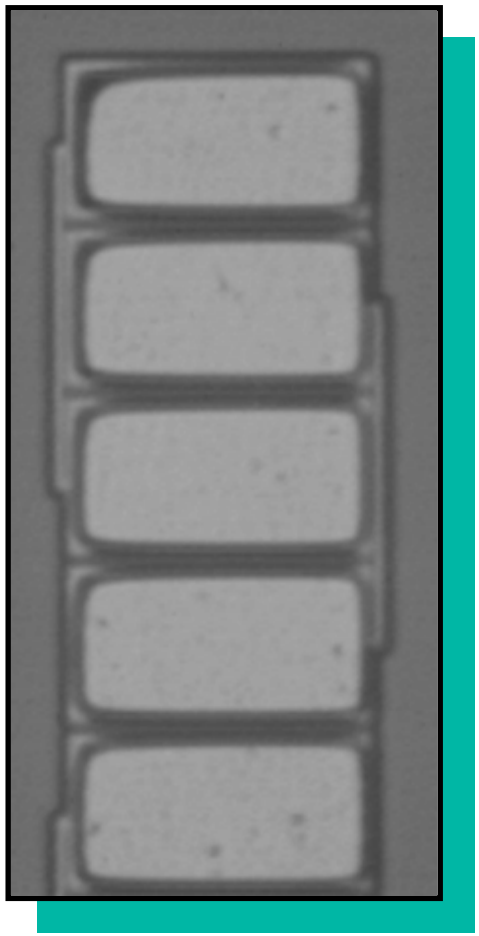
Bright marks



Probe Mark Inspection

More challenges

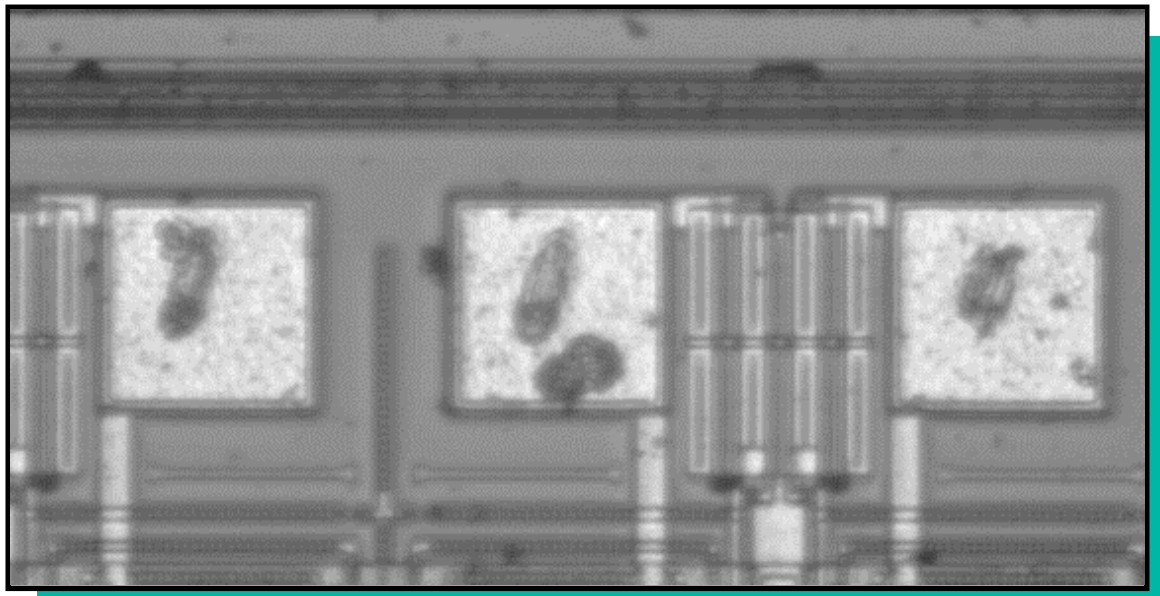
Background variation due to wafer process

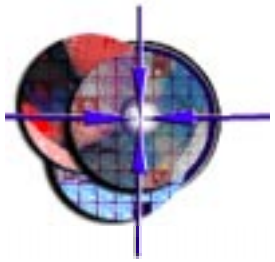


Probe Mark Inspection

More challenges

Dirt on pads

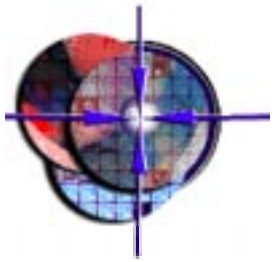




Probe Mark Inspection

More challenges

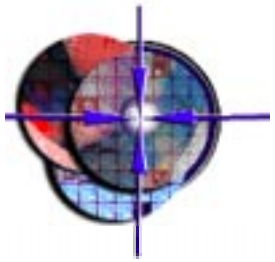
- **New probe card technologies**
  - membrane
  - vertical probe
- **C4 technologies (Flip Chip)**



Probe Mark Inspection

Summary

- **PTPO provides**
  - close loop control
  - data can be used for process monitoring
- **PMI options**
  - inspects every n^{th} die on every n^{th} wafer
  - min/max mark size
  - max # of fails per wafer
  - consecutive fail limit
  - evaluate drift
  - guard band adjustment



Probe Mark Inspection

Summary

- **Current PMI provides user maximum flexibility**
- **Minimizes operator intervention**
- **In-line process verification**
- **Probe card validation**
- **Minimal throughput hit**
- **Post probe checking**