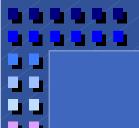
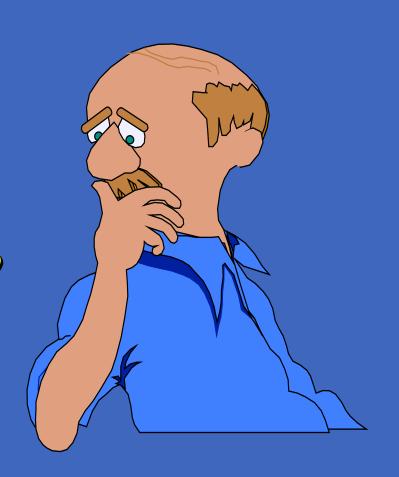
### MULTI-DIE PROBING

by John Peters
Director, Test & MIS
Fujitsu Microelectronics, Inc.





Why multi-die?



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### Test times are increasing!



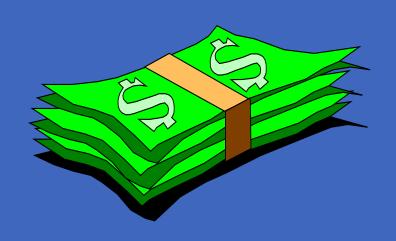






## Costs are going up!

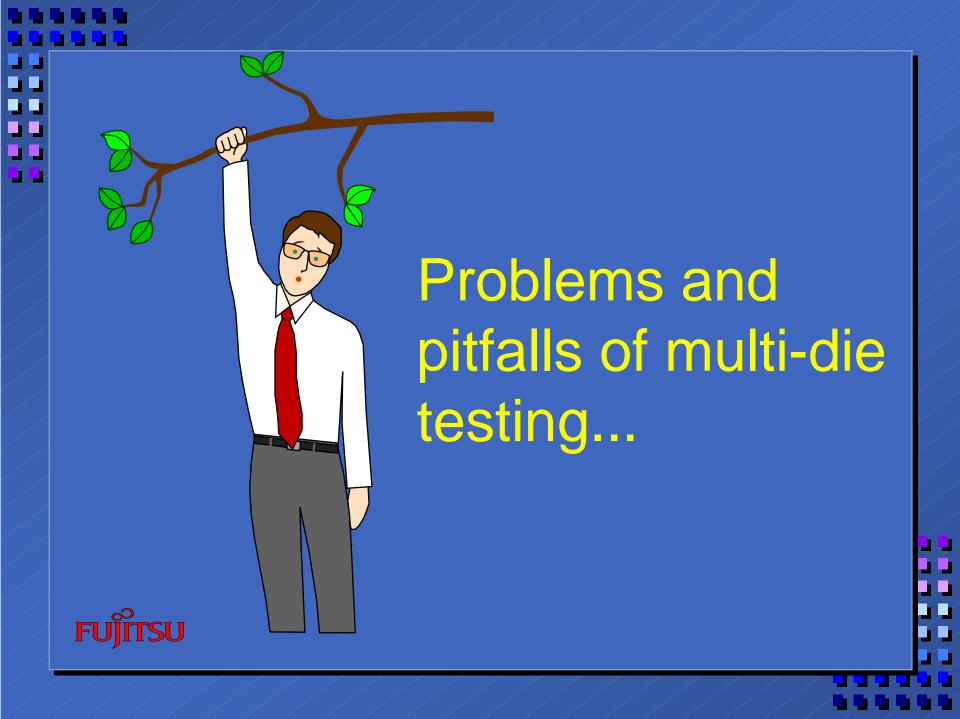




Hardware Cost: ATE, Probers& Probe Cards

Direct Labor costs are rising





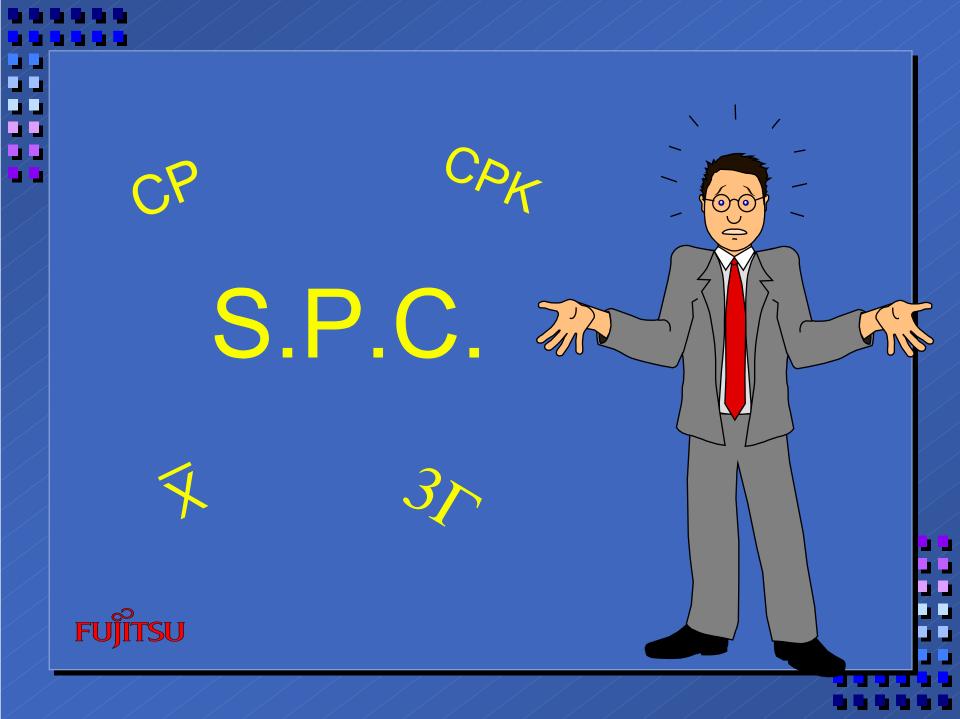
- The Boss
- Cost of hardware
- Probe card design
- Hardware check-out time
- Identifying problems as they occur during testing

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S.S.P.C.

Simple Statistical Process Control





# While testing, compare DUT's good die against all DUTS so that each DUT yields the same

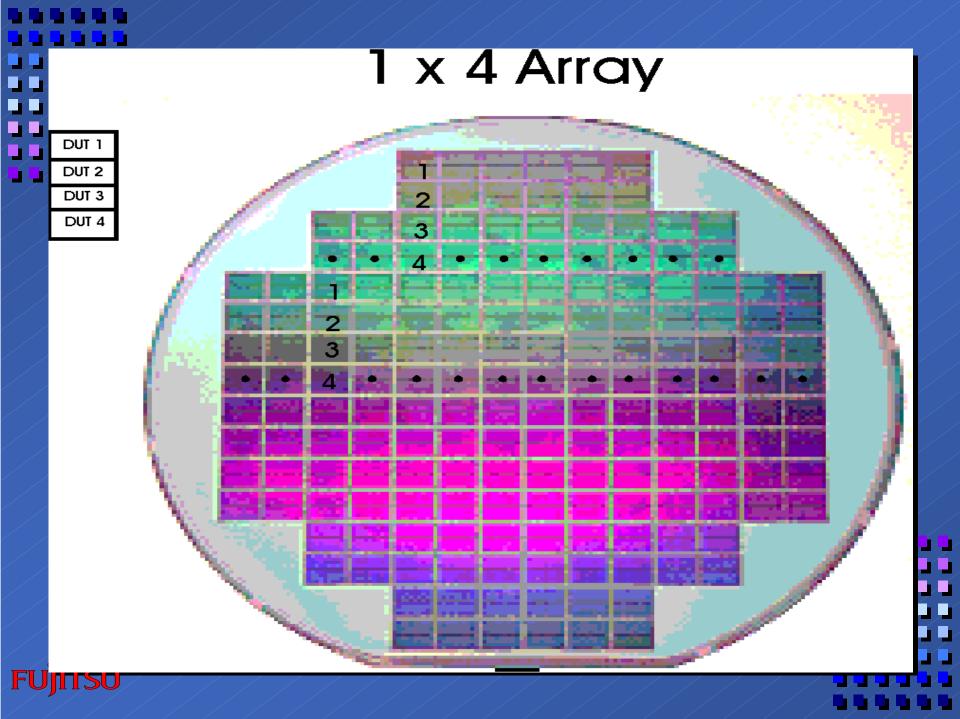
- If good die varies more than (3 die) DUT to DUT stop testing
- Future: Program will automatically verify bad DUT on a probe card with previously tested good die

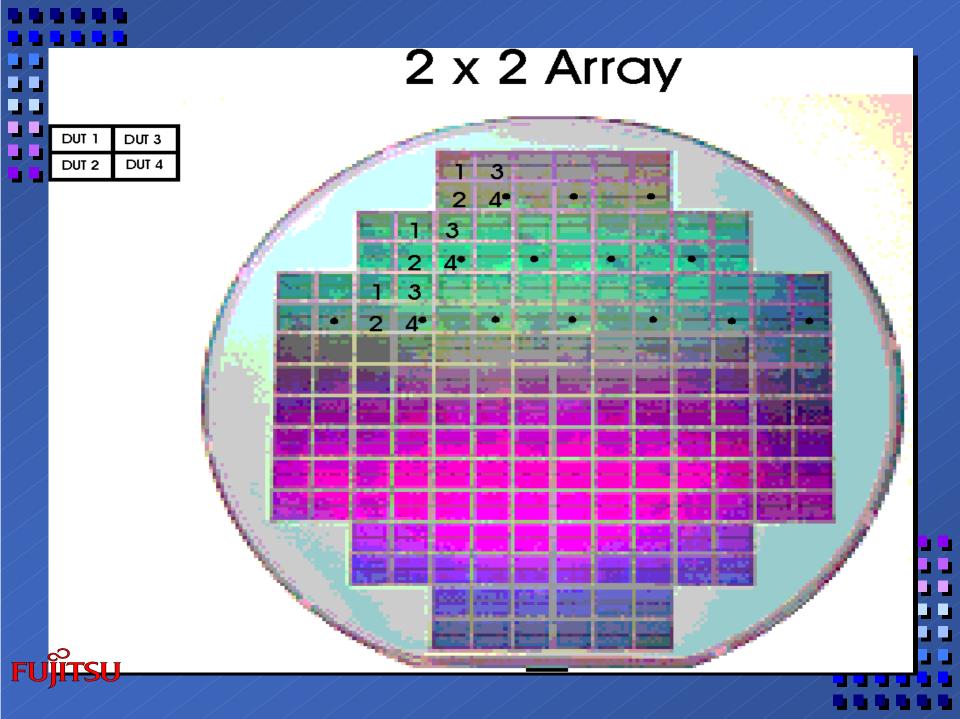


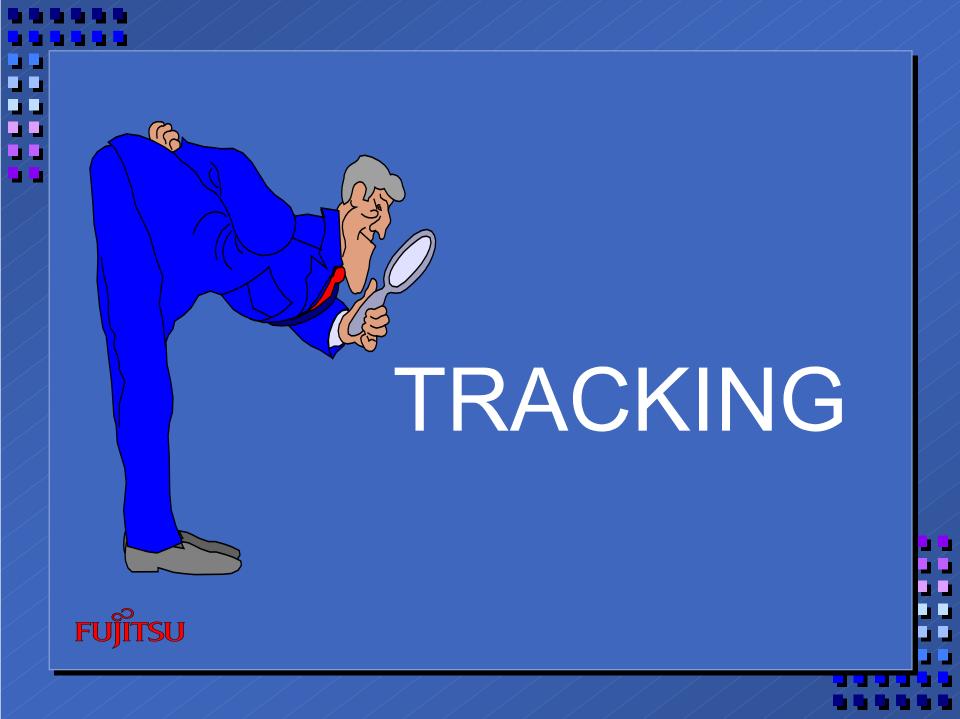
#### Compare failure modes

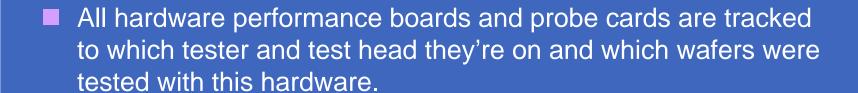
- If more than (3) consecutive common failures, verify the setup
- If more than (6) open failures per wafer, stop and verify the setup











- Setups are automatic:
- Lot numbers are bar coded
- Operator ID is bar coded
- Test program selection is automatically downloaded
- Automatic probe to pad alignment
- \* Future (October) auto probe mark inspection
- All SPC trips require operator ID to clear.





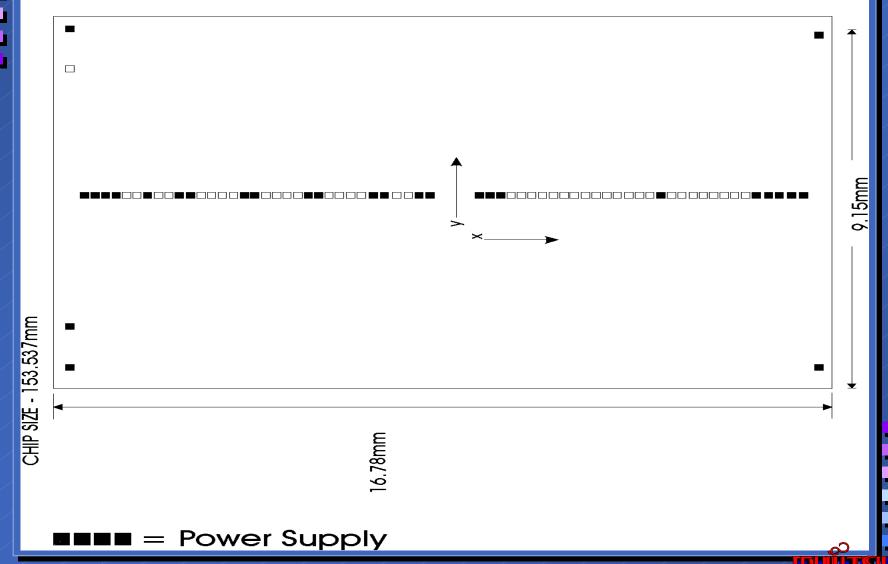




# Current 64Meg DRAM Pad Layout

**FUJITSU** 

#### 64Meg DRAM



#### What is FMI GMD Using For Probe Cards?

- 4Meg DRAM membrane probe cards were qualified for 8 DUT testing
- Currently, 64Meg SDRAM is qualified for 8 DUT tungsten needle probe cards (250 mm diameter)
- Evaluated:
  - Vertical (Cobra)
  - Modified Tungsten
  - Epoxy Ring
- In September we will use a tungsten needle card for 16 DUT (2 x 8) 300 mm diameter
- We would like a 3 X 6 Array (18 DUT) card





- Currently using GPIB interface to control prober stepping
- Results: No major probe card repairs with more than 6,000 wafers probed per card

