Wafer Temperature Control for Testing High Power Chips
Measured Thermal Chuck Performance

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History

- Commercially available thermal chucks provide uniform temperature control only when testing low power devices.
- In the past IBM has developed custom internal solutions for testing high power Bi-Polar devices, US patents 5001423, 5088006, 5186238.
- Current management philosophy is towards a vendor supported chuck which can be retrofit to Electroglass steppers.
- The work presented here is the result of a joint development project between IBM, Digital and Temptronic Corporations.
- The goal was to end up with a state of the art, dry interface, high power thermal chuck sold and supported by Temptronic Corporation.

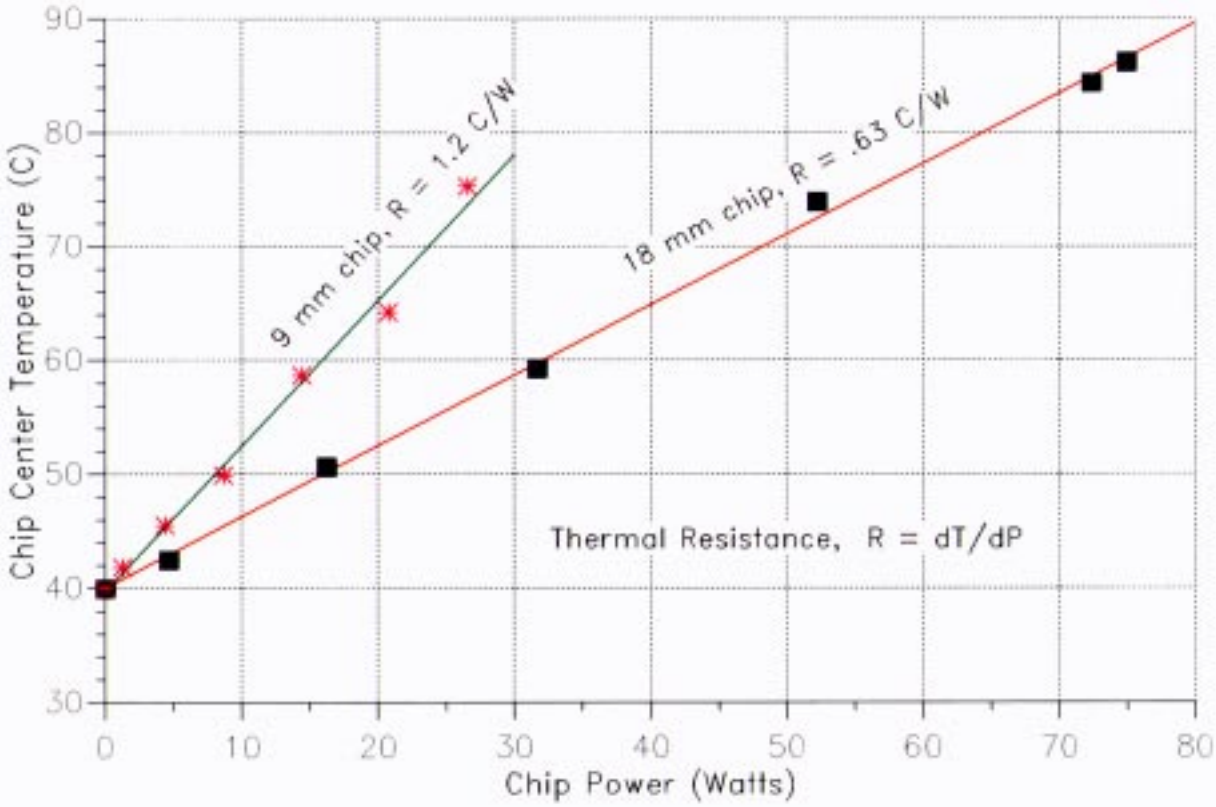
OVERVIEW

- ***Measured Thermal Performance***
  - Conventional thermal chuck.
  - Prototype high power thermo chuck.
- ***Chuck Construction and Theory***
- ***Finite Element Thermal Models***
  - Understand and optimize chuck design.
  - Extrapolate measured data to other chip sizes.
- ***Predicted Chip Temperature as a Function of;***
  - Chip Power
  - Chip Size
  - Location on Chip
  - Chip Location on Wafer
  - Test Time

Measured Thermal Performance

- ***Testing***
  - Conventional thermal chuck and prototype Temptronic high power thermo chuck.
  - 200 mm IBM thermal wafers have integrated heaters and temperature sensors.
  - Two custom Cobra probe heads, 80 and 2218 probes.
  - Two specific chip sizes tested, 9 mm and 19 mm square.
  - Ten chip sites across two wafers, average and standard deviation.
  - Air and Helium interface.
- ***Results***
  - Measured temperature increase is linear with respect to power.
  - Thermal resistance is defined as the change in temperature at a point on the chip divided by the total chip power.
  - Thermal resistance is strongly dependent on chip size.

Typical steady state measured data for a chip site near the center of a conventional thermal chuck



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Conventional Thermal Chucks

- Use a temperature sensor in the chuck surface to control heaters or thermo electric units.
- High Power devices cause temperature gradients in chuck surface.
- Thermal performance is dependent on distance to the temperature sensor.
- Conventional thermal chucks provide uniform temperatures only with low power devices.
- Design allows rapid change to new test temperatures.

High Power Thermo Chuck

- Optimized liquid cooling channels in a copper chuck.
- High velocity fluid flowing physically close to the chuck surface.
- Constant liquid inlet temperature (= chuck set point temperature).
- No temperature sensor in chuck surface.
- Thermal performance is independent of chip location on chuck.
- Helium interface between wafer and chuck surface.
- Chuck has slower response to a change in test temperature.
- Designed to fit on an Electroglass Z stage.

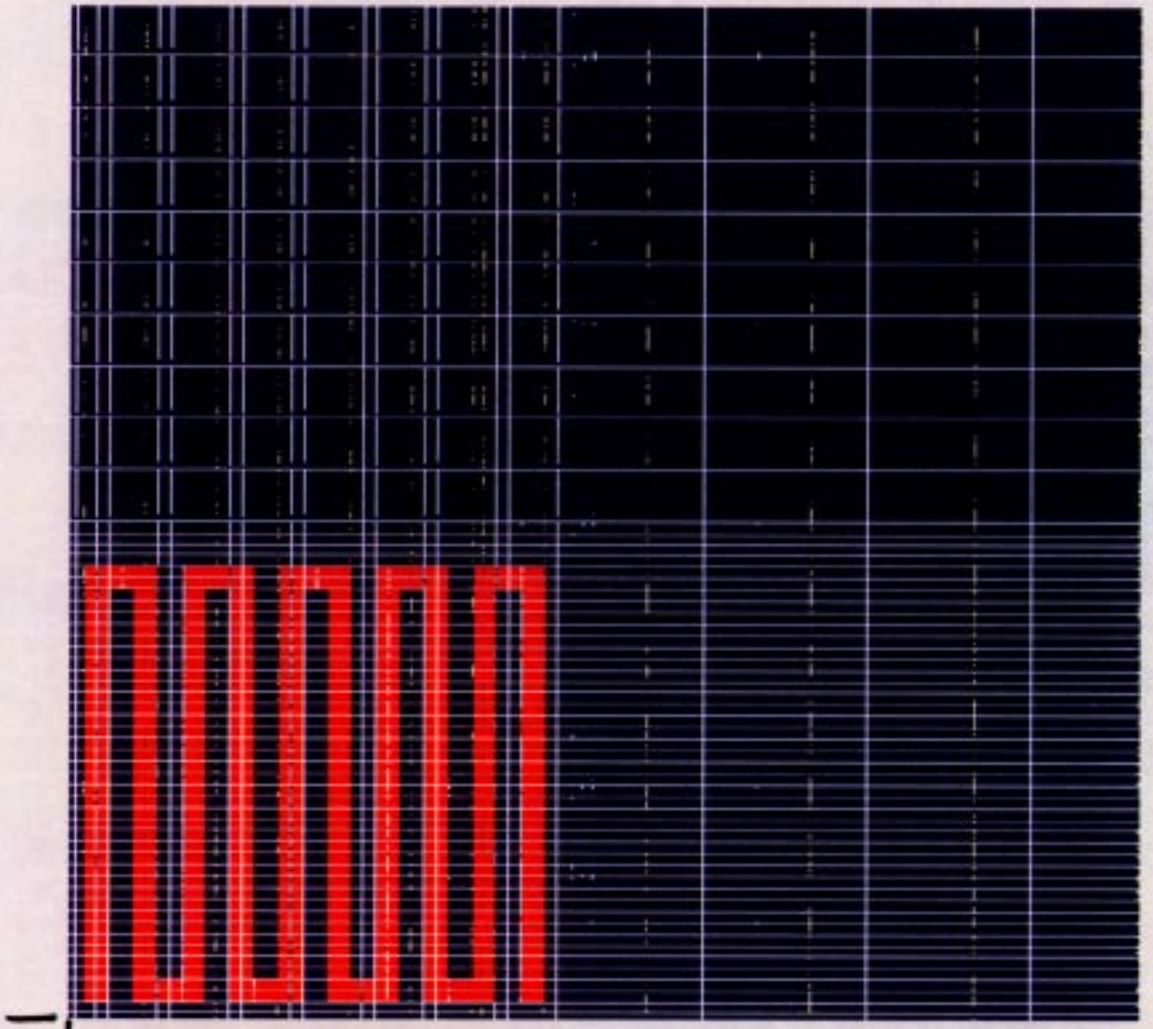
Thermal Modeling

- ***Analytical Models***
  - Empirical and closed form solutions were used to optimize the size and shape of the liquid cooling passages.
  - Analytical models assume one dimensional heat transfer from the device directly down into the chuck and neglects heat spreading into adjacent chip sites.
  - Reasonable assumption only for very large chips.
- ***Finite Element Analysis***
  - Detailed 3-D models of the thermal wafer including the heater pattern and temperature sensors.
  - Conduction models of the entire thermal chuck coupled to the wafer.
  - Heat spreading into adjacent chip sites is a predominate mechanism with small chips.
  - 3-D Modeling is used to extrapolate measured data to other chip sizes and uniform heat flux.
  - Finite element modeling also predicted the transient heat transfer and chuck stiffness.

I-DEAS Master Series 4: Simulation

Databases /home/gardell/ideas28dlg3b.unf1
View : ISOMETRIC (modified)
Task : Mesh/QD
Model: fe1 17.3mm serp on 38mm sq wafer

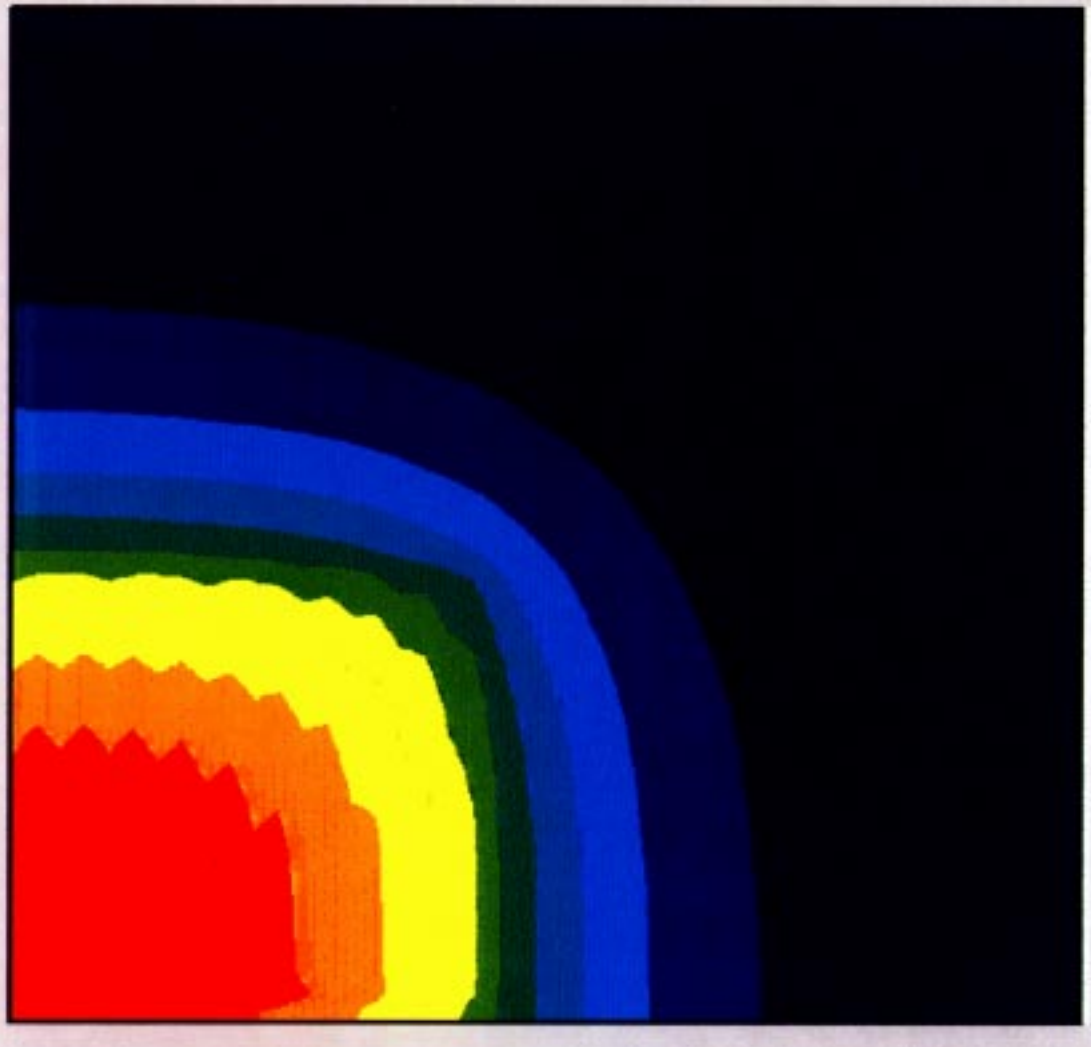
21-May-97 10:58:43
Units : SI
Display : No stored Option
Model/Part: Elmo Mesh
Parent Part: Penta therm chip



/u/gardell/ideas20dlg3.mf1

RESULTS: 3- B.C. 2,LOAD 2,TEMPERATURE_3
TEMPERATURE - MAG MIN: 5.40E-02 MAX: 1.17E+01

VALUE OPTION: ACTUAL



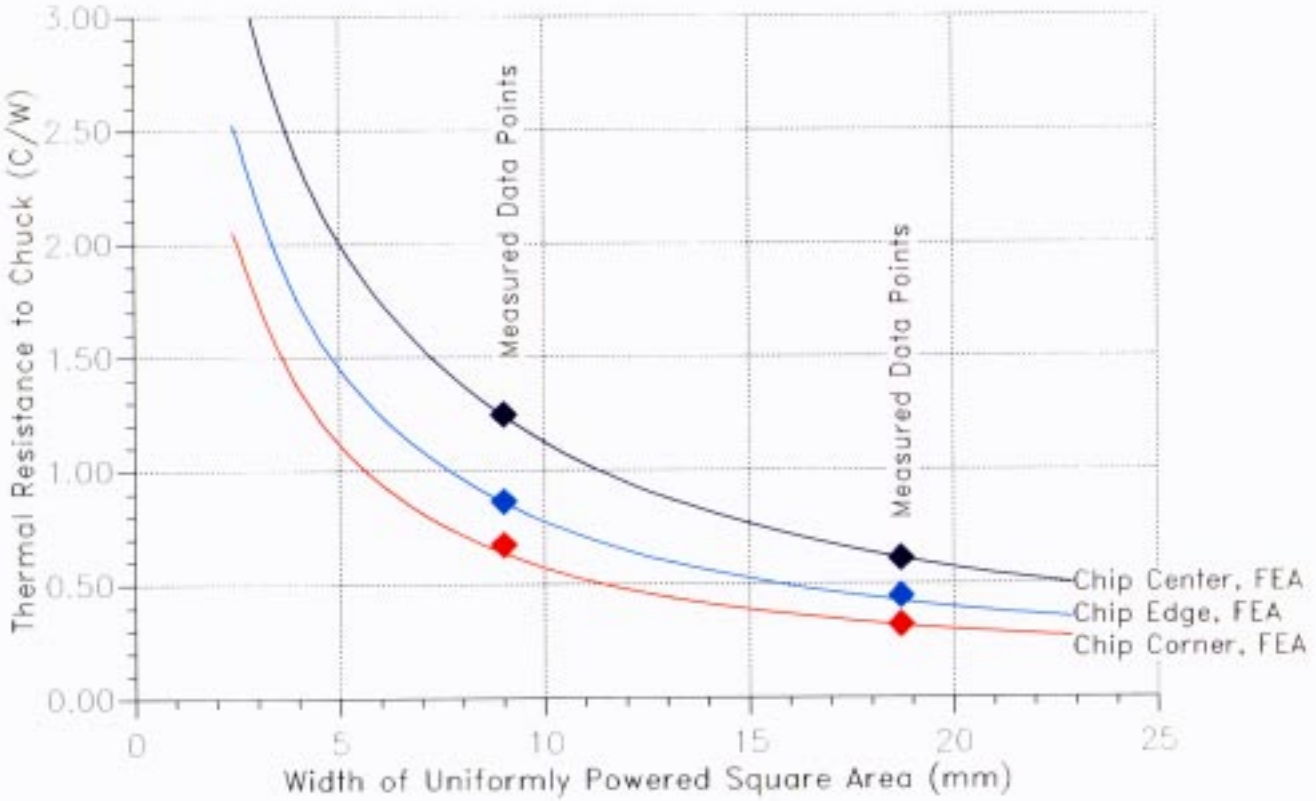
1.17E+01
1.05E+01
9.34E+00
8.18E+00
7.02E+00
5.86E+00
4.70E+00
3.54E+00
2.38E+00
1.21E+00
5.40E-02

Y
Z
X

Finite Element Model Results

- The thermal interface resistance between the wafer and chuck is initially unknown.
- It is a function of surface finish, hardness, thermal conductivity, interface force and interstitial fluid.
- The interface resistance in the finite element model is adjusted to fit one measured data point and then solved for a wide range of chip sizes.
- The other 5 measured data points fall very near the FEA curves resulting in high confidence in the models and measured data.
- The thermal resistance is strongly dependent on chip size.
- The center of the chip gets about twice as hot as the corner of the chip.

FEA predicted thermal resistance vs chip size curve fit to average data measured on a conventional thermal chuck.



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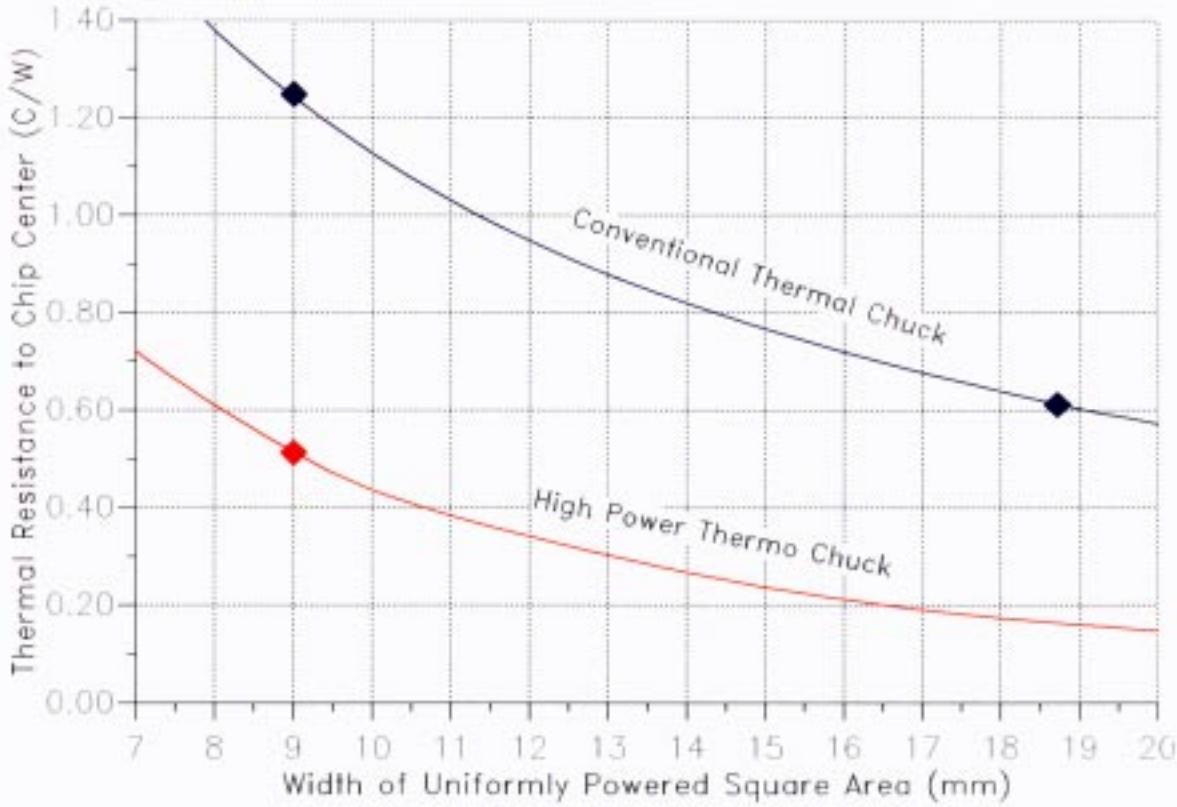
Thermal Resistance Comparison

- Comparison of conventional thermal chuck and the prototype Temptronic high power thermo chuck.
- Finite element model results and average measured data.
- Thermal resistance between the center of a uniformly powered square area and the chuck.
- To use the chart, thermal resistance is estimated from the chuck type and chip size and multiplied by the chip power to obtain the steady state temperature rise at the center of the chip.
- This is a very concise way to document the thermal performance. However, the effect of chip size on chip temperature is not intuitive from the chart.

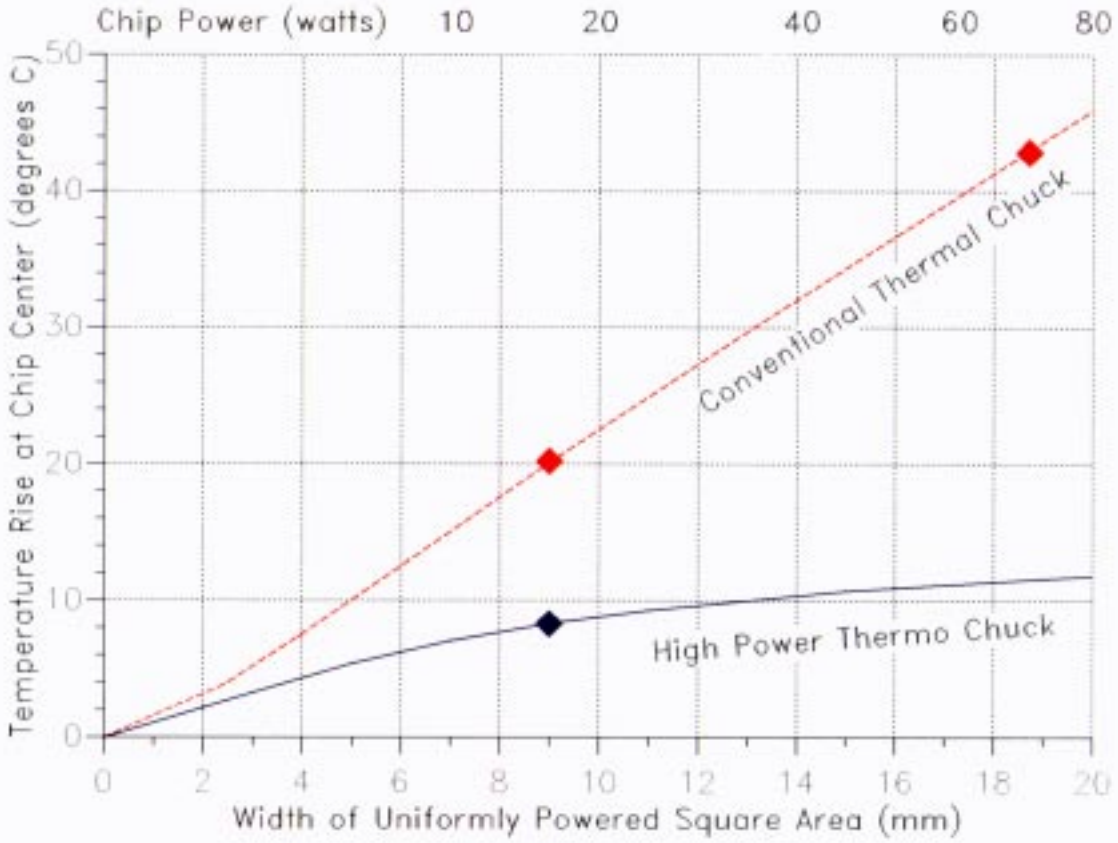
Thermal Resistance Comparison of conventional and high power chucks, FEA predicted curves and measured data points.



Temperature Rise Comparison

- Alternate method of presenting exactly the same data as the previous chart.
- Pick a constant value of heat flux to apply to various size chips (i.e., 20 Watts / sq. cm).
- Solve for chip temperature rise vs size of heated area.
- Chip temperature rise is read directly from the chart, total chip power also shown.
- Results can be scaled to other values of heat flux or chip power.
- Note that a 1-D model which neglects heat spreading into adjacent chips would result in a horizontal line at delta T = (Q/A)(1/h).

Temperature rise comparison of thermal chucks assuming uniformly powered square areas at 20 W/sq cm.



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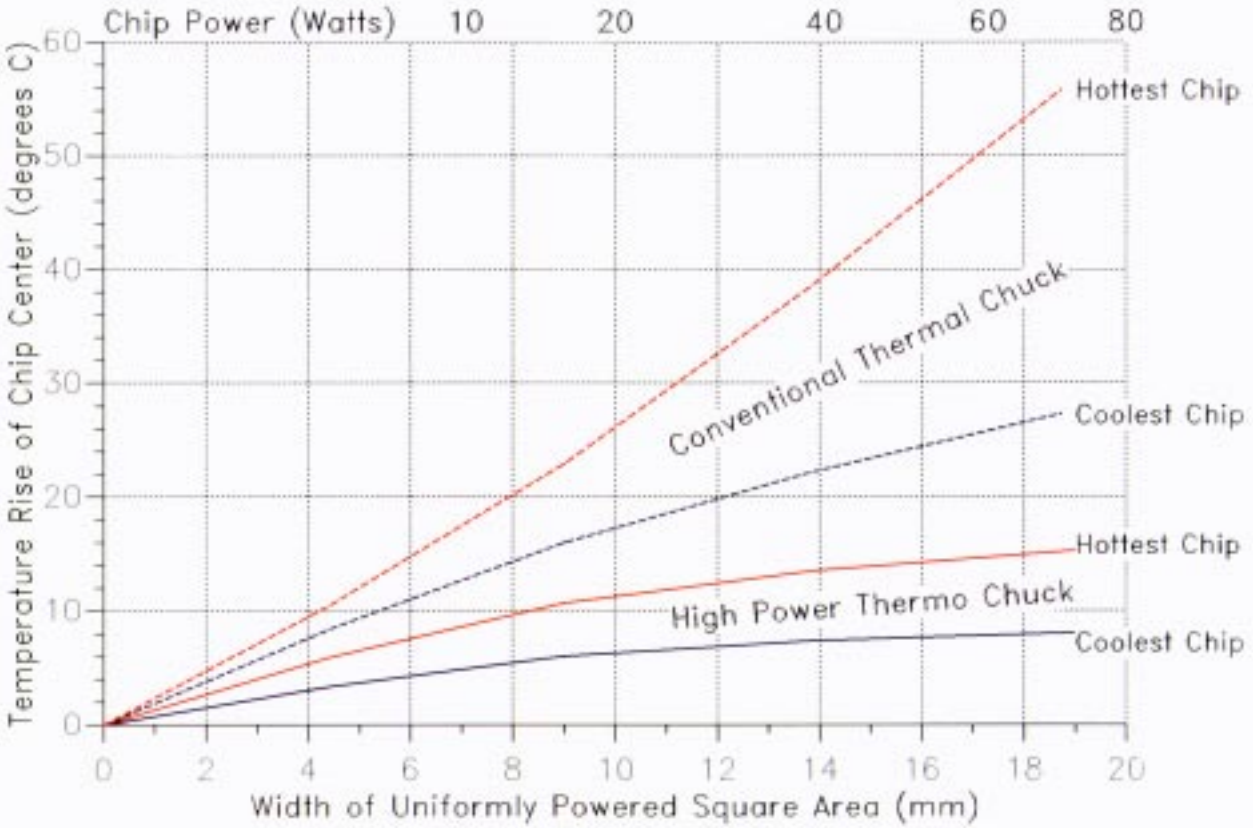
Temperature Uniformity

- Temperature variation between the center and corner of a typical chip on the chuck.
  - Caused by heat spreading out into adjacent chip sites on the wafer.
  - These temperature variations may not be present at package test.
  - Will the device function reliably with a large temperature difference between two points on the same chip?
- Temperature variation between the hottest and coolest chip sites on the chuck (+/- 2 std. dev.).
  - Caused by variations in interface resistance (copper is better) and internal resistance of the chuck (high power chuck is much better).
  - Two different chips on a wafer can have significantly different test temperatures even if the chip power is identical.
  - What is the effect on product function, yield and reliability?
- Effects of helium interface and probe force on chuck thermal performance.
  - Adding helium at the wafer to chuck interface improves thermal performance by 10 to 20%.
  - Increasing the number of probes (probe force) improves thermal performance by 24 to 33%.

Chip to chip temperature variation across chucks, +/- 2.0 std. dev.
chips powered to 20 W/sq cm.



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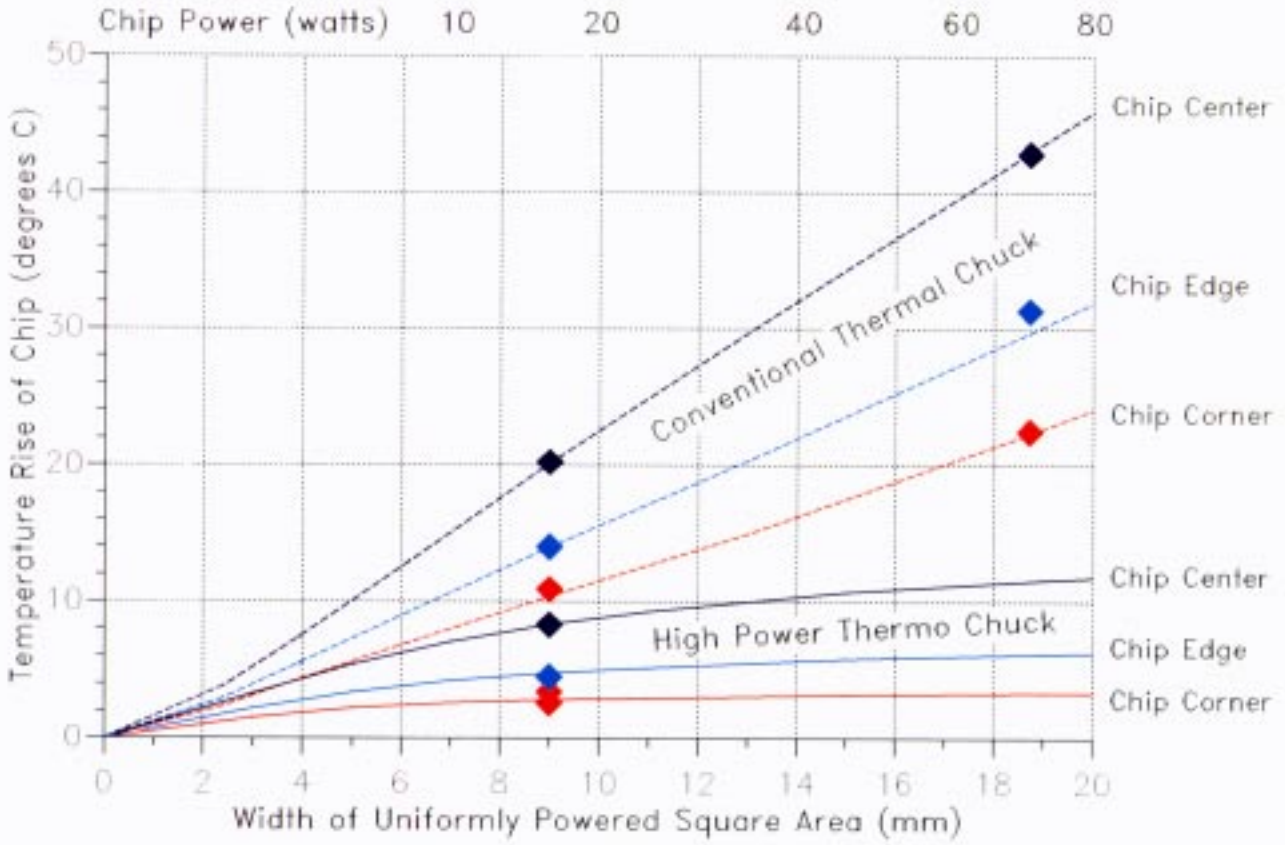
Temperature Variation Across Average Powered Chip
Uniformly Powered Square Area, 20 W/sq cm



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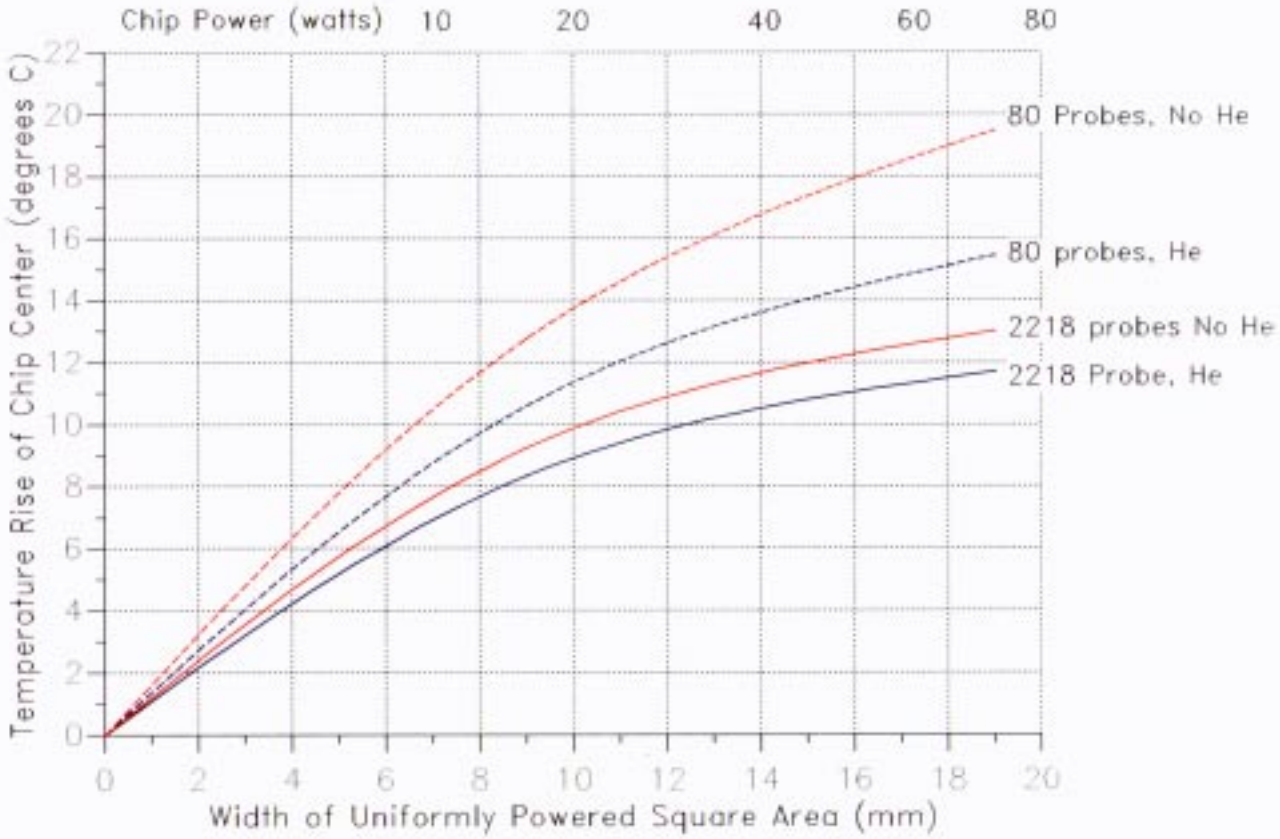
Temptronic high power thermo chuck at 20 W/sq cm chip power.
Effects of Helium interface and probe force.



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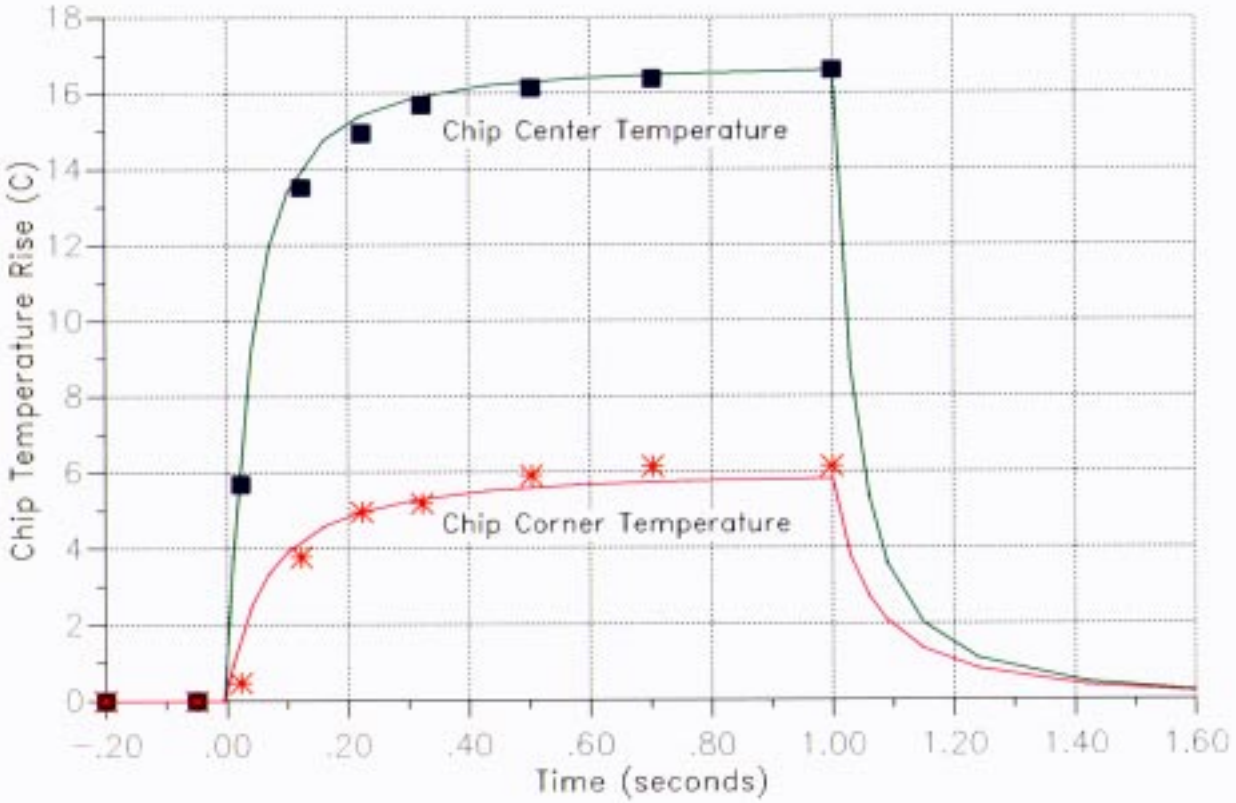
Transient Temperatures

- Transient temperatures predicted with the finite element model.
  - Good agreement to measured temperature and time.
- Conventional thermal chucks require a long time to reach a steady state temperature for chip sites far from the chuck thermocouple.
- Chip temperature increases very quickly in the first 100 milli seconds after the power is applied.

**Temptronic high power thermo chuck,
measured data and FEA predicted transient response,
30 watts on a 9 mm chip for 1 Second.**



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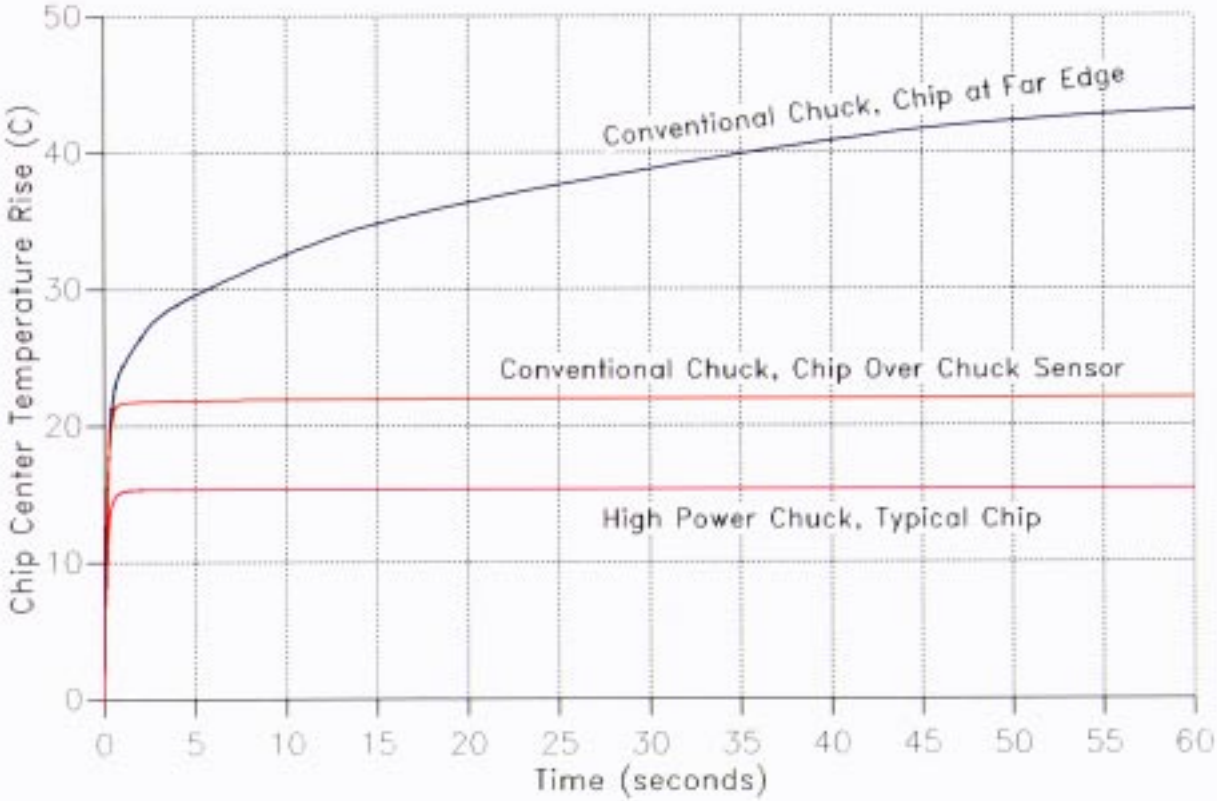
Comparison of transient thermal response between conventional and high power thermal chucks, 65 watts on a 19 mm square chip.



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Conclusion

- Large temperature variations (40 C or more) will occur during wafer test of high power parts. Temperature variations will be a function of:
  - Chip Power
  - Chip Size
  - Location on Chip
  - Chip Location on Wafer
  - Test Time
  - Wafer chuck performance
- If the chip power map is known, verified thermal models can be used to predict chip temperatures.