

An Introduction To Area Array Probing

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1998 Southwest Test WorkShop

An Introduction To Area Array Probing

Topics:

- ▼ Introduction & Background
- ▼ Considerations & Experiences
- ▼ Q & A

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Introduction & Background

▼ Vertical Probe Market Growth

– Potentially 40% of the Probe Market Revenue by 2001

– Technical Drivers

Performance --> Data Rates, Power Distribution, etc.

I/O Requirements --> 2500 and Growing

Packaging --> Multi-Dut (e.g. TCM)

Perimeter Pad Applications

– Business Drivers

- e.g. Cost/Performance, Customer Requirements, etc.....

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Introduction & Background (cont.)

▼ Area Array Probing History/Experience

– Over 30 Years in IBM

A Variety of Vertical Technologies (Ref. 1) Until.....

– COBRA

Patented in 1977!! (Ref. 2)

Key Enabler Even Today

Typical Pitch: .005" on .009"/.010"

– "Vertical" Space Transformer (Fanout)

Wired

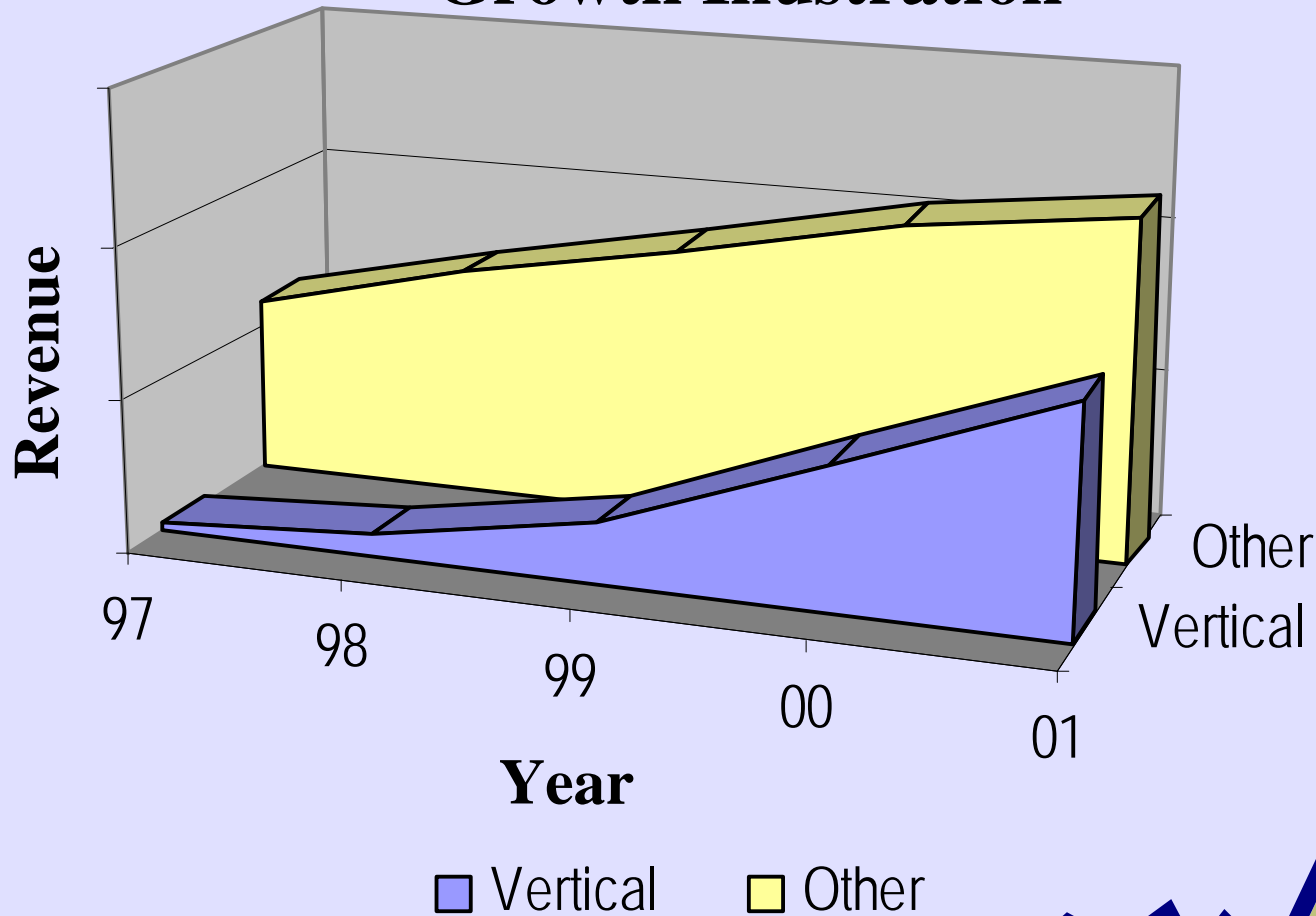
Ceramic

– Test System & Prober 'Tailoring'

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Vertical Market Growth:

Wafer Probes Growth Illustration



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Considerations & Experiences:

▼ **Test System/Methodology/Product**

– **Detecting Power/Ground Shorts**

"Soft Power" Protection

– **AC Performance: Product & Test System Design**

Power Distribution Network

Power/Ground I/O to Signal I/O Ratio and Placement

– **Product**

Evaporated or Plated C4's

Low Volume Solder / Height Variations

Run out (Evaporated C4's)

Retest Budget

High Temperature Test --> Greater C4 Pad Deformation

Reflow (If/When and Limits)

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Considerations & Experiences (cont.):

▼ Test Head

- **Planarity / Co-Planarity**
Set-ups May Differ By Probe Technology
- **Deformation/Movement**
Higher Probe Forces
Probe Technology Dependent

▼ Wafer Prober

- **Alignment**
Look-up Optics
Larger Probing Window/Target
- **Chuck**
High Z Force
Tilt Issues at Edge

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Considerations & Experiences (cont.):

▼ Wafer Probe

– Mechanical Specifications

I/O & DUT Capacity

Pitch Boundaries

PbSn Pick-up / Removal

– Electrical Performance

Bandwidth

Near-in Decoupling

Sub-System Contributions (Space Transformer, DUT Board, etc.)

Bulk & Contact Resistance

Current Carrying Capacity

– C4 Deformation Effects

Probe Technology Dependent

Retest Capability

Voids Occurring After Reflow --> Reliability Issue

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Considerations & Experiences (cont.):

▼ Wafer Probe

– Manufacturing Considerations

Robustness

Set-up/Replacement/Repairability

COO

– Source of Supply

Limited Offerings /Suppliers Today

Second-Sourcing

– Planarity / Compliance / Cleaning Effects

Probe Life

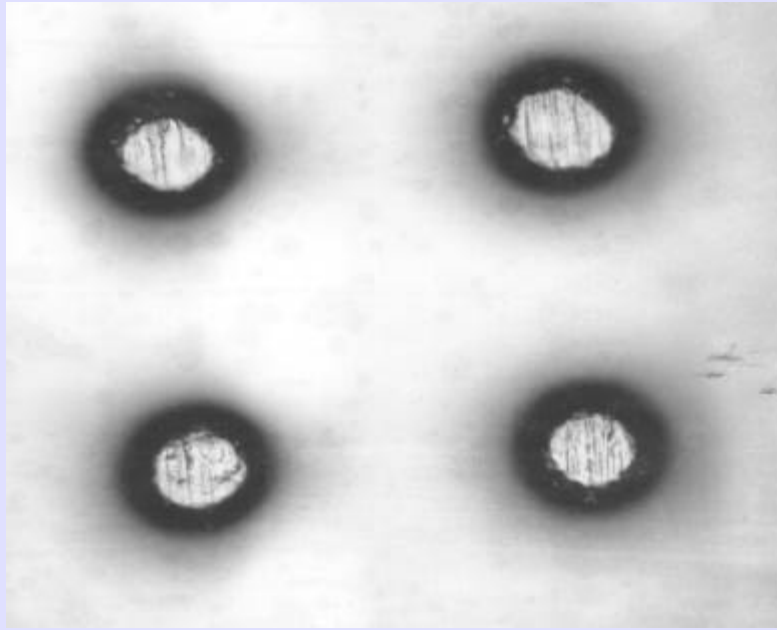
Force / Deflection - Operating Point/Range

Contact Resistance Vs. Number of Touch Downs

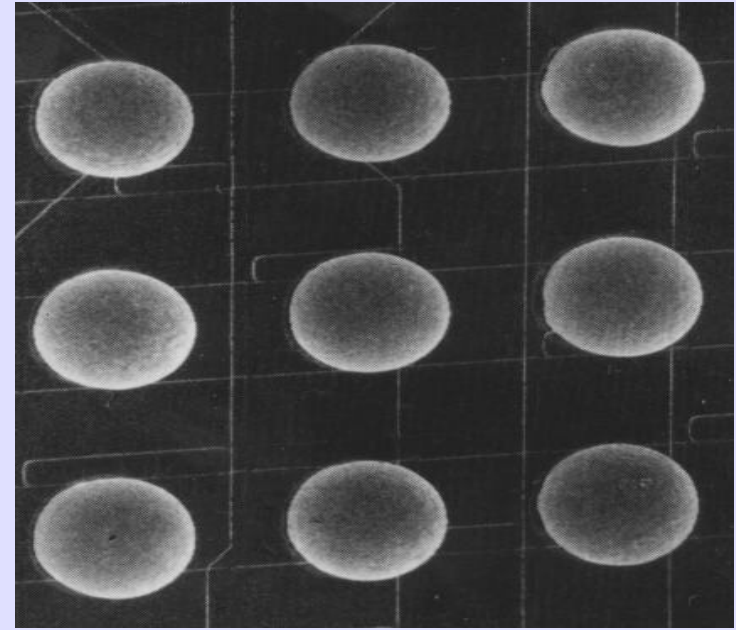
Cleaning Techniques: Abrasive, In-situ?

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C4 Deformation / Reflow:



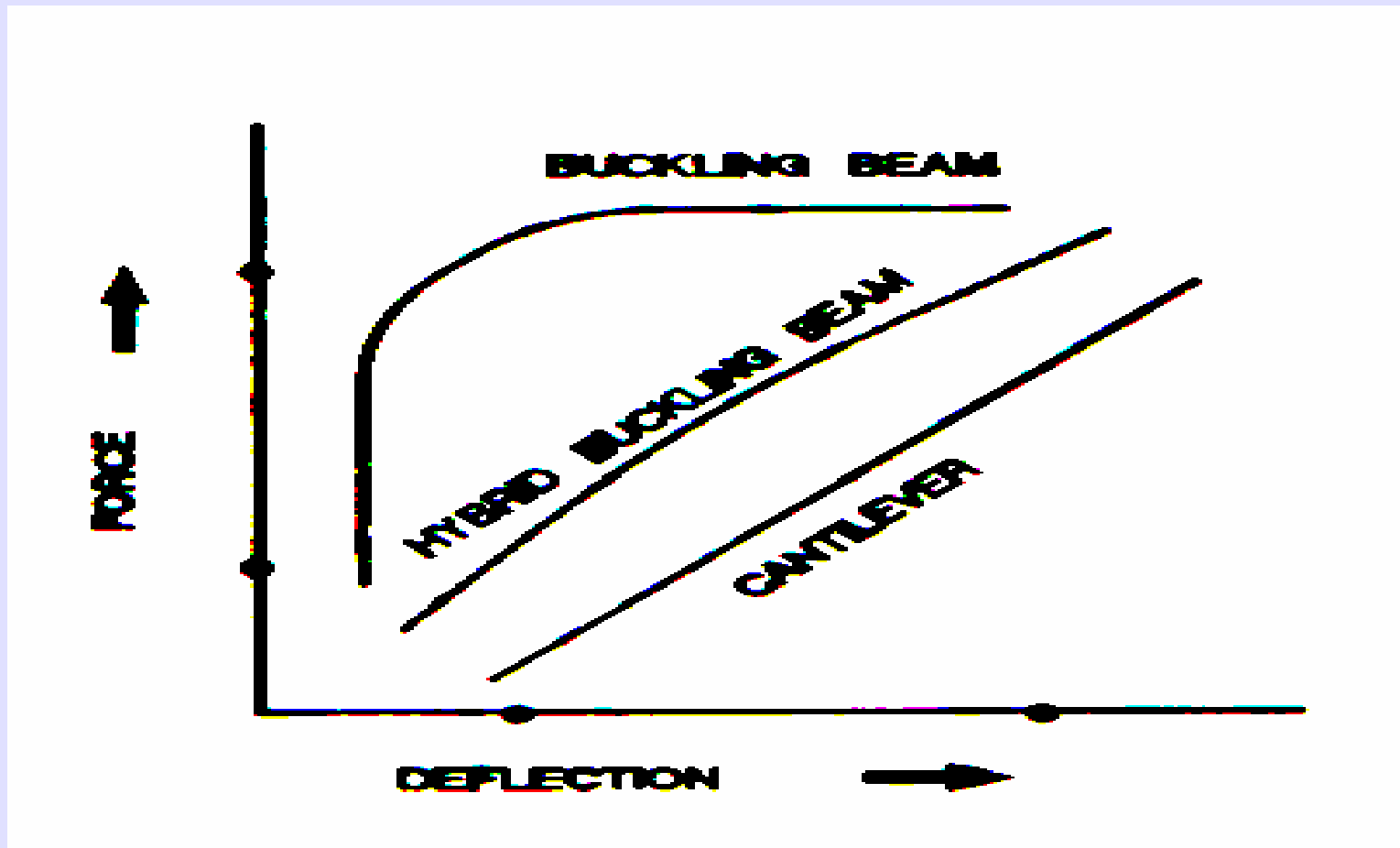
After COBRA Probing
(Optical 200x)



After Reflow
(SEM)

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Force / Deflection Curves:



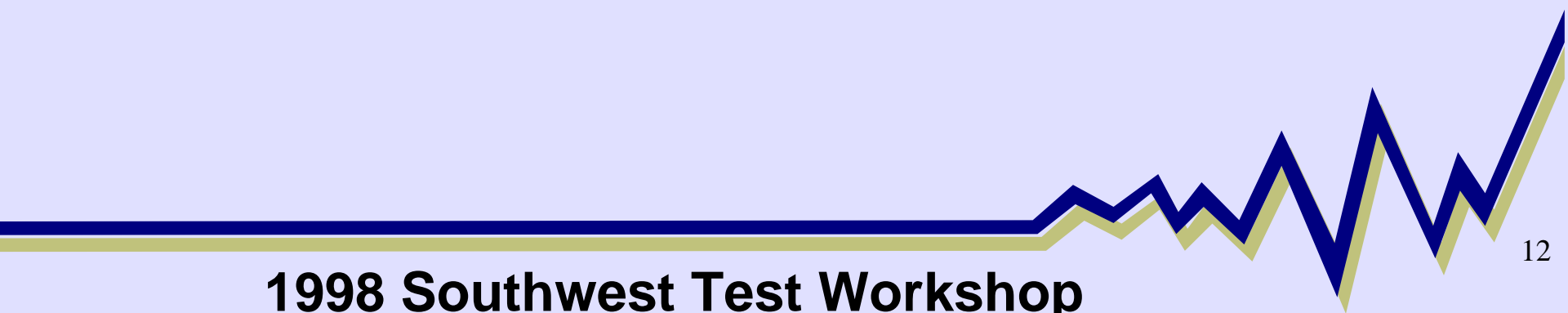
ref. 1

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Q & A:

▼ **What Are Your Experiences?**

▼ **Any Questions?**



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References & Acknowledgements:

– Ref. 1

"Probing Considerations In C-4 Testing Of IC Wafers" by Dennis J. Genin and Manfred Wurster, IBM Corporation, 1992

– Ref. 2

United States Patent #4,027,935; June 7, 1977; "Contact For An Electrical Contactor Assembly"; Herbert Byrnes and Richard Wahl (Assignee: IBM)

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