Halving Cost of Test Using Parallel Multi-Die Approach for Mixed Function Testing

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COTRED Project

- Funded by European Union under ESPRIT program
- Semiconductor Equipment Assessment
- STMicroelectronics, TEMIC-MHS, Schlumberger ATE
- Assessment of tester designed to reduce Cost of Test

COTRED Project Objectives

- To halve the Cost of Test of complex microcontrollers, comprising purely digital and/or embedded analog functions
- To ensure that ITS 9000*CV* fulfills the technical requirements of the users
- To evaluate the single to parallel program transfer efficiency and ease of use

Microcontroller Test Requirements

- Product complexity
  - Match mode
  - Analog
    - A/D and D/A
    - Wireless applications
    - TV applications
  - Embedded memories (ROM, EPROM, E^2PROM, Flash)
  - Timing and level calibration
- Test at speed
  - 4MHz to 80MHz
  - Test time between 1 and 10 seconds
- Pad pitch and die area

Why Parallel Test?

- Test more units with the same investment
- Optimize all hardware resources
  - QFP80 by 2
  - SDIP56 by 3
  - SO28 by 6
  - DIP16 by 8
- Better Return on Assets
  - Low ASP of Microcontrollers (declining by 10% per year)
  - VLSI testers cost from $0.5M to $2M
  - High pin count needed for some low volume parts

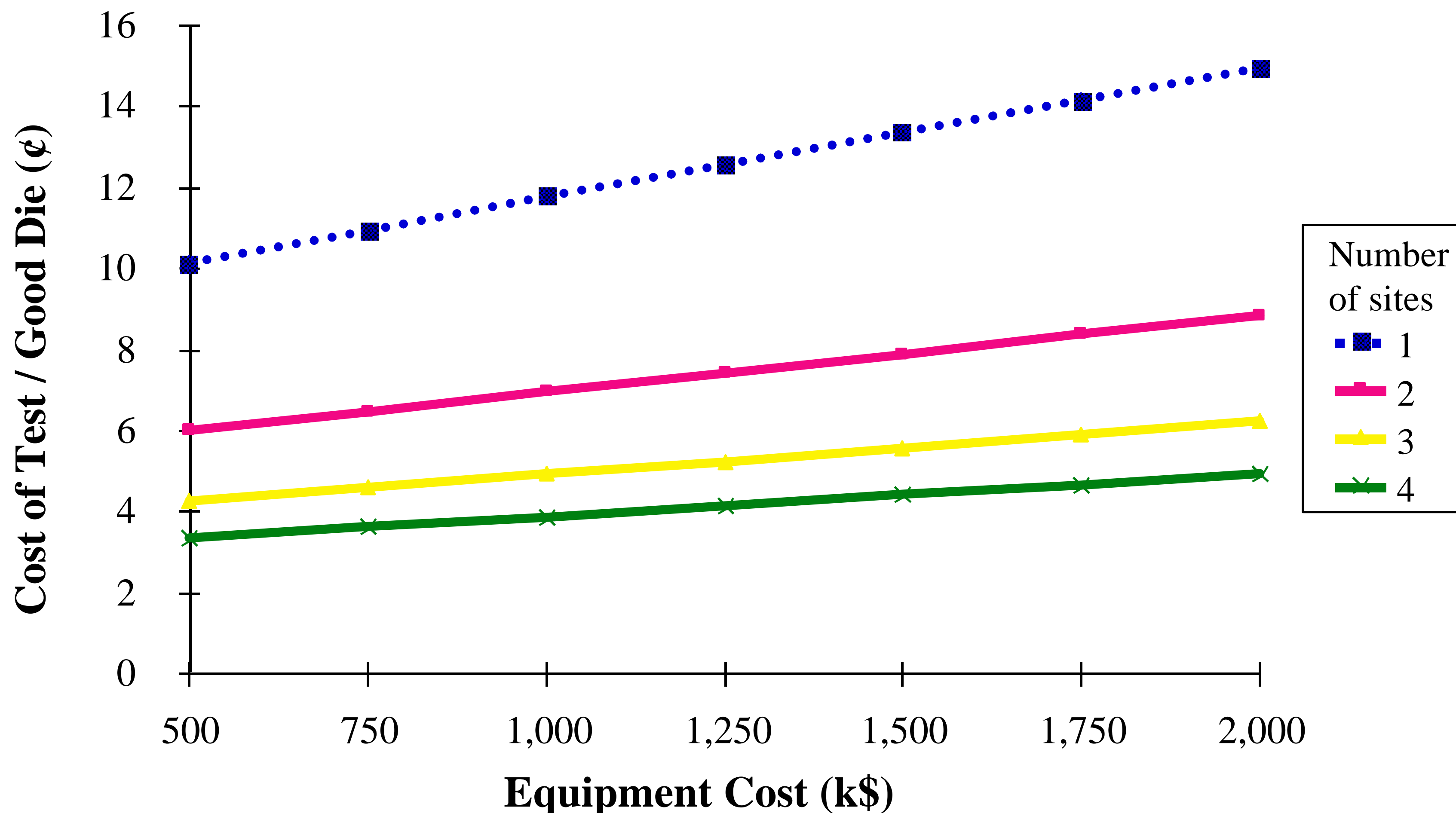
Cost of Test Analysis

- Test-related spending
  - Operating cost
  - Ramp up cost
  - Maintenance cost
  - Capital equipment cost

$$COT = \frac{\sum test_related_spendin}{\sum good_parts}$$

- Using ACOLYTE©
  - EXCEL® based cost analysis model
  - 126 parameters

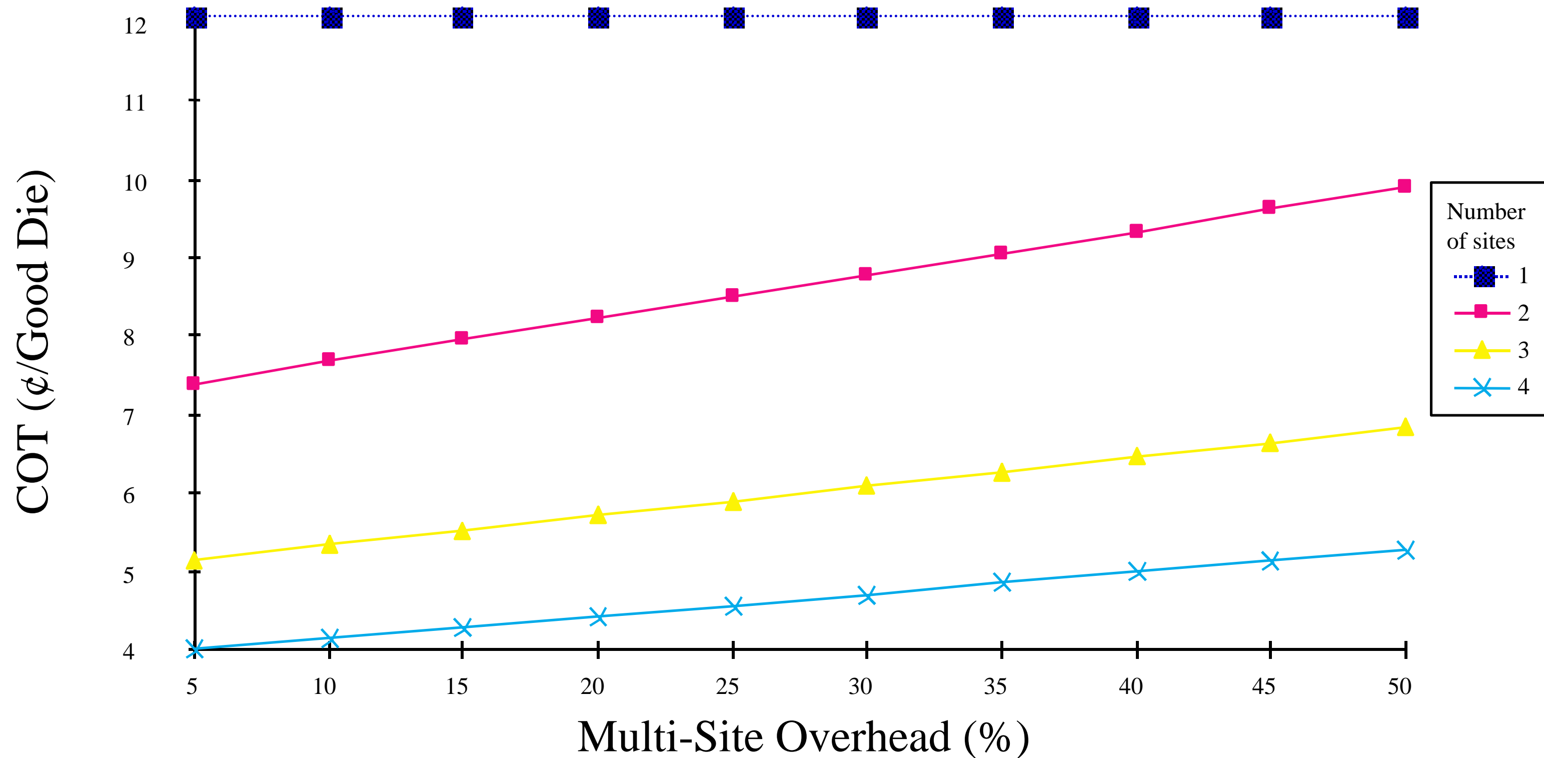
Key for Cost of Test Reduction



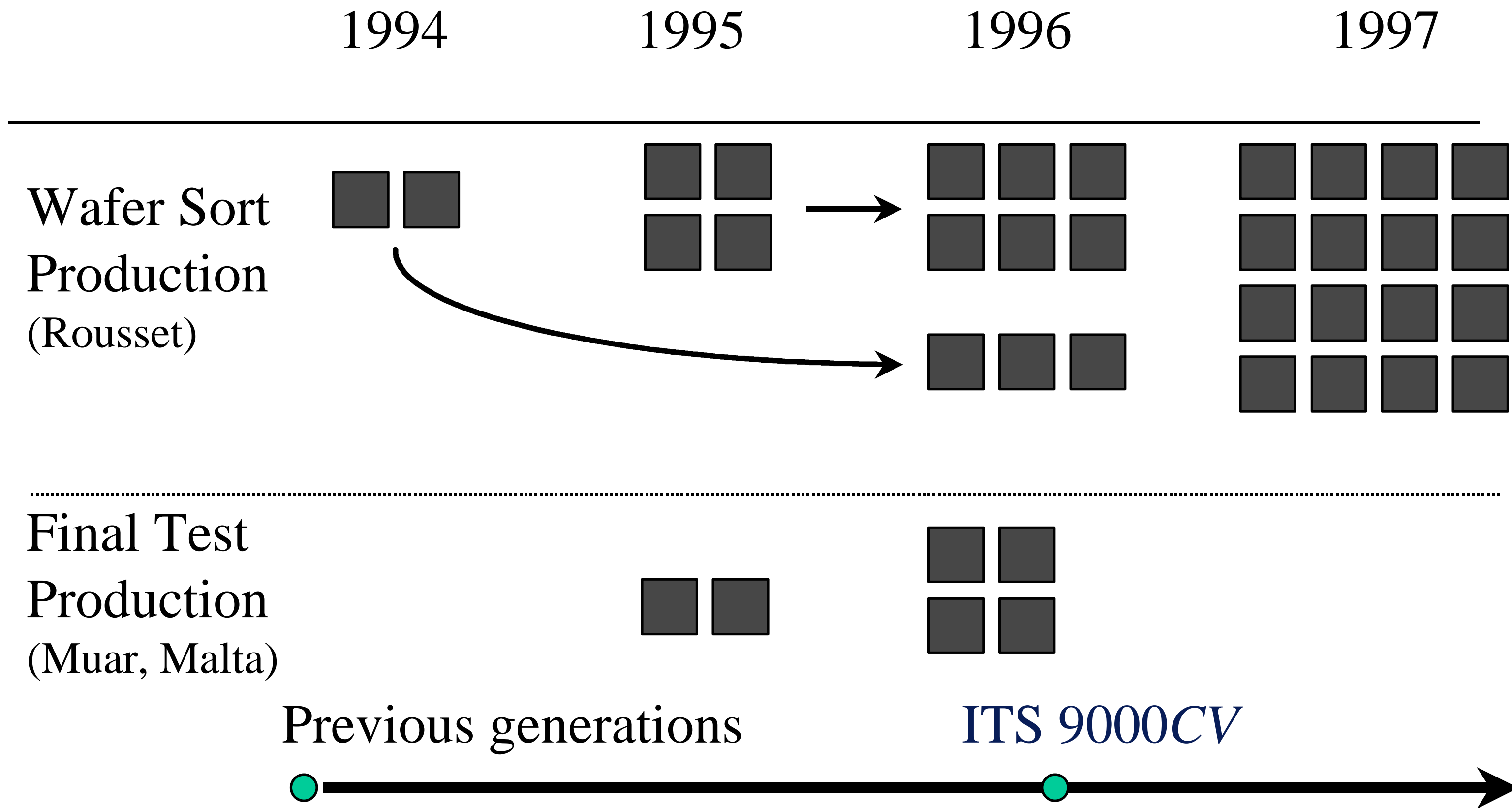
Issues for Parallel Test

- Wafer sort
  - Probing issues: pitch, layout, use of vertical probing
  - Handling and index time compared to test time
- Final test
  - Parallel handler (high parallelism & high efficiency)
  - Sorter and index time compared to test time
- Partner approach is mandatory
- Tester optimized for parallel test
  - Minimal overhead
  - Parallel resources

Importance of Overhead



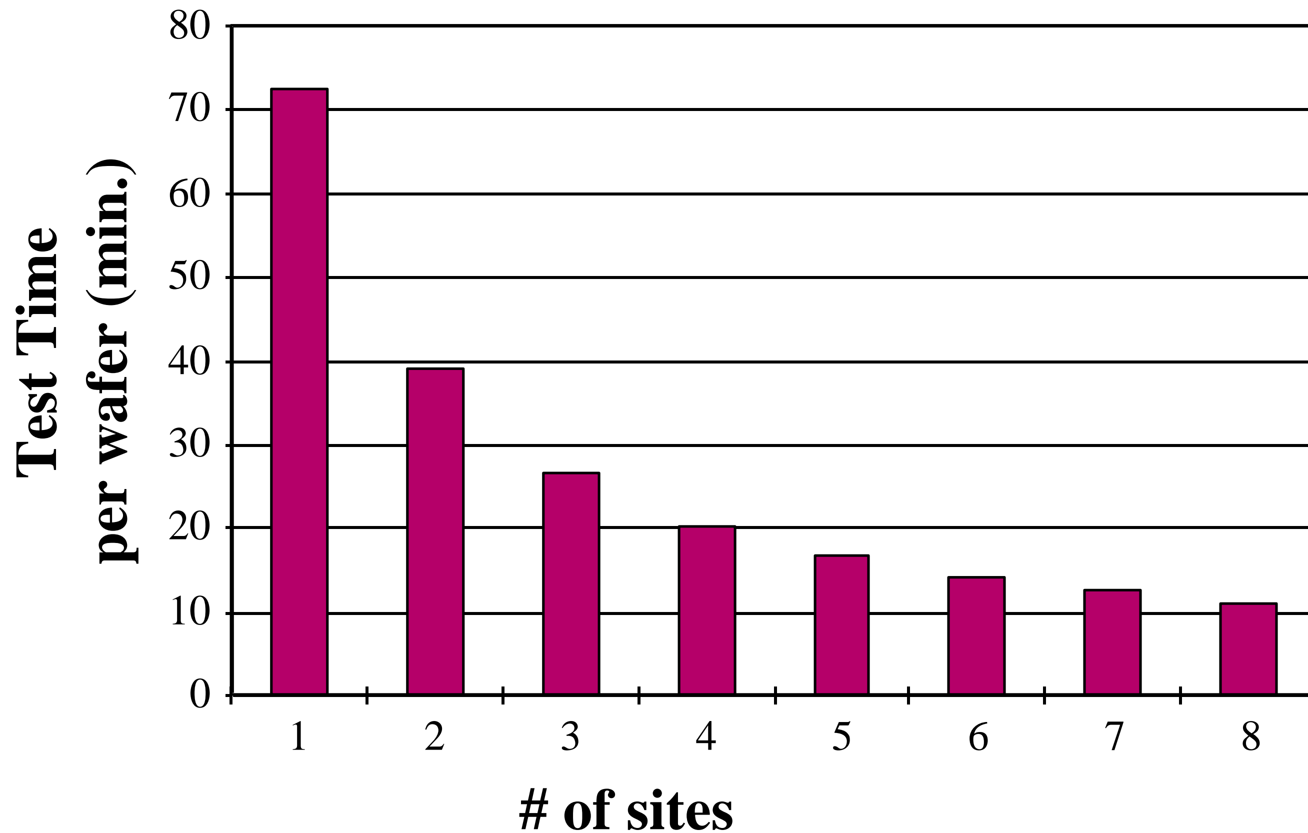
ST Micro's Parallel Test History



Achievement at STMicroelectronics

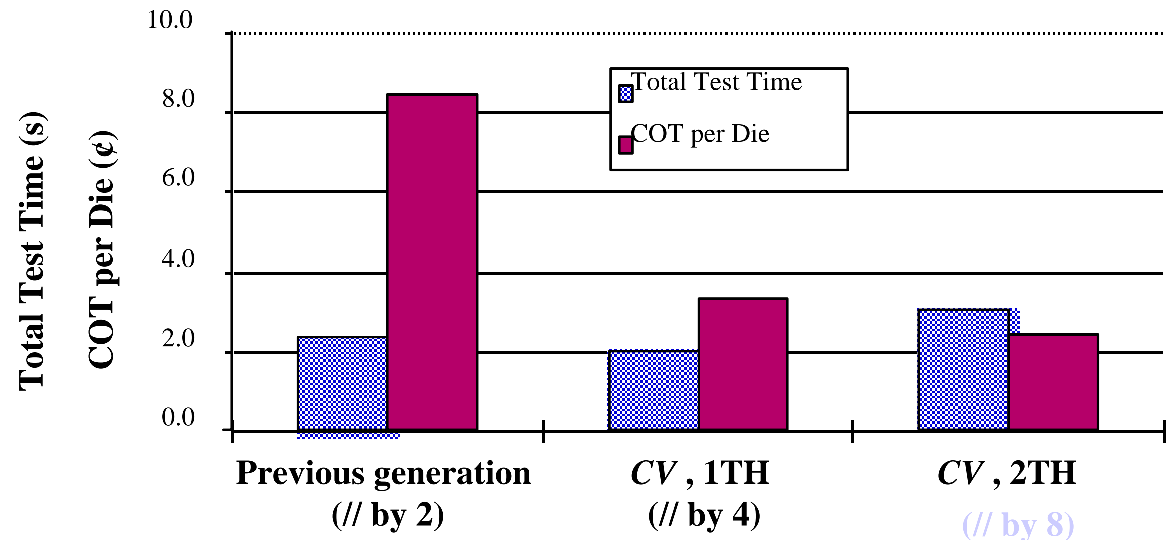
- Test Time $\Rightarrow Test_time_n \approx Test_time_1$
  - overhead is minimal
- COT per die (Throughput)
  - All products are tested by 2, 3, 4 or 6.
  - Transfer of single program into parallel automatic
  - Vertical probing using COBRA technology.

Wafer Test Time vs. # of sites



Cost of Test Reduction at STMicroelectronics

- Overall global gain ratio compared to single site
  - Wafer sort > 3
  - Final Test > 2
- COTRED objective exceeded: COT reduced by 70%

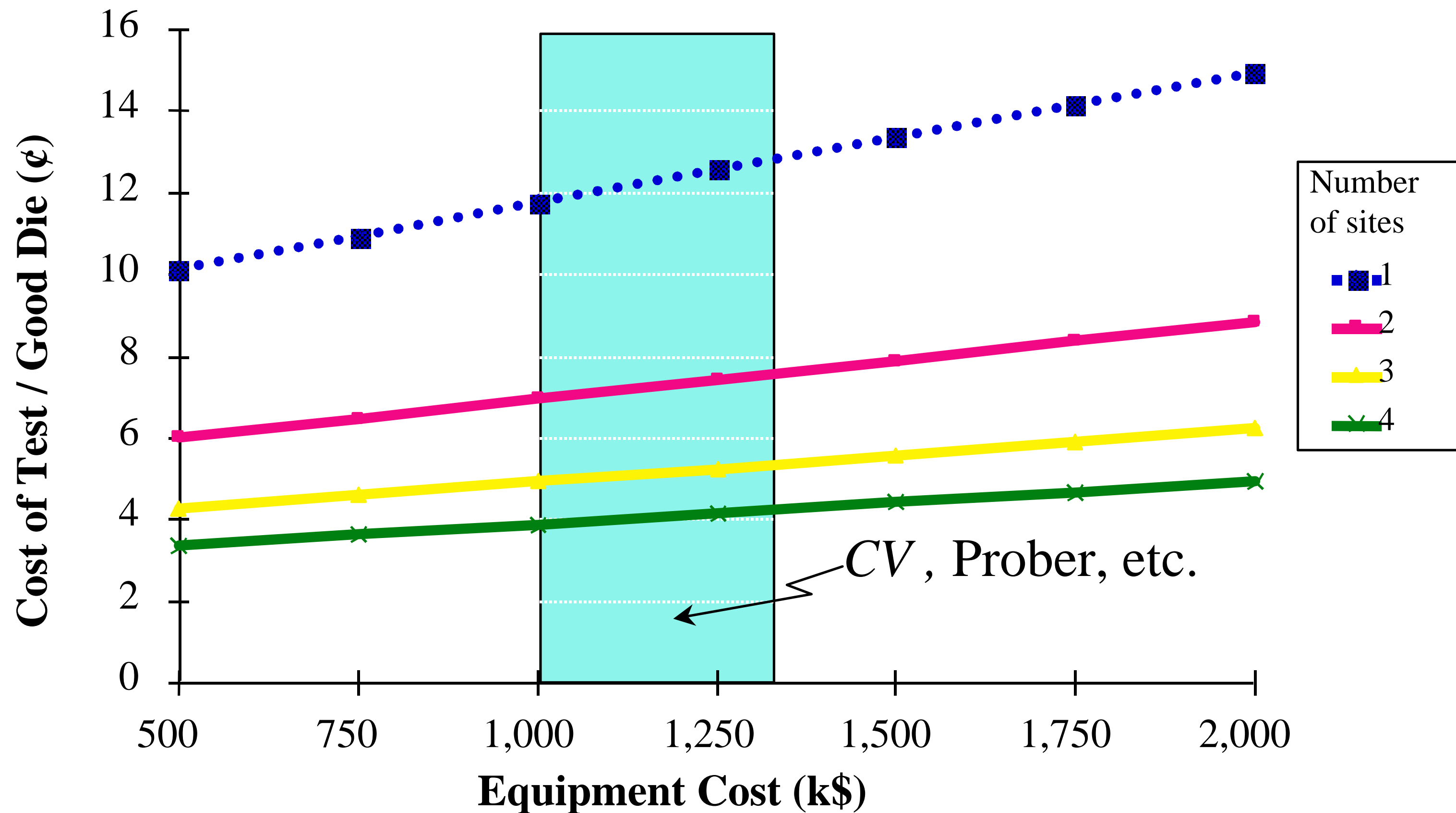


ITS 9000*CV* features

- Parallel by 16
  - 8 per test head
  - 2 test heads simultaneously
- Parallel test program
  - Automatic transfer from single test program
- All tests (DC, ftest, APG scan, match, DAC/ADC) can be executed in parallel.
- Full compatibility with ITS9000 Family.
- Meets COTRED objectives

Key for Cost of Test Reduction

Sensitivity: COT vs ATE cost, # of sites



Conclusion

- The only effective way to reduce the cost of Test is to maximize parallel capability.
  - not only software but also hardware
  - all test features must be in parallel

Future of Parallel Test

- The number of test sites will increase (tester, prober, handler, probe card)
- More parallel resources