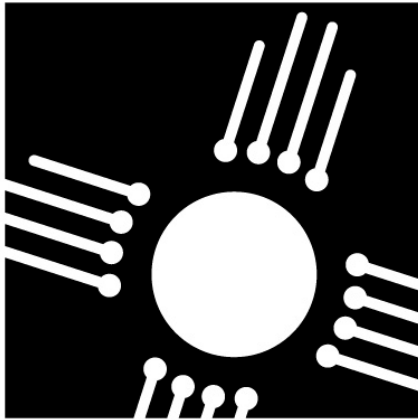
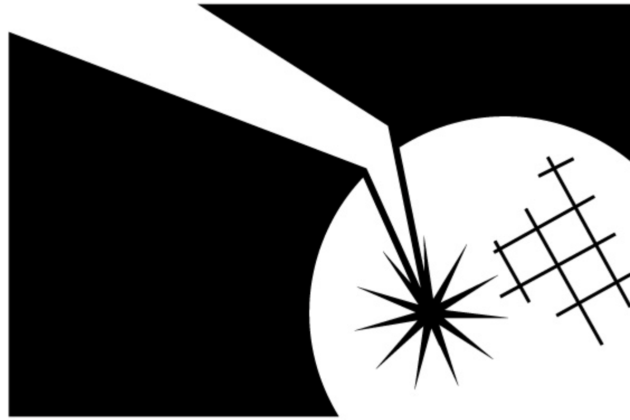
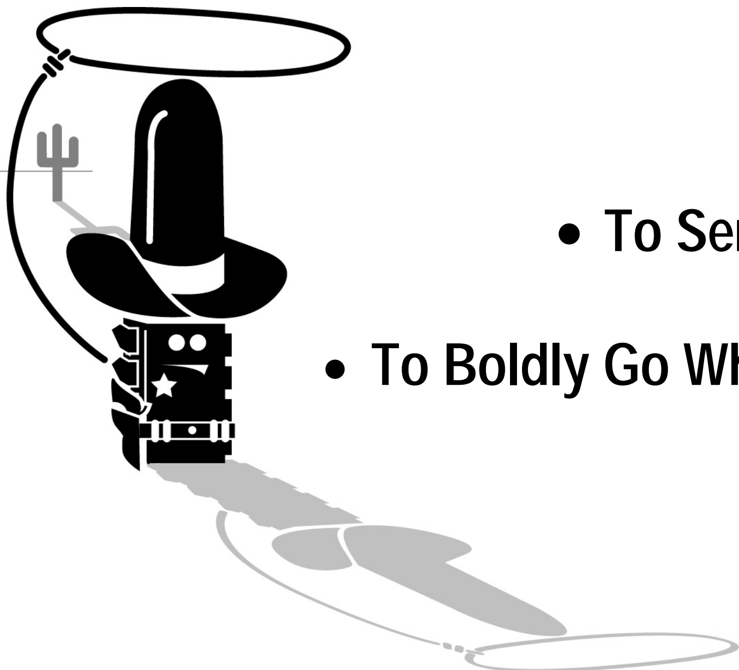



SOUTHWEST TEST WORKSHOP



- To Advance Wafer Testing Technology
- To Serve and Inform the Wafer Test Professional
- To Boldly Go Where No Other Workshop Has Gone Before

June 6 – 9, 1999
San Diego, CA. USA

Visit our Website at "www.swtest.org"

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What is a Test Workshop?

- It's Not a Theoretical or Academic Conference
- Workshops are Informal and Casual
- Provides Practical Solutions to Real Problems
- Mixture of Vendor and User Presentations
- Open Discussions and Networking
- Opportunity for Informal and Casual Interactions

INFORMAL INTERACTION

- Long Breaks….Talk with a Stranger
- Three Hosted Cocktail Receptions
- Extensive Social Activities
  - Barefoot Bar Trivia Contest
  - Ice Cream Sunday Contest
  - Miniature Golf Tournament
  - Scripps Aquarium
  - Mission Bay Cruise

PRIZES, PRIZES, AND MORE PRIZES

- **Best Technical Presentation**
- **Best Data Presented**
- **All Panel Members**
- **Best Questions Asked**
- **A Few Surprise Awards**
- **Tuesday Awards Banquet**
- **All Presenters on Wednesday**

TEST TECHNOLOGY PERIODICALS

- International Test Conference Proceedings
  2000 L Street, N.W., Suite 710
  Washington, D.C. 20036

- Test Technology Technical Committee
  Newsletter
  1474 Freeman Drive
  Amissville, VA 20106

- Journal of Electronic Testing
  Kiuwer Academic Publishers
  101 Philip Drive
  Norwell, MA 02061

  Design and Test of Computers - IEEE Computer Society
  10662 Los Vagueros Circle
  P.O. Box 3014
  Los Alamitos, CA 90720-1314

- Final Test Report
  Ikonix Corporation
  P.O. Box 1938
  Lafayette, CA 94549

- Evaluation Engineering
  Nelson Publishing
  2504 N. Tamiami Trail
  Nokomis, FL 34275-3428

IEEE Computer Society

TTTC: Test Technology Technical Council

PURPOSE: The Test Technology Technical Council (TTTC) is a volunteer professional organisation sponsored by the IEEE Computer Society. The goals of TTTC are to contribute to member's professional development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the art. All activities are led by volunteer members.

MEMBERSHIP: TTTC membership is open to all individuals interested in test engineering at a professional level. In addition to the benefits of personal association with other test professionals and the opportunity to serve on a wide range of committees, members receive TTTC Newsletters and announcements.

DUES: There are NO dues for TTTC membership and no parent-organisation membership requirements; however there are substantial reductions in fees for TTTC-sponsored meetings and tutorials for members of IEEE and/or IEEE Computer Society (IEEE and IEEE/CS do have member fees).

NEWSLETTER: Every year TTTC publishes four issues of its newsletter embedded in the magazine IEEE Design & Test of Computers. In addition TTTC publishes several issues of a more comprehensive newsletter that is mailed to all members. The newsletter covers current issues in test, TTTC technical activities, standards, technical meetings, etc.

STANDARDS: TTTC initiates nurtures and encourages new test standards. TTTC-initiated Working Groups have produced numerous IEEE standards, including the 1149 series used throughout the industry.

TECHNICAL ACTIVITIES: TTTC sponsors a number of Technical Activity Committee (TACs) that address emerging test technology topics. TTTC TACs guide a wide range of activities in these topic areas.

TECHINCAL MEETINGS: TTTC sponsors several well-known conferences and symposia and holds numerous regional and topical workshops to spread technical knowledge and advance the state-of-the art.

TUTORIALS and EDUCATION: TTTC sponsors a comprehensive *Test Technology Educational Program (TTEP)*. This program provides opportunities for design and test professionals to update and expand their knowledge base in test technology, and earn official accreditation from IEEE TTTC, upon the completion of four full day tutorials offered by TTEP. TTEP tutorials are held in conjunction with ITC, VTS, ATS, ETW, and DFTS.

TTTC On-Line: The TTTC Web Site at http://computer.org/tttc offers samples of the TTTC Newsletter, information about technical activities, conferences, workshops and standards, and link to the Web pages of a number of TTTC-sponsored technical meetings.

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IEEE 1450 - (STIL)	**Gregory MASTON**	Fluence	gregm@fluence.com
	Tony TAYLOR	Fluence	tonyt@fluence.com
IEEE P1500	**Yervant ZORIAN**	LogicVision, Inc.	zorian@logicvision.com
IEEE P1532	**Neil JACOBSON**	Xilinx Corp.	neil.jacobson@xilinx.com

TTTC sponsored Technical Meetings in 1999

Date	Meeting	Location	Contact
Feb 23-26	***Pacific Northwest Test Workshop***	Botega Bay, CA - USA	E. J. McCLUSKEY
Feb 28 - Mar 02	***TWS'99 German Workshop***	Potsdam - Germany	H. T. VIERHAUS
Mar 9-12	***D.A.TE'99***	Munich - Germany	R. ERNST
Mar 22-24	***Test Synthesis Workshop***	Santa Barbara, CA - USA	R. C. AITKEN
Mar 30 - Apr 01	***Design, Test of MEMS/MOEMS***	Paris - France	B. COURTOIS
Apr 25	***IDDQ Testing Mini-Workshop***	Dana Point, CA - USA	Y. K. MALAIYA
Apr 25-29	***VLSI Test Symposium***	Dana Point, CA - USA	M. NICOLAIDIS
Apr 28-29	***Testing Embedded Cores Workshop***	Dana Point, CA - USA	Y. ZORIAN
May 19-21	***Signal Propagation Workshop***	Titisee-Neustadt - Germany	J. P. MUCHA
May 25-28	***European Test Workshop***	Constance - Germany	H.-J. WUNDERLICH
May 27-28	***North Atlantic Test Workshop***	West Greenwich, RI - USA	J.-C. LO
Jun 06-09	***Southwest Test Workshop***	San Diego, CA - USA	W. R. MANN
Jun 15-18	***Mixed Signal Testing Workshop***	British Columbia - Canada	A. IVANOV
Jun 16-18	***Rapid System Prototyping***	Clearwater, FL - USA	R. LAUWEREINS
Jul 05-07	***On-Line Testing Workshop***	Rhodes - Greece	M. NICOLAIDIS
Aug 05-06	***VLSI Design & Test Workshops***	New Delhi - India	C. P RAVIKUMAR
Aug 09-10	***Memory Test Workshop***	San Jose, CA - USA	R. RAJSUMAN
Aug 17-22	***Computer Science Conference***	Yerevan - Armenia	Y. SHOUKOURIAN
Sep 06-08	***Electronic Systems Conference***	Bratislava - Slovakia	D. DONOVAL
Sep 12-15	***High Density Module Test VI***	Napa, CA - USA	R. J. WAGNER
Sep 15-17	***Known Good Die Industry Workshop***	Napa, CA - USA	L. GILG
Sep 28-30	***International Test Conference***	Atlantic City, NJ - USA	M. TOPSAKAL
Sep 30 - Oct 01	***Production Test Automation Workshop***	Atlantic City, NJ - USA	A. P. AMBLER
Sep 30 - Oct 01	***Microprocessor Test Workshop***	Atlantic City, NJ - USA	M. S. ABADIR
Sep 30 - Oct 01	***System Test and Diagnosis Workshop***	Atlantic City, NJ - USA	R. W. SIMPSON
Oct 04-06	***Thermal Investigations of ICs Workshop***	Rome - Italy	B. COURTOIS
Oct 25-27	***1999 DAK Forum***	Trondheim - Norway	E. J. AAS
Nov 01-03	***Defect & Fault Tolerance Symposium***	Albuquerque, NM - USA	C. METRA
Nov 04-06	***High-Level Design Validation Test W.***	San Diego, CA - USA	A. ORAILOGLU
Nov 16-18	***Asian Test Symposium***	Shanghai - China	B. M. Y. HSIAO

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Southwest Test Workshop
Technical Program

Sunday - June 6, 1999 - 2:00pm

Tutorial

"Probe Card Evaluation Process"

Dave Unzicker

Intel Corporation, FM3-25

1900 Prairie City Road

Folsom CA, 95630

(916) 356-6156

david.e.unzicker@intel.com

Southwest Test Workshop
Technical Program

Monday - June 7, 1999 - 8:30am

Vertical Probing

"Overview of C4 Area Array Probing"
Justin Leung, Ph.D. - Intel Corp.

"Modeling the Array Force in C4 Probe-Cards During Wafer Sort"
Arun Ramamoorthy and **Rahima K. Mohammed** - Intel Corp.

"Advances in Performance of Buckling Beam Probes"
Dean Gonzales - Intel Corp.
January Kister - Probe Technology

Southwest Test Workshop
Technical Program

Monday - June 7, 1999 - 10:30am

Probe Card Cleaning

"Low C_{RES} with Reduced Cleaning…A Paradigm Shift"

Jerry Broz, Ph.D. - Advanced Probing Systems, Inc.

Rey Rincon - Texas Instruments Corp.

"Membrane Cards with Microscrub Technology"

Ken Smith - Cascade Microtech, Inc.

"EHD (Electro-hydrodynamic) for Cleaning Probe Cards"

James Andersen - Applied Precision, Inc.

"Form Factor's No-Clean Probe Card Technology"

Mark Brandemuehl - Form Factor, Inc.

Southwest Test Workshop
Technical Program

Monday - June 7, 1999 - 1:00pm

Full Contact Wafer Probe and Burn-In

"WLBI and Test System Considerations"

Mark Carbone - Aehr Test Systems

"Full Wafer Burn-In and Test"

John Mosko and **John Budnaitis -** W.L. Gore

"Wafer-On-Wafer Technology for WLBI"

Dave Pedersen - Form Factor., Inc.

Southwest Test Workshop
Technical Program

Tuesday - June 8, 1999 - 8:00am

Probe Potpourri

"Introduction of the X32 Test in IBM Essonnes France"

Dominique Langlois - IBM Essonnes

"Advances in Conventional Cantilever Probe Cards"

Krzysztof Dabrowiecki - Probe Technology

"Effects of Lower Force Interfacing Solutions on Wafer-Test Systems"

Mark Wojcik - CerProbe Corp.

Southwest Test Workshop
Technical Program

Tuesday - June 8, 1999 - 10:00am

<u>Analyzer to Probe Mark Correlation</u>

"Can I Correlate My Probe Card"
Heather McGill and **Nasser Ali Jafari** - Intel Corp.

"Probers as the Primary Metrology Tool"
Dia Dee Casavant - Electroglas

"Statistical Approach to PCA Correlation/Comparison"
Larry Cowart - Adaptec and **Hank Scutoski** - CerProbe Corp.

"A Study of the Probing Process"
John Strom - Applied Precision, Inc.

"Analyzer-Prober Correlation"
Rod Schwartz - Integrated Technology Corp.

Southwest Test Workshop
Technical Program

Wednesday - June 9, 1999 - 8:00am

SEMI Standards Activities

"Overview of SEMI Standards Activities"

Bettina Weiss - SEMI

"Automatic Prober Headplate/Ring Carrier Standardization"

Jim Anderson - CerProbe Corp.

"Probe Card Correlation Task Force"

Roger Sinsheimer - Xandex
Bill Knauer - Keithley Instruments

"Wafer Map Standards"

Dave Huntly - Kinesys Software Inc.

Southwest Test Workshop
Technical Program

Wednesday - June 9 ,1999 - 10:00am

New Probe Technology

"The Necessities Of New Probe Card Technologies"
Frank.Pietzchmann - Infineon GmbH

"Vertical Scrub Probe Card"
Mark Godfrey - Prime Yield Systems Inc.

"Microstrip Beam Technology Update"
Lynn Saunders - MicroConnect, Inc.
Rey Rincon - Texas Instruments Corp.

"J-Probe System"
Joe Mai - JEM America