Overview of C4 Array Probing

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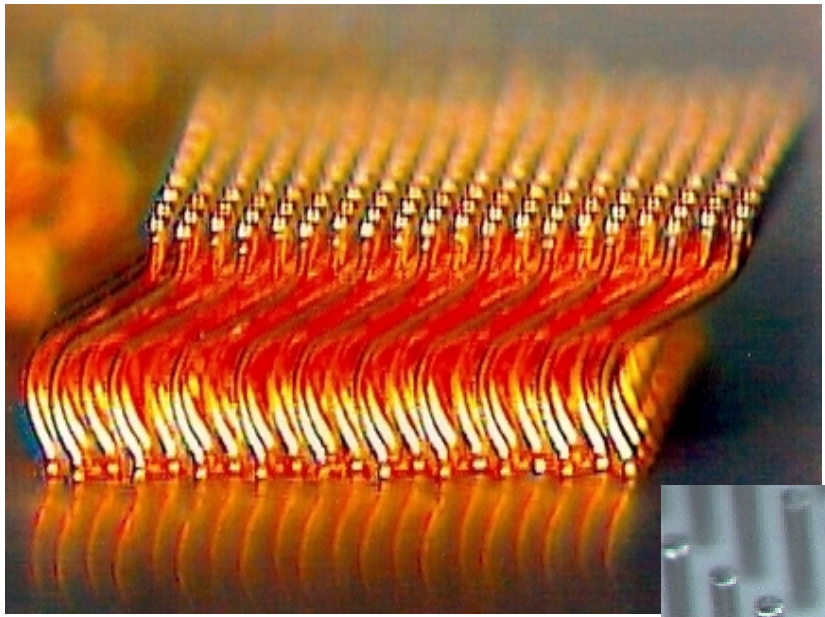
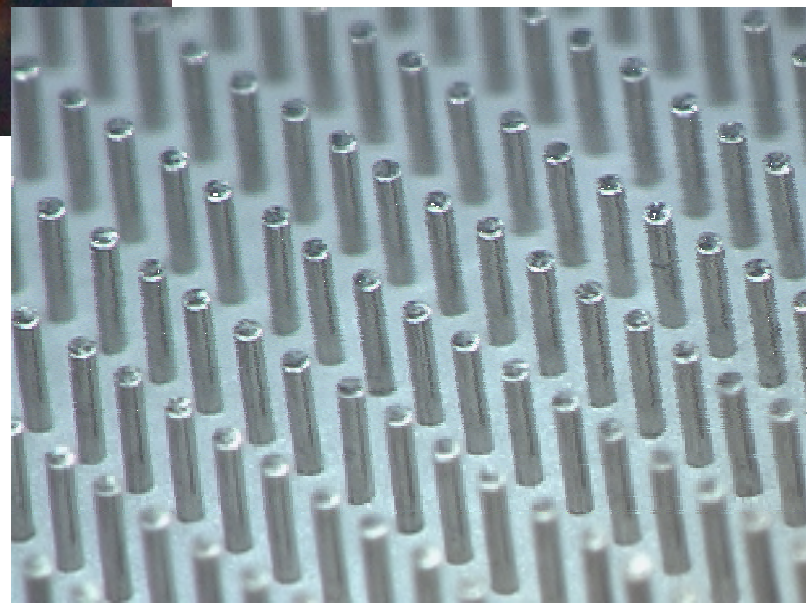
OUTLINE

- C4 probing technologies
- C4 probecards
- Electrical and Mechanical Characterization
- Process Integration challenges
- Future requirements

C4 Probing Technologies at Intel

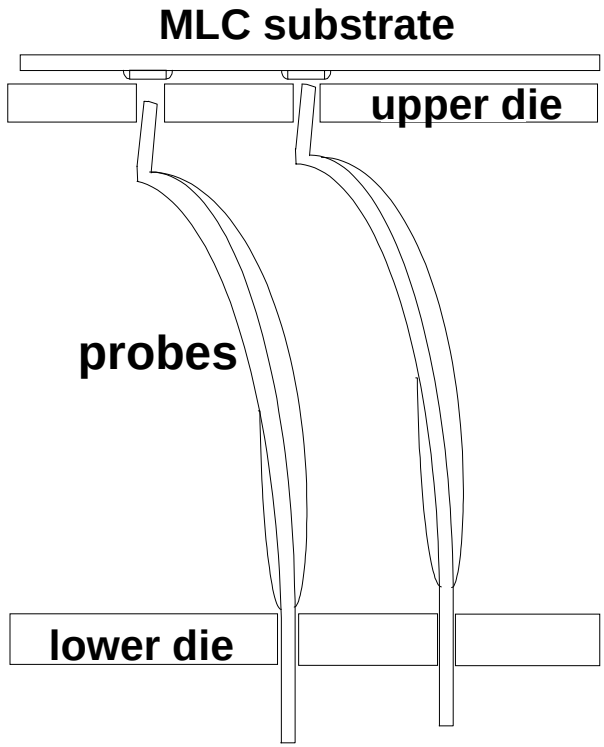


Resilient Contact Technology



Buckling Beam Technology

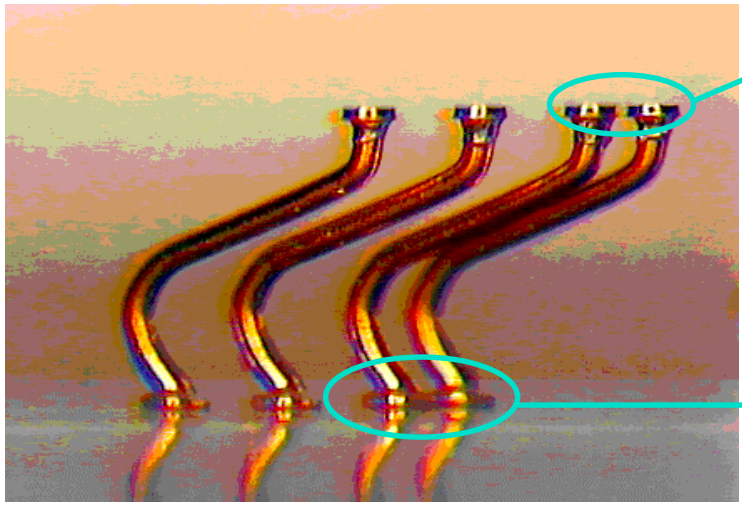
Buckling Beam Probes



Typical characteristics:

- precision die drilling, manual assembly
- 4-mil diameter, 225-mils length probes
- Paliney-7 or BeCu probes
- 1-mil alignment, 3-mils planarity, 2.5-3g/mil force,
- probe replacement, head interchangeability

Resilient Contact Probes

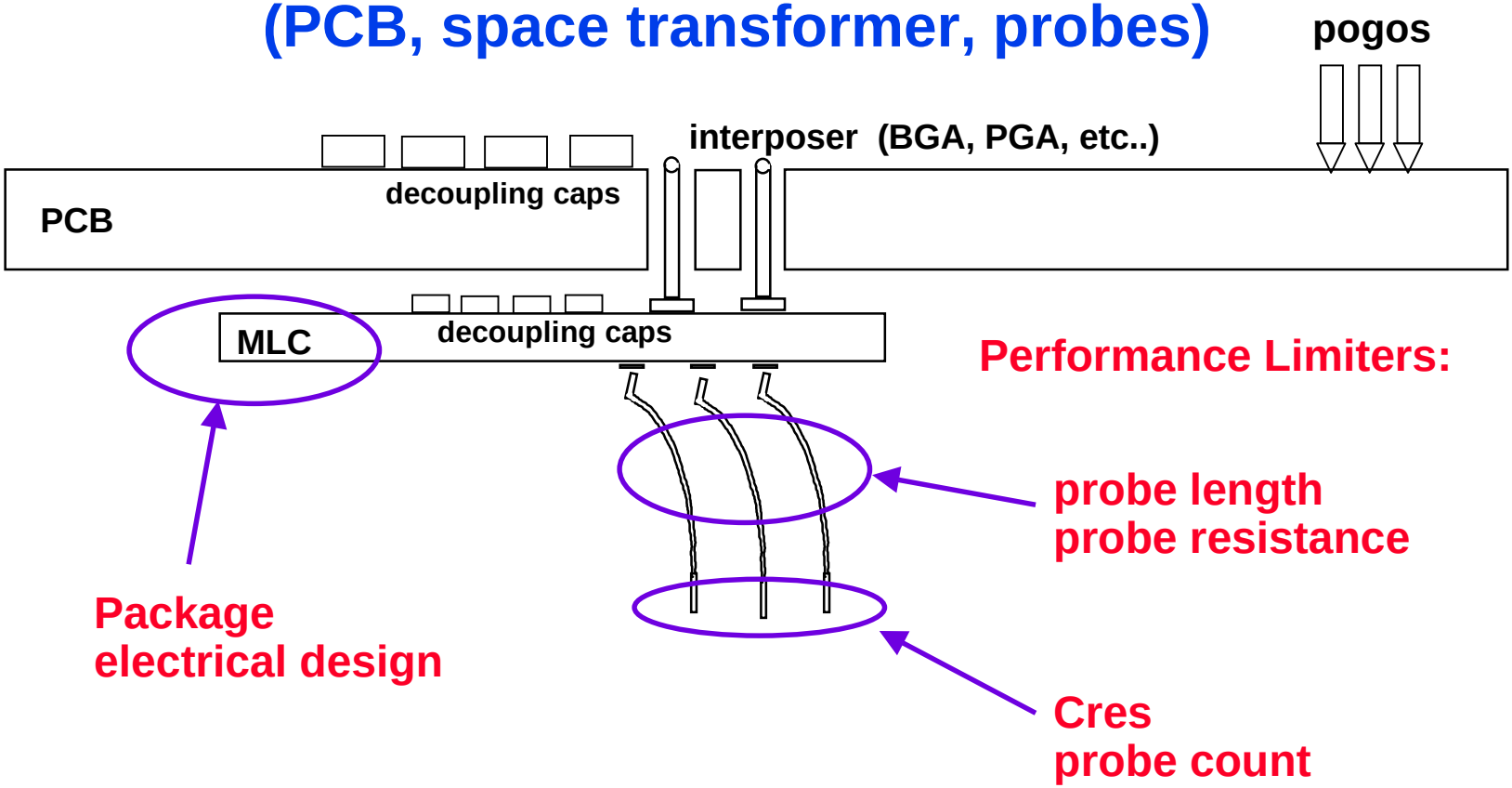


Typical characteristics:

- plated gold core springs with custom tip geometry
- 5-mil tip diameter, 70-mil length probes
- 13-um alignment, 13-um planarity, 1.2-3.0 g/mil

C4 ProbeCard Cross-section

(PCB, space transformer, probes)



Electrical Characterization & Modeling

DC Electrical characterization:

- Probe max current capability
- Pwr/Gnd DC resistance

AC Electrical characterization:

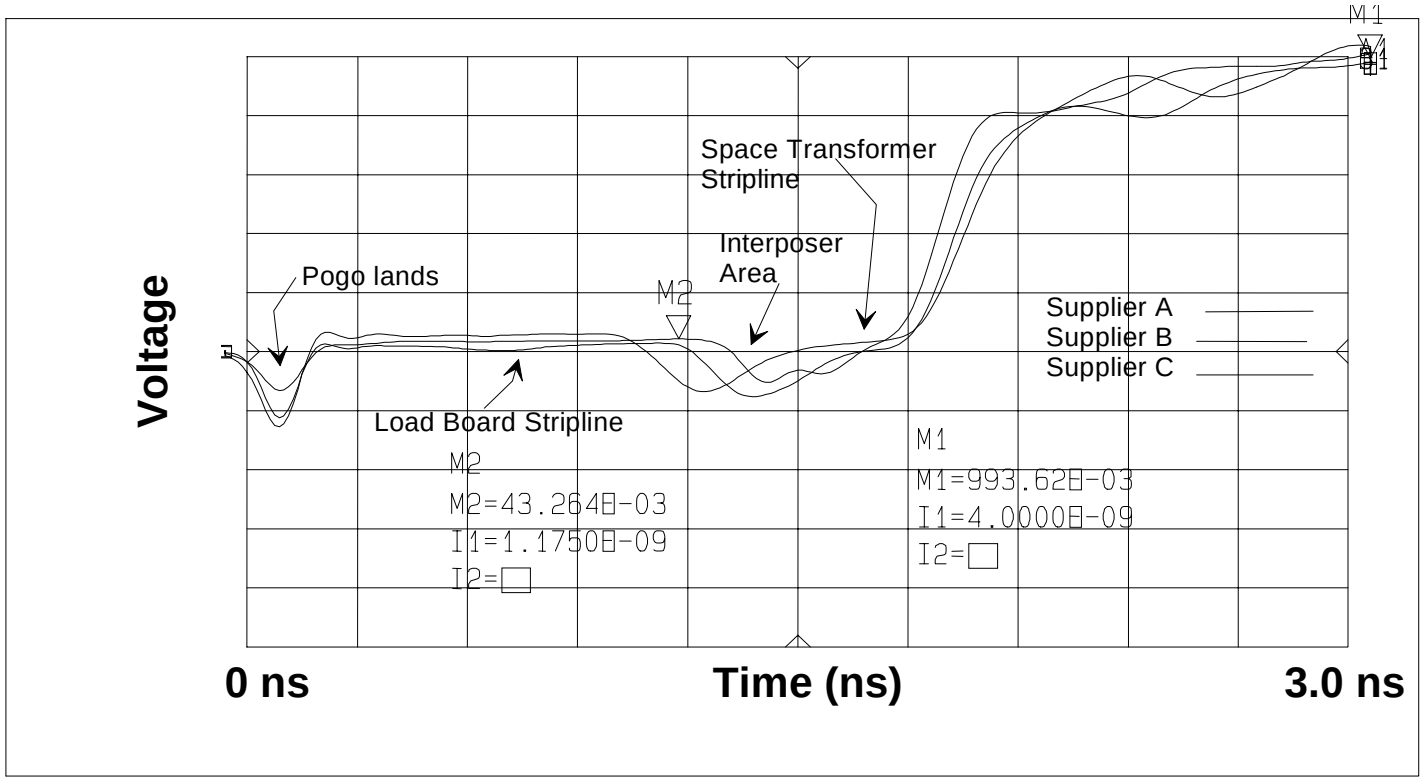
- TDR characterization
- Network analyzer measurements
- MDS and HFSS circuit modeling
- High speed current switch “Slammer” which switches

  40 Amps in 5 ns to simulate DUT VCC turn-on transient.
- Measured performance matched model within 10%.

➡ **Power Integrity system design is the key challenge.**

Requires accurate knowledge of product specs, power supply performance, component parasitics, etc..

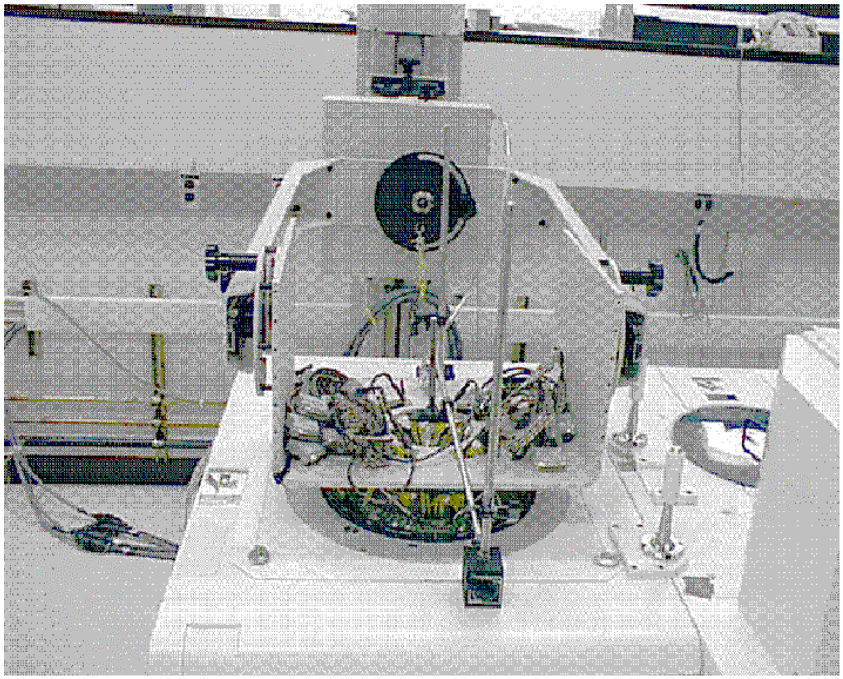
AC Characterization



C4 probecard bandwidths in the range of 1.3-1.5 GHz.

Bandwidth limiters include pogo interface, interposer, and probes.

Mechanical Characterization



S9k testhead emulator and test system:

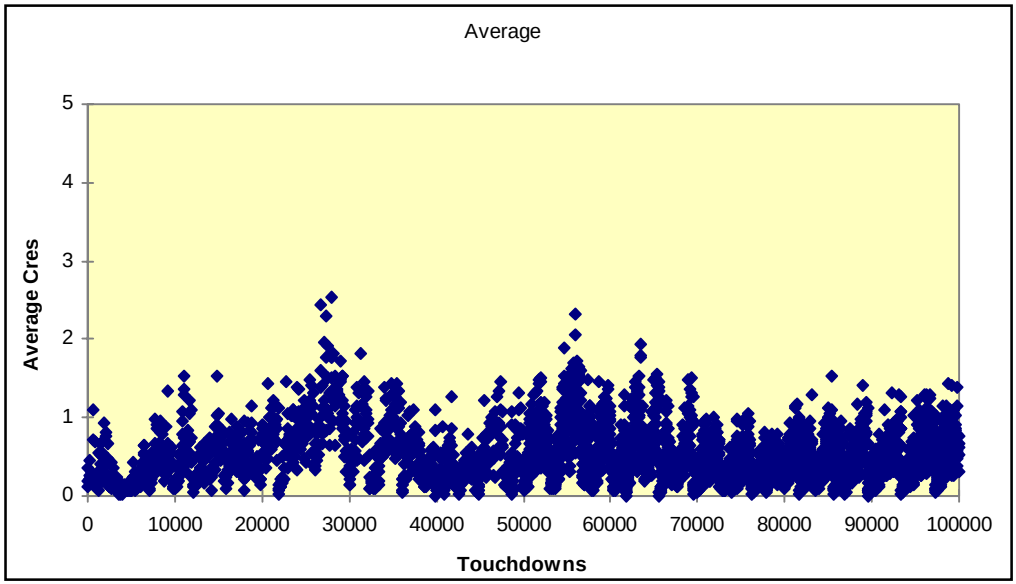
- **Sort Process development**
- **Probecard mechanical characterization.**

Experiments include:

- **Cres experiments**
- **Lifetime robustness studies**
- **PCB, chuck and probe deflection characterization**
- **Array force measurements**

  (single probe measurements inadequate)

Cres Results

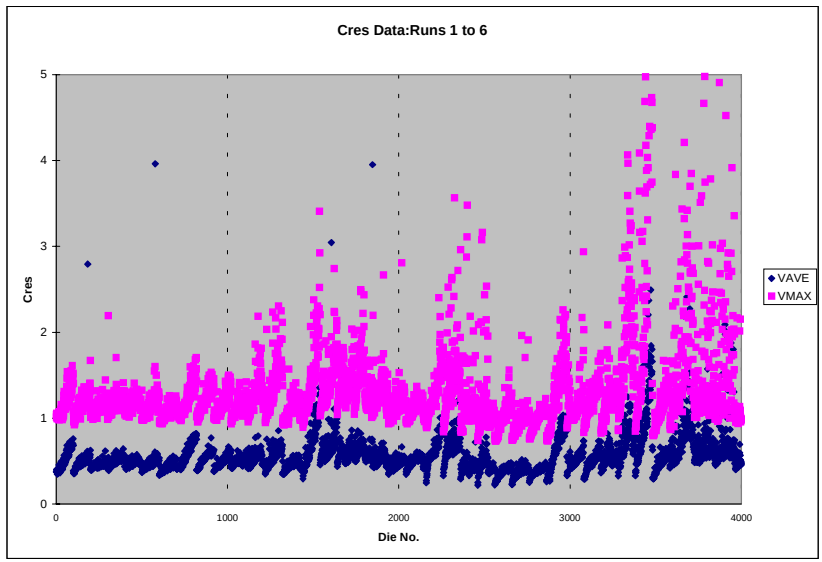


During process development,

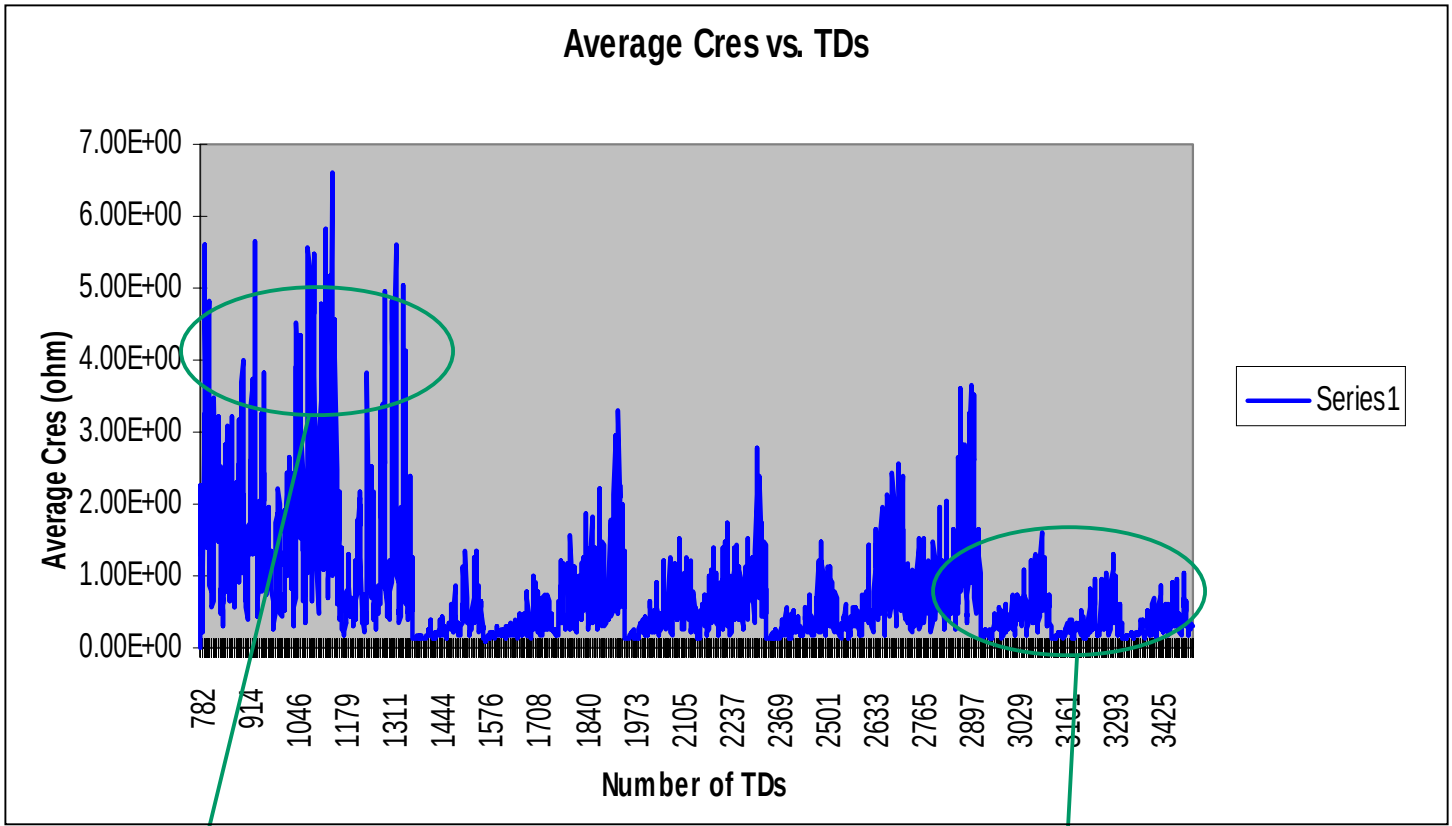
Cres serves as chief sort process health monitor during development.

Bin-switch criteria takes over once silicon is available.

Monitor both average and maximum Cres.



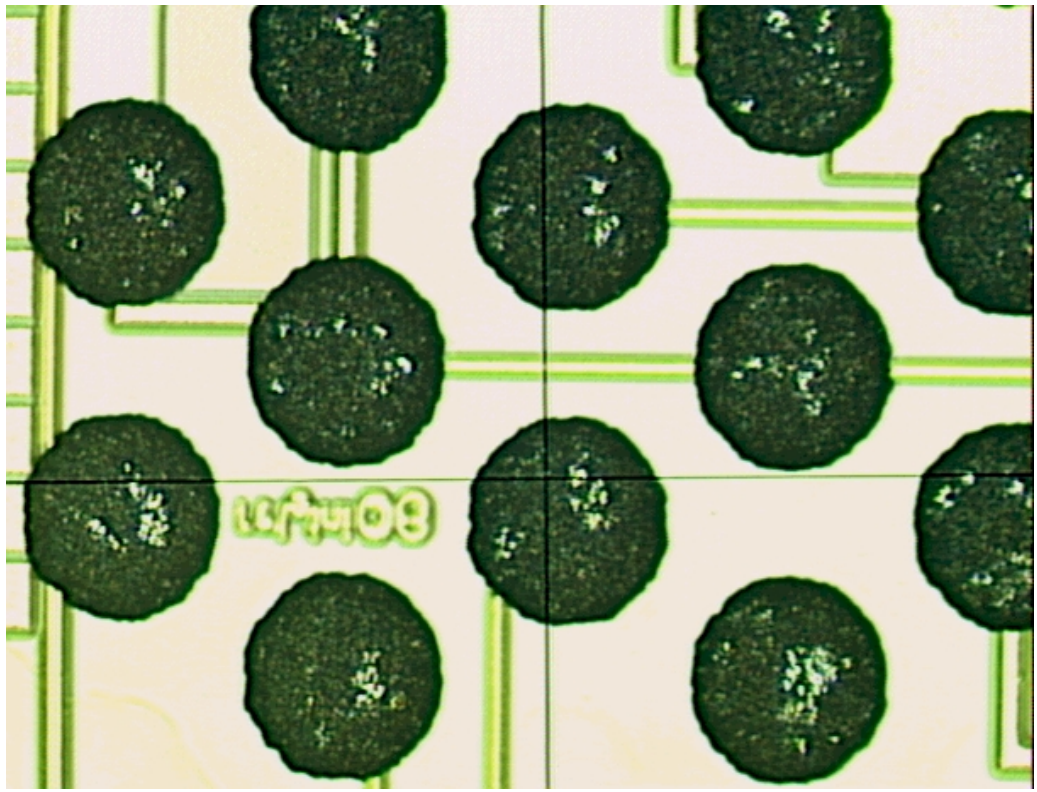
Cres Optimization



Sort recipe #1

Sort Recipe #2

Bump Impact

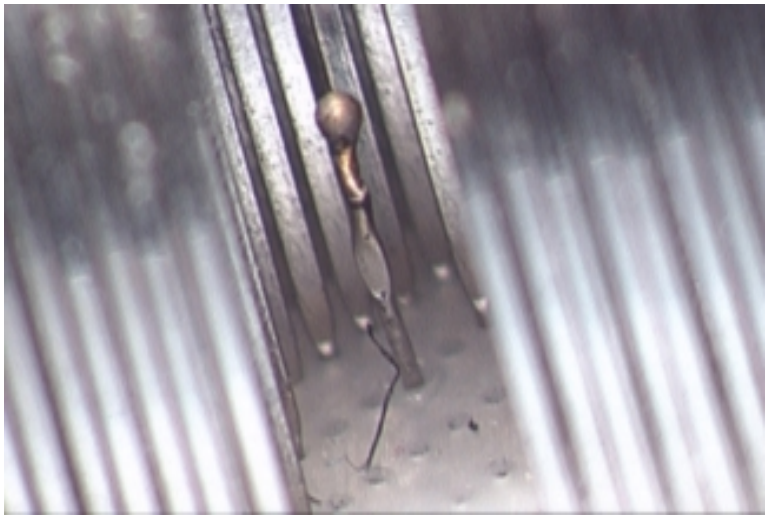


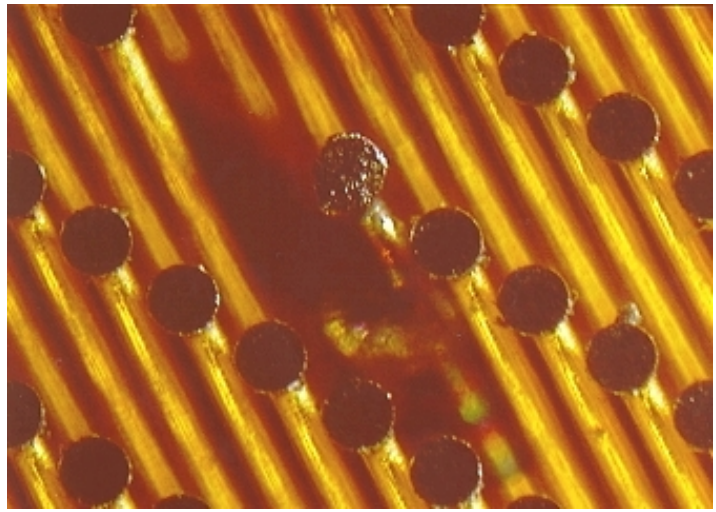
Bump alignment and impact marks generally not a problem.

Process Integration Considerations

- **Prober**
  - -- PTPA recognition
  - -- PTPA robustness
  - -- scrub plates
  - -- chuck force / deflection
- **Sort Process**
  - -- clean recipe optimization
  - -- OT optimization
  - -- bump interaction
  - -- bump defects
- **Probecard Repair**
  - -- offline PM procedures
  - -- repair processes
- **Metrology**
  - -- crash protection
  - -- tip recognition
  - -- supplier matching

Burnt Probes





Burnt probes was key manufacturing issue early on.

Addressed on several fronts:

- **bin limit triggers**
- **testtape modifications**
- **bump defect inspection**
- **repair processes**
- **etc...**

Dual Technology

Currently, both technologies in HVM despite incompatible process recipes

Technology runoff resulted in high rates of improvement as competing teams leveraged sort process learnings.

Both technologies now in production on multiple sort floors.

Supplier selection criteria:

- **Manufacturing performance**
- **Manufacturing cost of ownership**
- **Next Generation Capability**
- **Supplier Health**
- **Second Sourcing**

Future C4 probing requirements

Trends:

- Higher DUT currents (>100 A)
- Lower Vcc (< 1 V)
- Severe di/dt transients (>50 A/ns)
- Power (>150 W)
- High speed clocks, Rambus
- Increasing Test Costs

Required Probecard Development:

- Higher probe counts
- Lower Cres
- Shorter probes
- Robust probes
- High performance chucks
- Microwave design techniques
- Parallel sort

Acknowledgements

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