Modeling the Array Force of C4 Probe Cards during Wafer Sort

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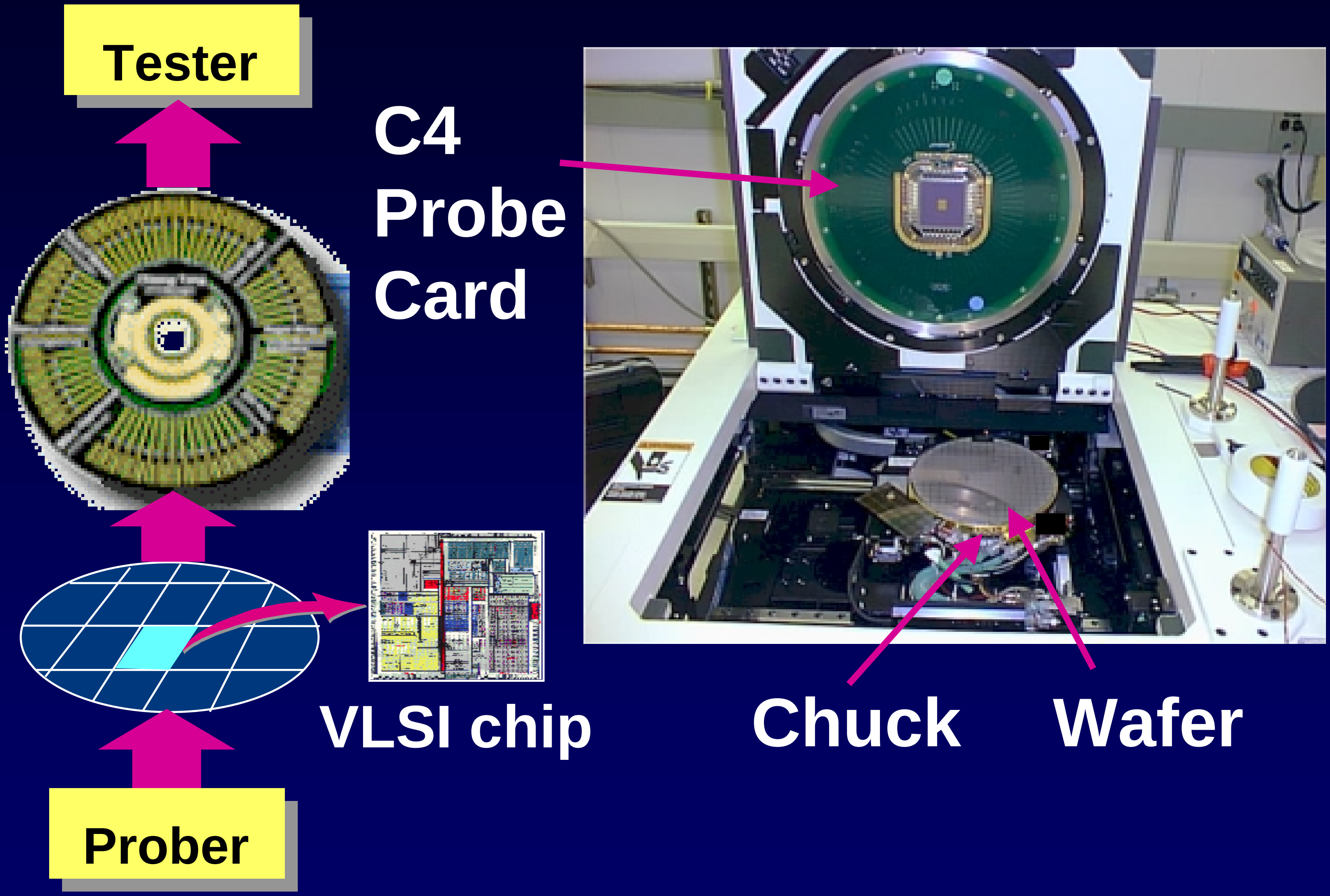
Overview

- Problem Definition
- System Model
  - PCB Deflection Model
  - Pro/E and Pro/Mechanica model
  - Chuck Deflection
- Model Validation
  - Pressure Paper and Load Cell
- Conclusions

Probe Card and the System



Tester

C4 Probe Card

VLSI chip

Chuck

Wafer

Prober

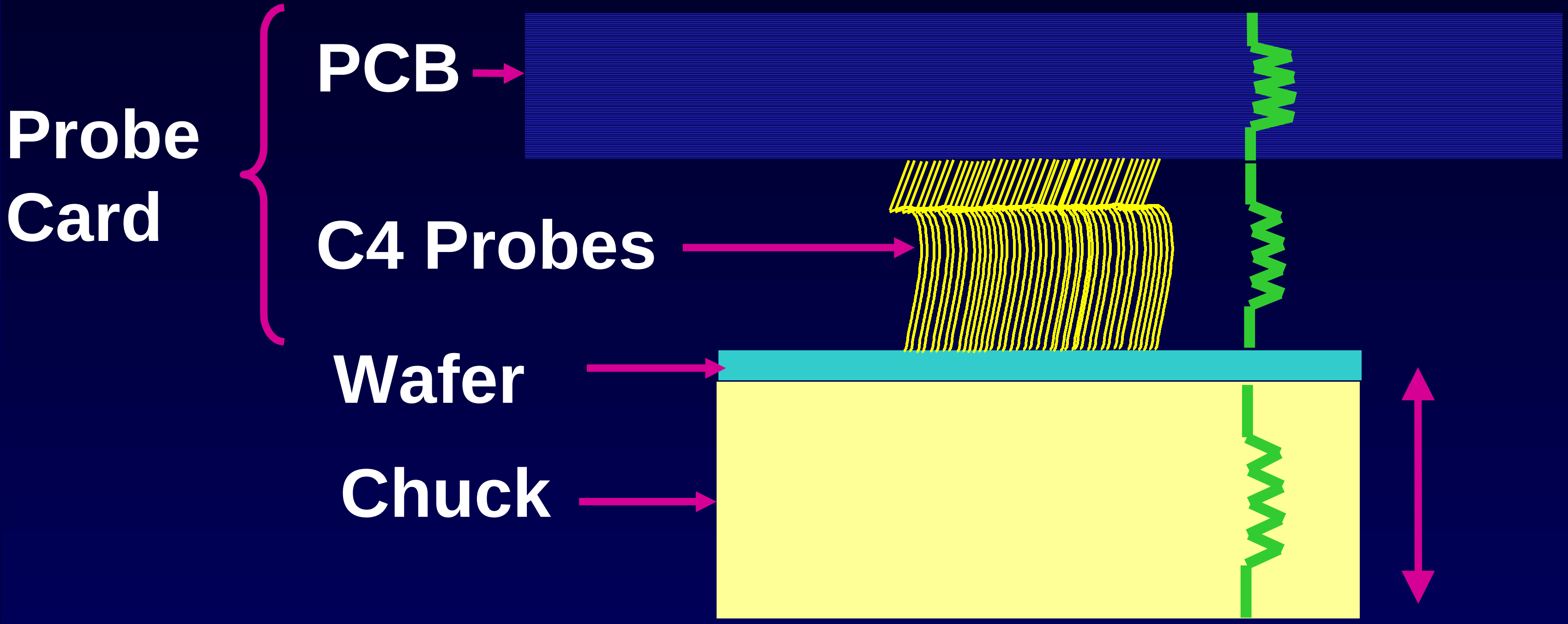
Contact Resistance and Model?

- Contact Resistance (Cres) is the resistance between the C4 bumps and the probes.
- High power requirements of the products require reducing Cres to achieve good electrical contact.
- Without good Cres - False Failures and Yield Reduction.
- Control variable over Cres is overtravel (OT).
- Overtravel (OT) required to achieve good Cres during wafer sort varied with the product probe count.

Why do we need a Model?

- Increase in probe count increases the array force exerted by the probes on the chuck.
- Normal contact force is due to the compression of the probes, it is critical to model the actual compression of the probes for an OT programmed (input) into the prober.
- Determine the array force on the chuck from the actual compression of the probes.

Schematic of the System



Probe Card

PCB

C4 Probes

Wafer

Chuck

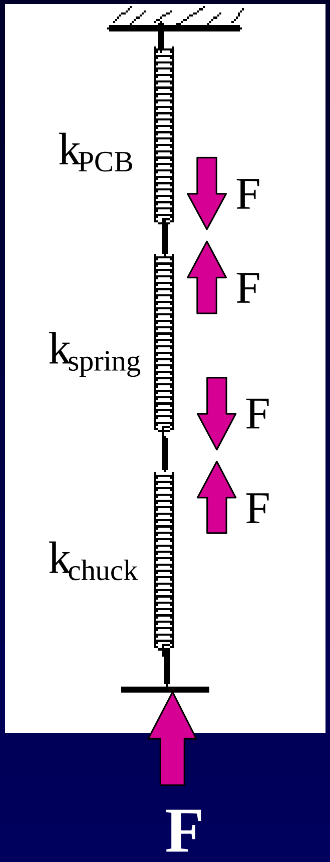
High power CPU sort requirements result in probe count increase and hence, increase in the array force.

System Modeling

- **PCB, Probes and Chuck treated as a system of springs in series (in equilibrium)**

$$\frac{1}{k_{system}} = \frac{1}{k_{chuck}} + \frac{1}{k_{springs}} + \frac{1}{k_{PCB}}$$

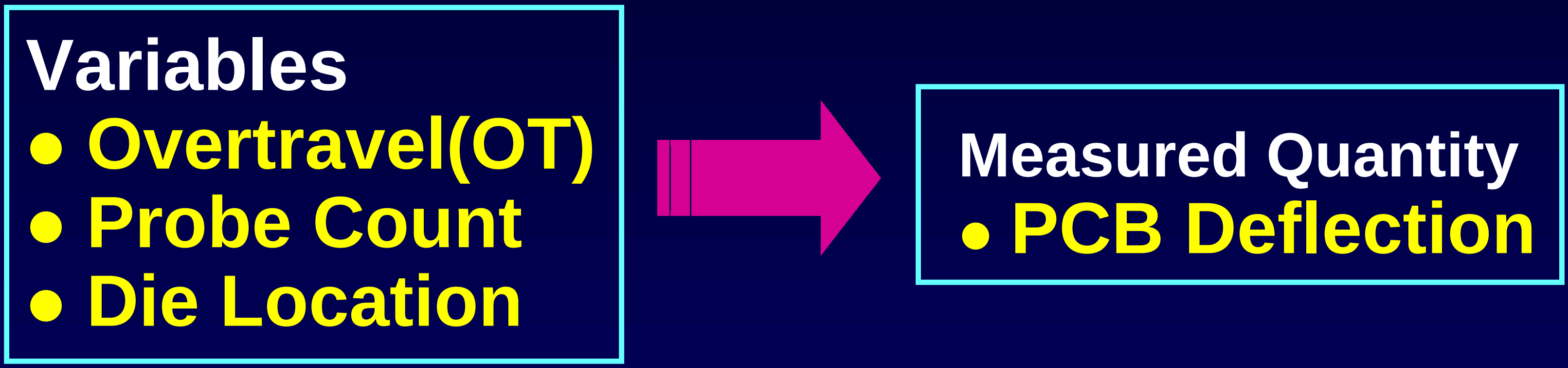
$$\frac{F}{k_{system}} = \frac{F}{k_{chuck}} + \frac{F}{k_{springs}} + \frac{F}{k_{PCB}}$$



- **Programmed OT = Chuck Deflection + Probe Compression + PCB Deflection**

Objective

Develop a model to predict the array force on the chuck for an overtravel programmed into the prober



Variables

- Overtravel(OT)
- Probe Count
- Die Location

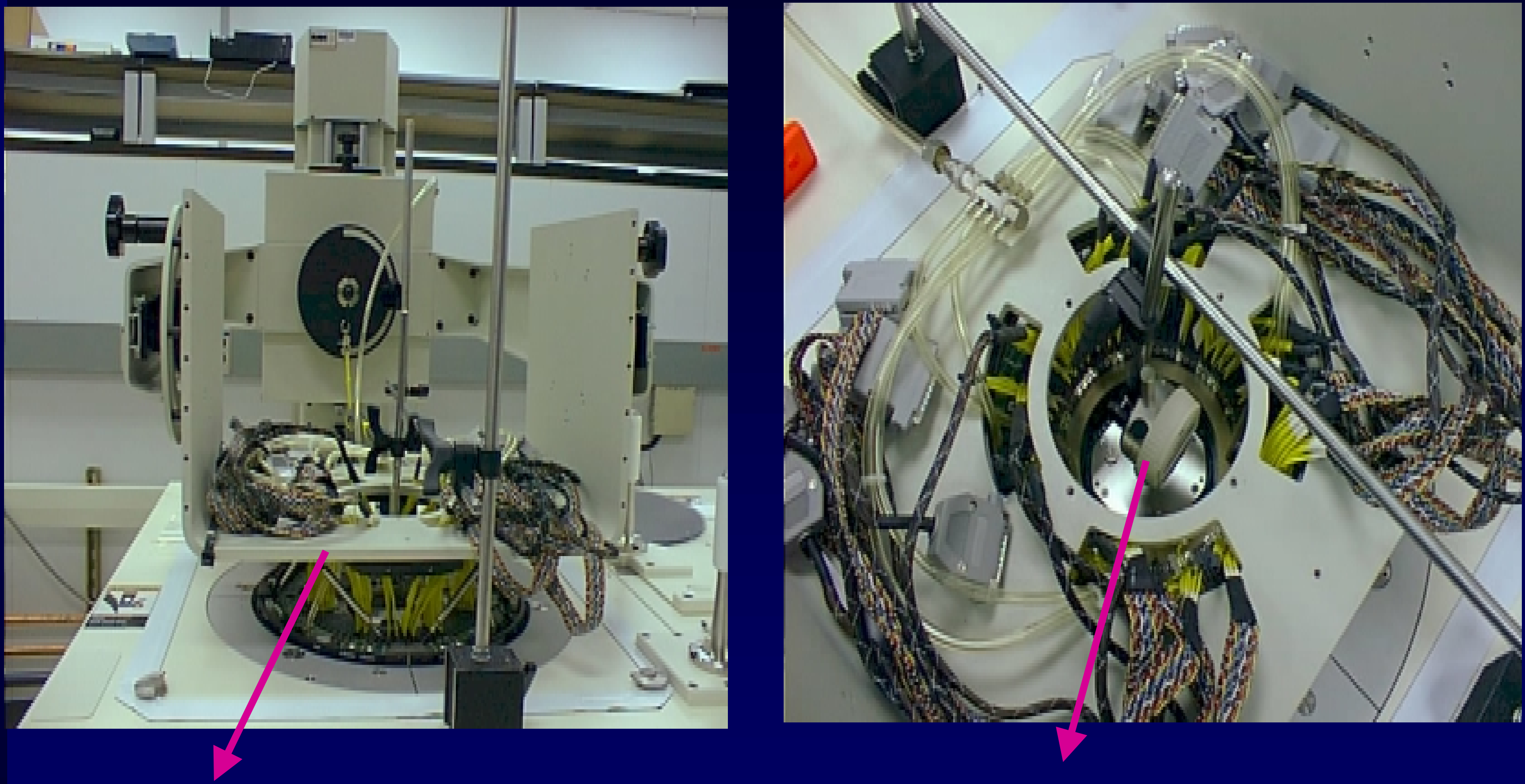
Measured Quantity

- PCB Deflection

Limitations

- Prober to prober variation (ITTO prober only)
- PCB to PCB variation
- Variation in k -value

PCB Deflection Expt. Setup



S9K Testhead Emulator

Dial Gage

Metrology Capability Study

- MCA done on dial gage used to measure PCB deflection (n=16 for accuracy evaluation, n=30 for repeatability study on known thickness samples)
  - Precision/Tolerance (P/T) of 0.21
- The chuck z-movement was verified to check for any bias in the z-movement.
  - Chuck z-movement linear with OT with a bias.

MCA Study (cont.)

- To obtain a baselines for the Std. Dev., 30 measurements of the PCB Deflection were taken on an Al wafer at 5 die locations each and 4 OTs at each location.
  - PCB Deflection linear with OT with a slope that varied based on the measured die location (due to variations in chuck deflection at different die locations).

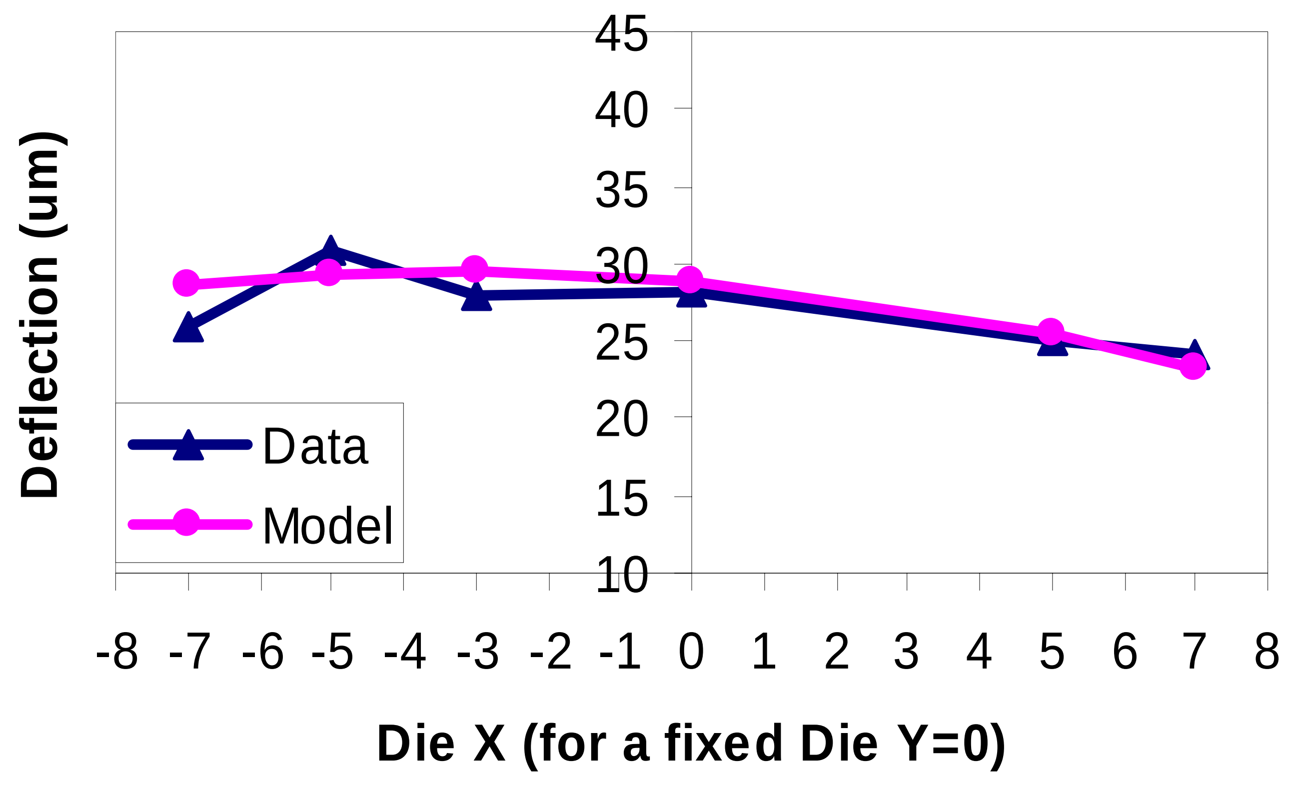
Experimental Design

- **Probe Count**
  - Started with C4 probe card and plucked sets of 200 probes.
- **Positional Dependence** (30 random die locations spread across the wafer).
- **Overtravel** (2 OT and 9 measurements per OT).

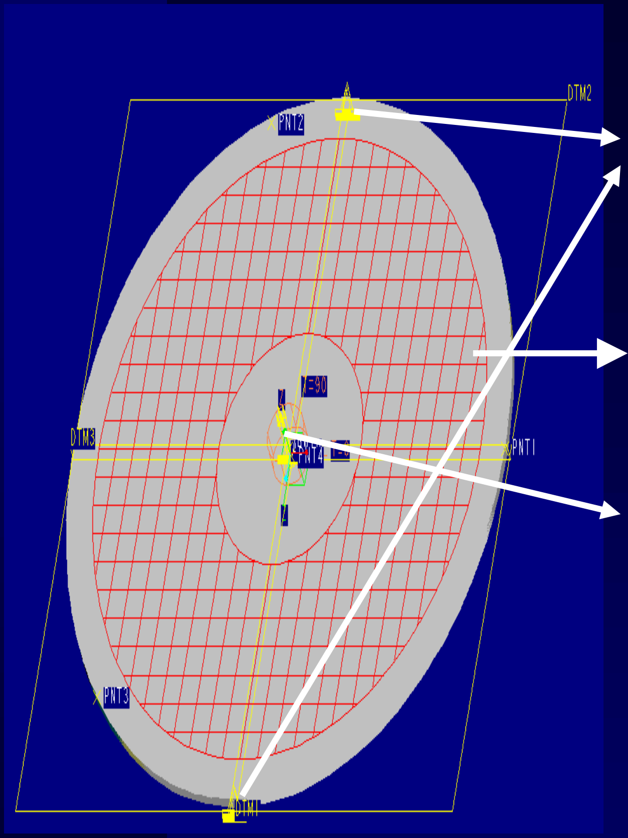
Analysis

- PCB deflection model by fitting the data using stepwise statistical regression analysis.
- Higher order effects (>2) were included in the model to start with and were dropped subsequently based on their significance level.
- The model was validated by collecting data with by removing another 100 probes from the C4 probe card.

Model Validation



Pro/E and Pro/Mechanica Model of the PCB

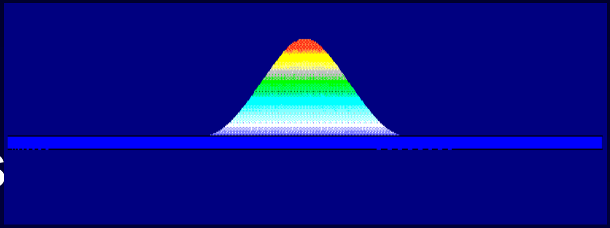


Constraints

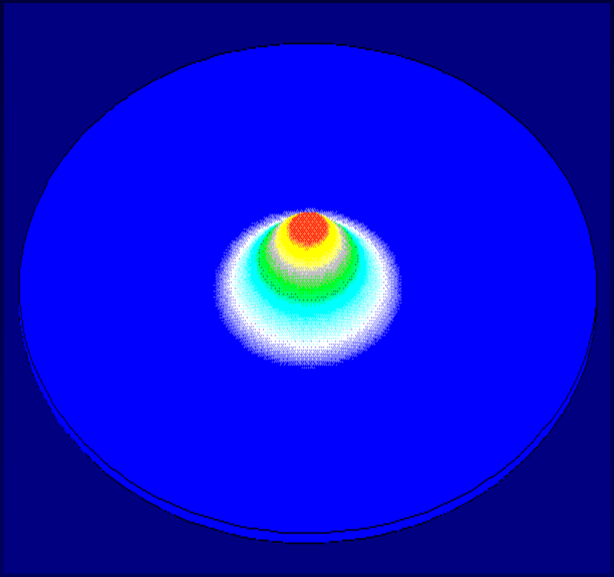
Test Head Emulator

Loads

Pro/E model



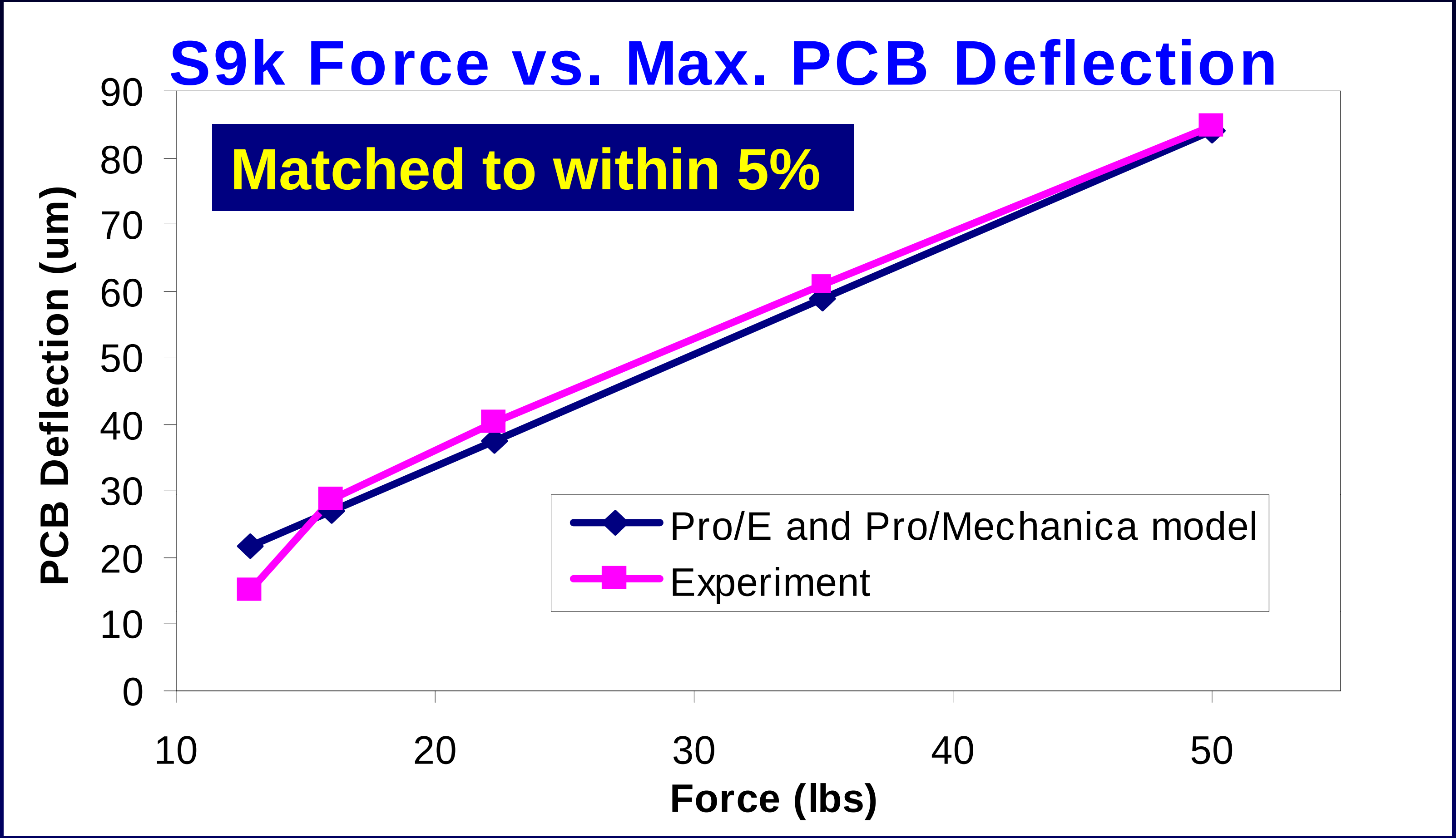
Side View



Isometric View

Pro/Mechanica Analysis of PCB Displacement Distribution

Empirical Model vs. FEM Model



PCB Deflection varied linearly with OT.

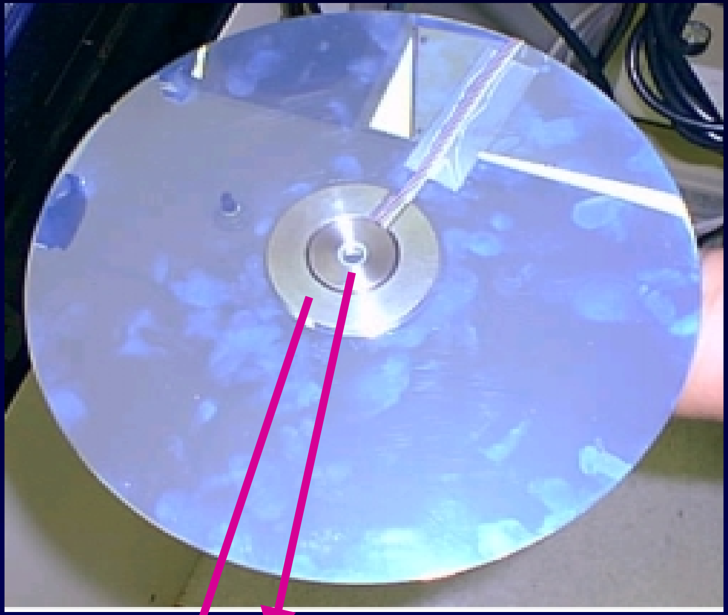
Chuck Deflection Modeling

- Prober parameters used to build a model for the chuck deflection
  - Chuck Deflection = f([X,Y], F,T); F = Force and T= Temperature

Model Validation by C4 array Force Measurements

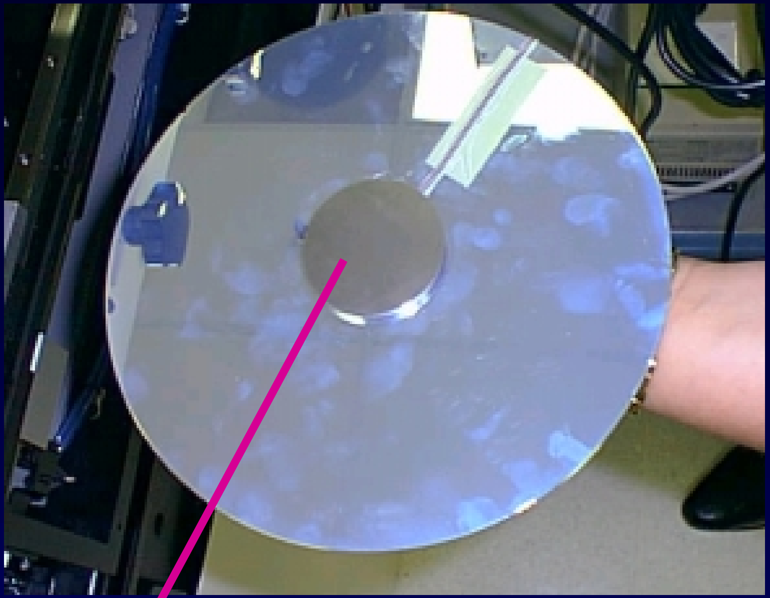
- S9K and J973 testheads do not have access to make PCB deflection measurements (can only be done at ITTO Lab).
- Alternative techniques have been developed to make array force measurements on the sort floor.
  - Pressure paper and load cell techniques

Load Cell Technique



Load Cell (to measure Resultant Force Loads)

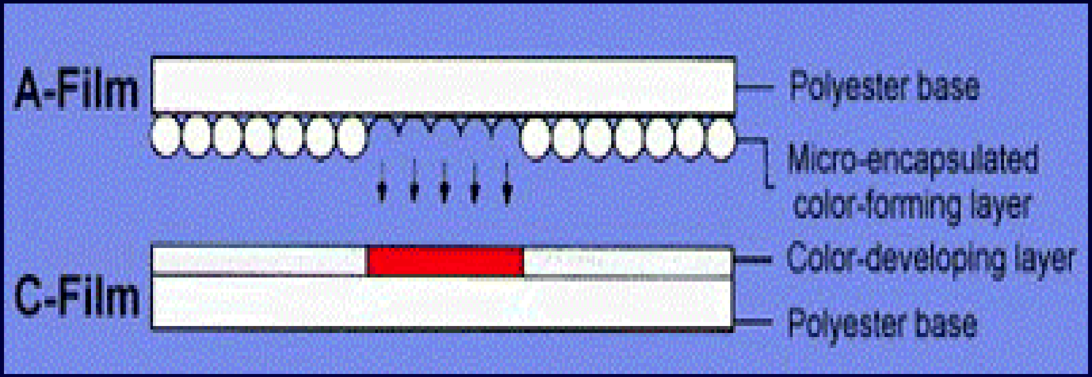
Fixture (Stainless Steel) surrounding the load cell to avoid any off-axis loading

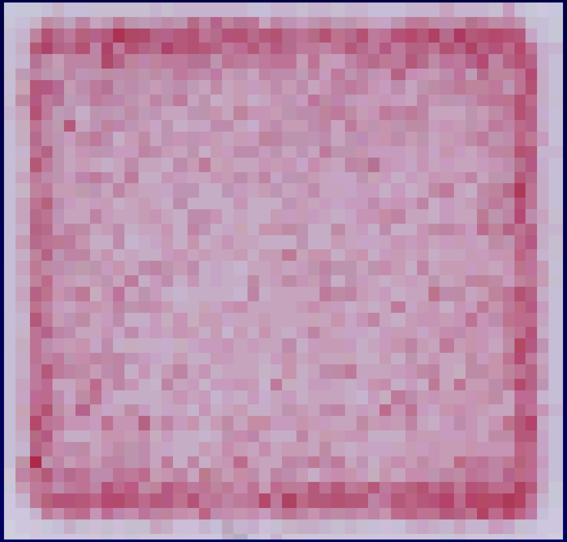


Tungsten Carbide plate on the surface of the load cell and the fixture around the load cell to allow evenly distributed compressive load on the loading surface and establish electrical contact.

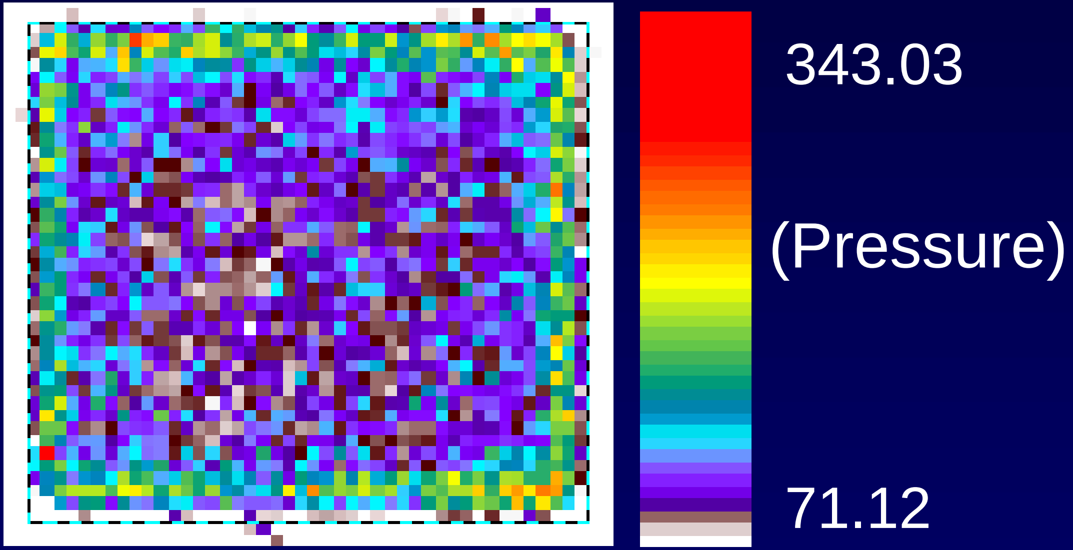
Pressure Paper Technique

Two - Sheet Prescale Film



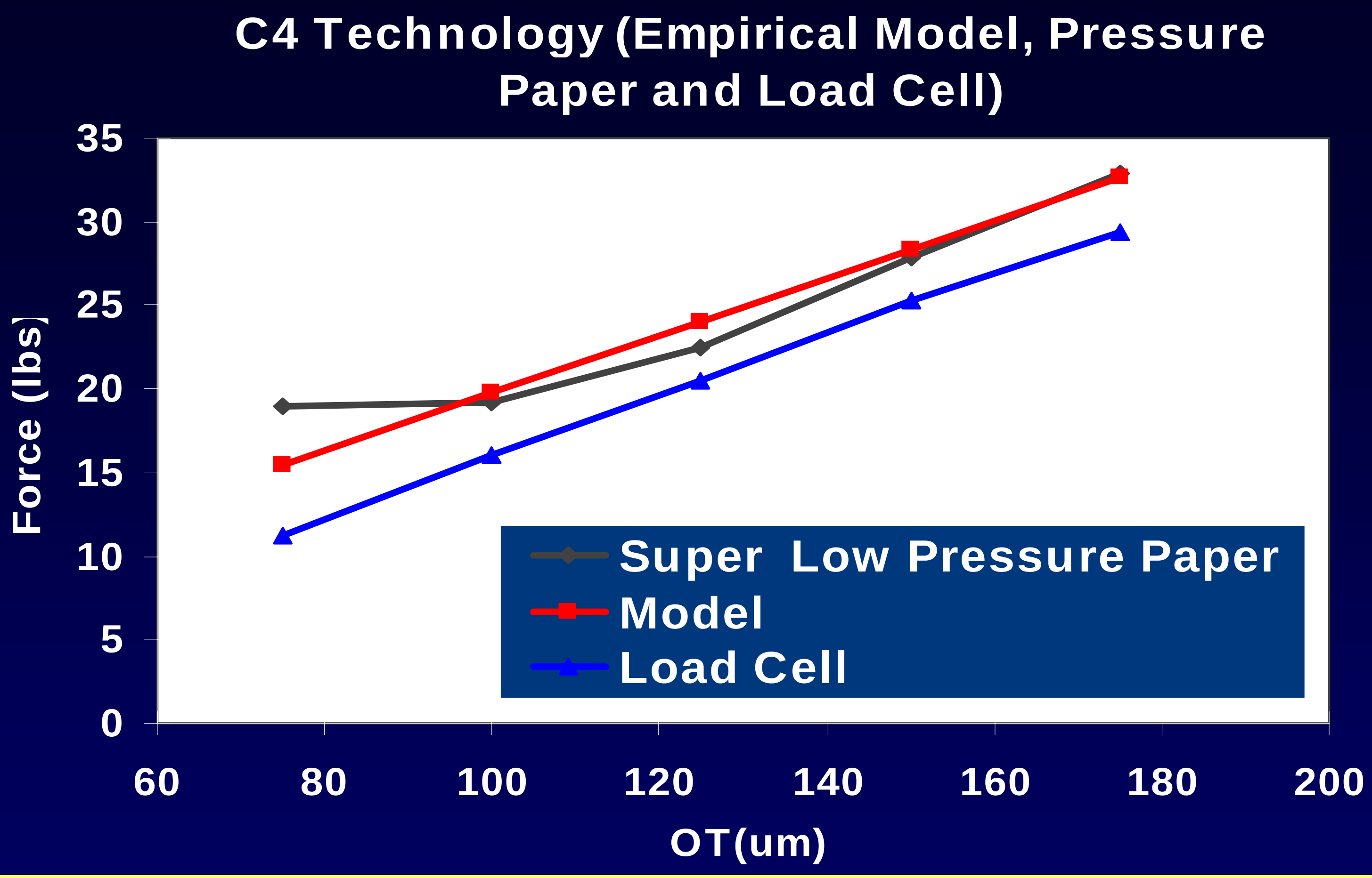


Initial Scan of the Die



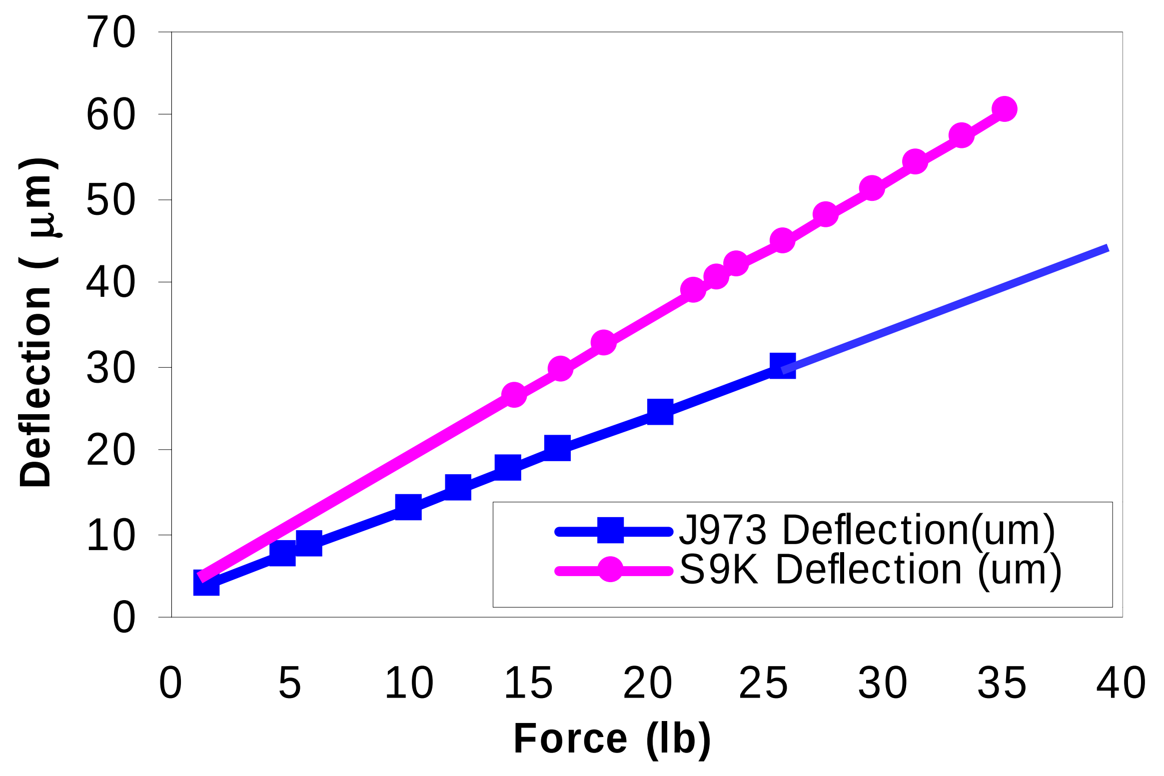
Pseudo-Color Representation by Topaq Analyzer

Combined Results



- Pressure paper technique matches the model closely and is more useful in the production environment.
- Load cell technique shows the right trend but with an offset and is useful in the Lab environment (Fast).

S9K vs J973 PCB Deflection



C4 Technology (Load Cell)

J973 system stiffer than S9k

- **Allowed to match actual probe compression between S9K and J973 to determine normal force per probe.**
- **Obtain comparable Cres**

Conclusions

- A novel model developed to predict the actual compression of the probes in a C4 probe card as function of POT, die location on the wafer, and the probe count.
- Pro/E and Pro/Mechanica analyses matched the PCB deflection to within 5%.
- Pressure paper and Load Cell techniques matched the model and are good techniques to measure array force when there is no access to make PCB deflection measurements.
- Determine maximum probe count and chuck force.
- Aid in optimization of sort OT’s.