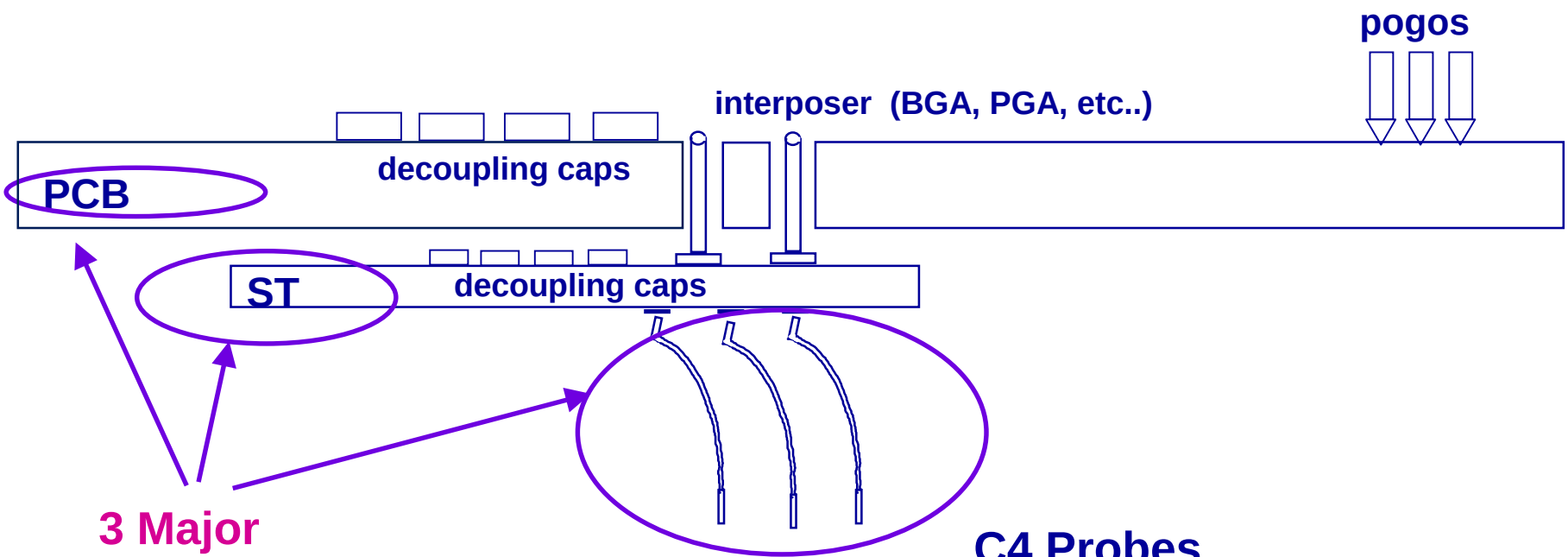
C4 Probe Card Space Transformer Technology Overview

Grace Chan
Justin Leung
Intel Corporation

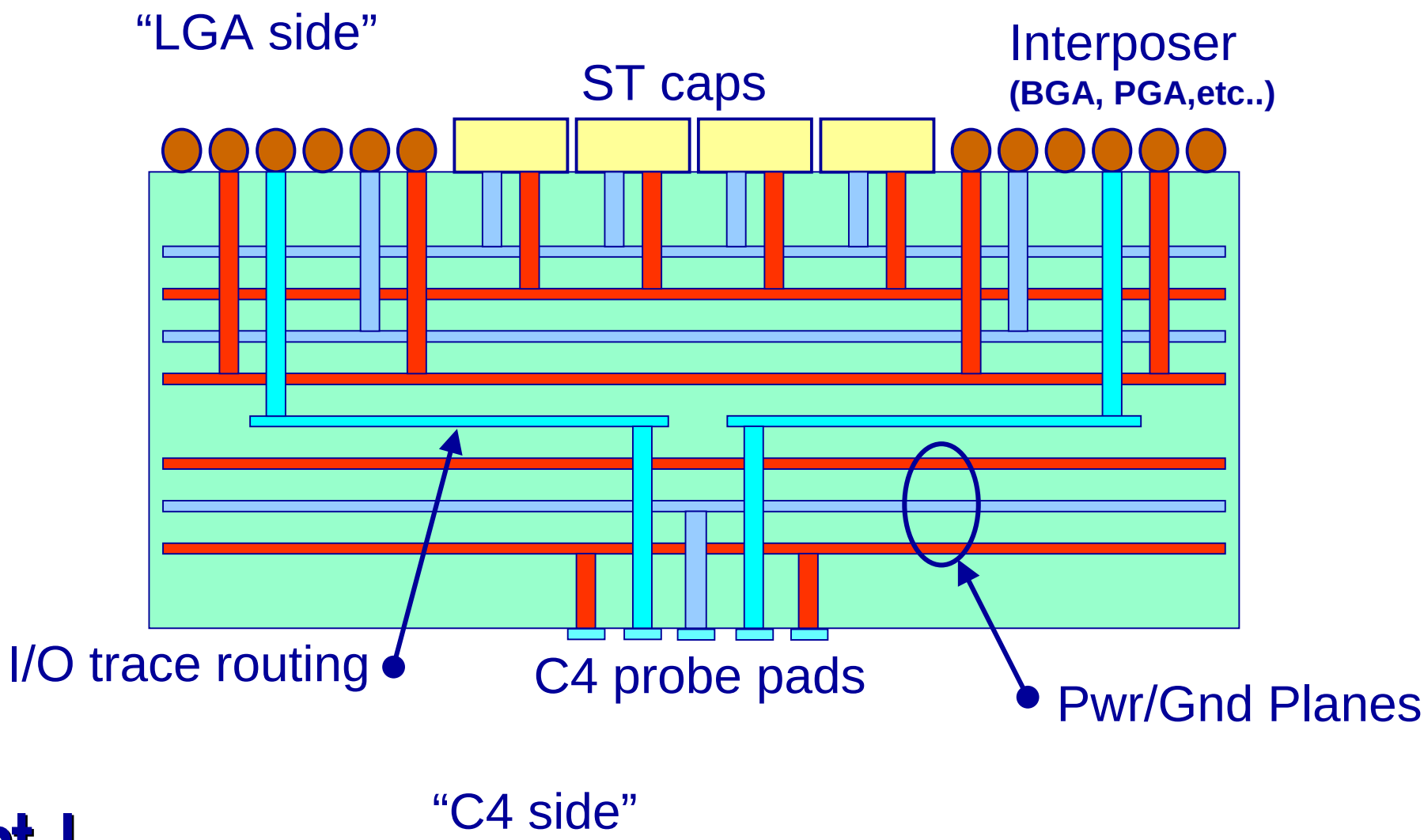
Outline

- C4 Probe Card Space Transformer Overview
- Multi-layer Ceramic Space Transformers
- Future Space Transformer Technologies

C4 Probe Card Cross-section



C4 Space Transformer Structure



Space Transformer Key Functions

- PCB pad to C4 bump pitch reduction
- Power delivery
- I/O routing
- Probe card structural integrity

Microprocessor Performance Trends

YEAR ***TECHNOLOGY NODE***	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100nm*
C4 Area Array bump pitch (μm)	200	200	200	200	200	200	150
Chip size (mm^2)	450	450	450	509	567	595	622
Projected bump count	11250	11250	11250	12725	14175	14875	27644
Clock Frequency (MHz)	1200	1321	1454	1600	1724	1857	2000
Power (W)	90	100	115	130	140	150	160
Core Supply Voltage (V)	1.8	1.8	1.8	1.5	1.5	1.2	1.2
Maximum Current (A)	50	56	64	87	93	125	133

Data abstracted from International Technology Roadmap for Semiconductors, 1999 Edition

Space Transformer Critical Physical Parameters

Minimum Via Diameter and Pitch

Minimum Line and Space Dimensions

Dielectric Thickness (100 - 250 μm)

Relative Dielectric Permittivity (ε_r = 3.0 - 9.5)

Metal Sheet Resistance (3 - 10 mΩ/sq)

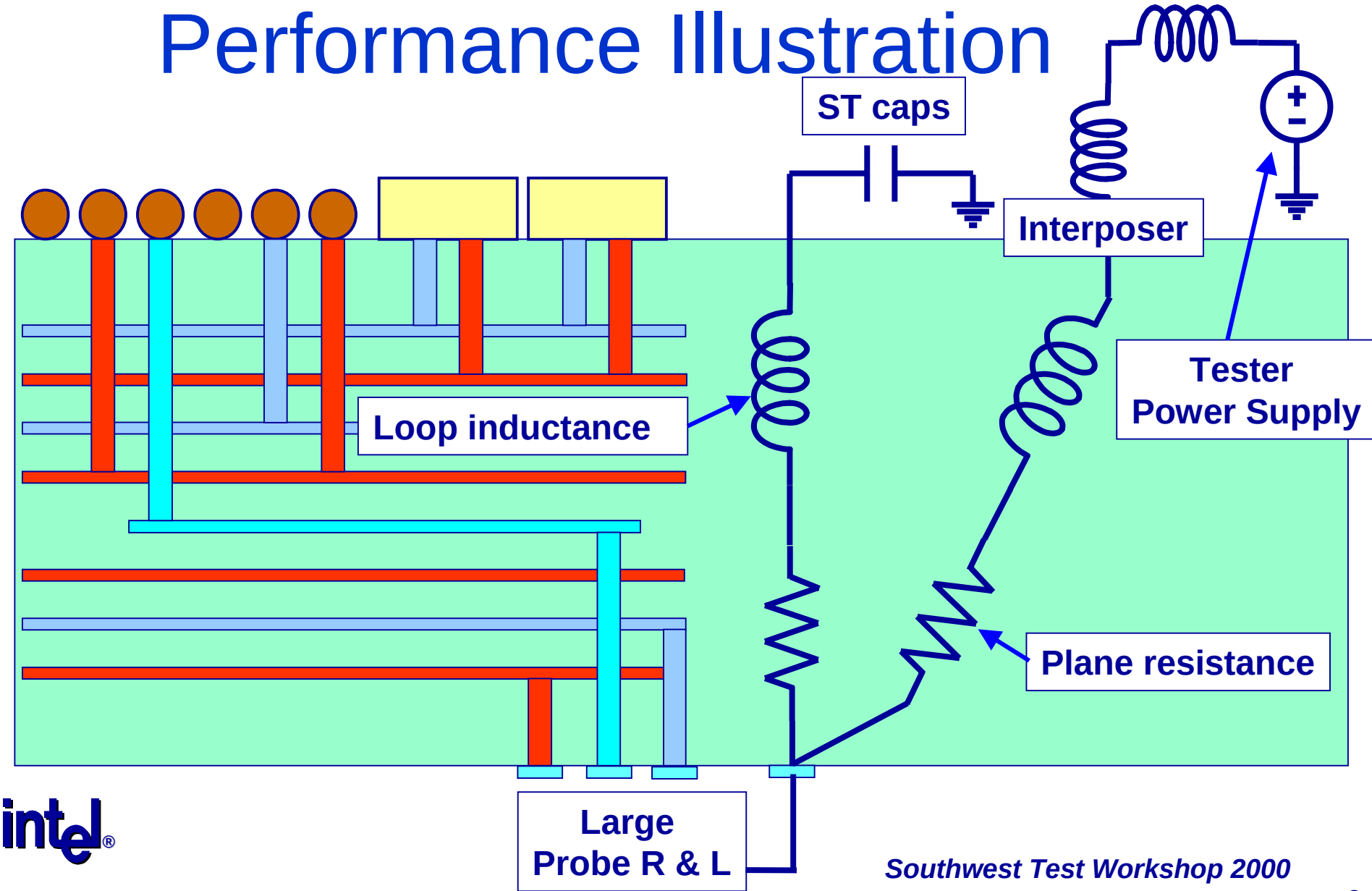
Power/Ground Perforation (0 - 50%)

Coefficient of Thermal Expansion (3 to 70 ppm/^{o}C)

Flexural Strength (80 - 400 MPa)

Thermal Conductivity (0.2 - 200 W/m-K)

Space Transformer Electrical Performance Illustration



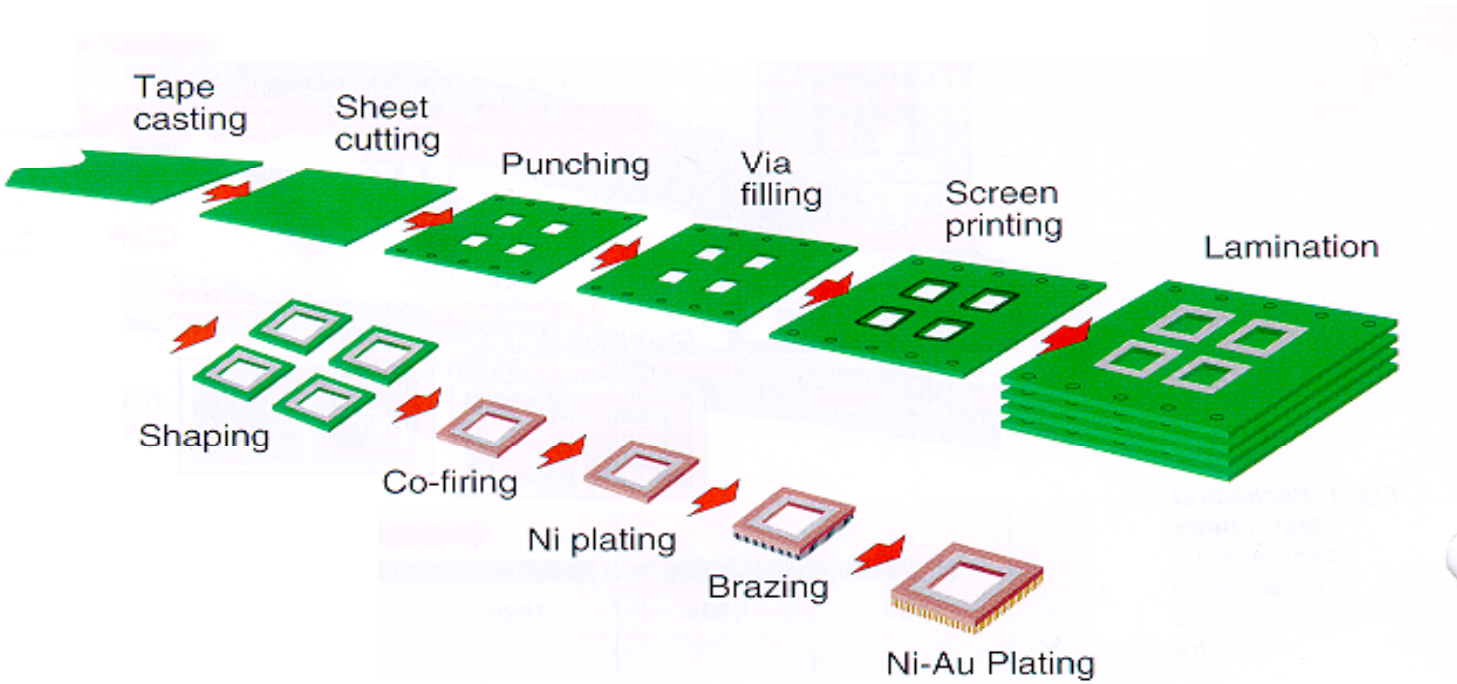
Package and Space Transformer Comparison

	Package	Space Transformer
I/O	Route all traces	Only route subset of I/O's
PWR/GND	All bumps	Probe subset of bumps
Number of layers	Cost restriction	Minimize via inductance
On-Pkg Capacitors	Cost restriction	Maximize # Caps
Force	Insertion	Probe forces
Operating Temperature	Designed for external temperature compatibility	Designed for sort
Reliability	Thermal shock tests	Mechanical touchdowns
Connections	C4 bumps	C4 probes (high R & L)

Space Transformer - Multi-layer Ceramic

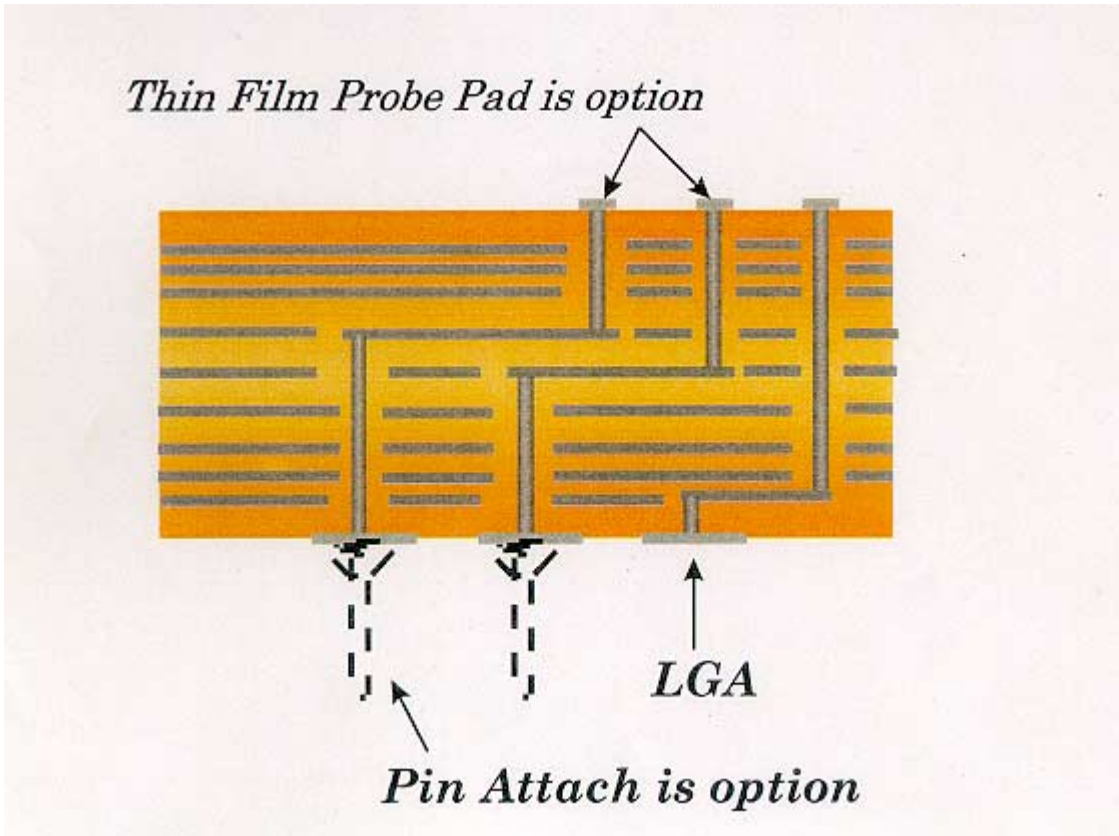
- High Temperature Co-fired Ceramic (co-firing temperature ~1600^{o}C)
- Alumina - 90%+ Al_2O_3 and 10%- Glass; AlN, BeO, Mullite ($3Al_2O_3 \bullet 2SiO_2$)
- W/Mo Metallization (High melting temperature) Resistivity = 5.0 $\mu\Omega$-cm
- Typical dielectric thickness range: 150 - 200 μm
- Relative Dielectric permittivity ε_r = 9.6
- CTE = 6.7 ppm $^{o}C^{-1}$
- Layer stack can exceed 30 layers

MLC Manufacturing Process Flow



Courtesy of Kyocera

Multi-layer Ceramic Cross-Section



Courtesy of NTK

MLC Technology limitations

- High metal resistivity
- High dielectric permittivity
- Via manufacturing process
- Line patterning process
- Dimensional tolerance
- Throughput time

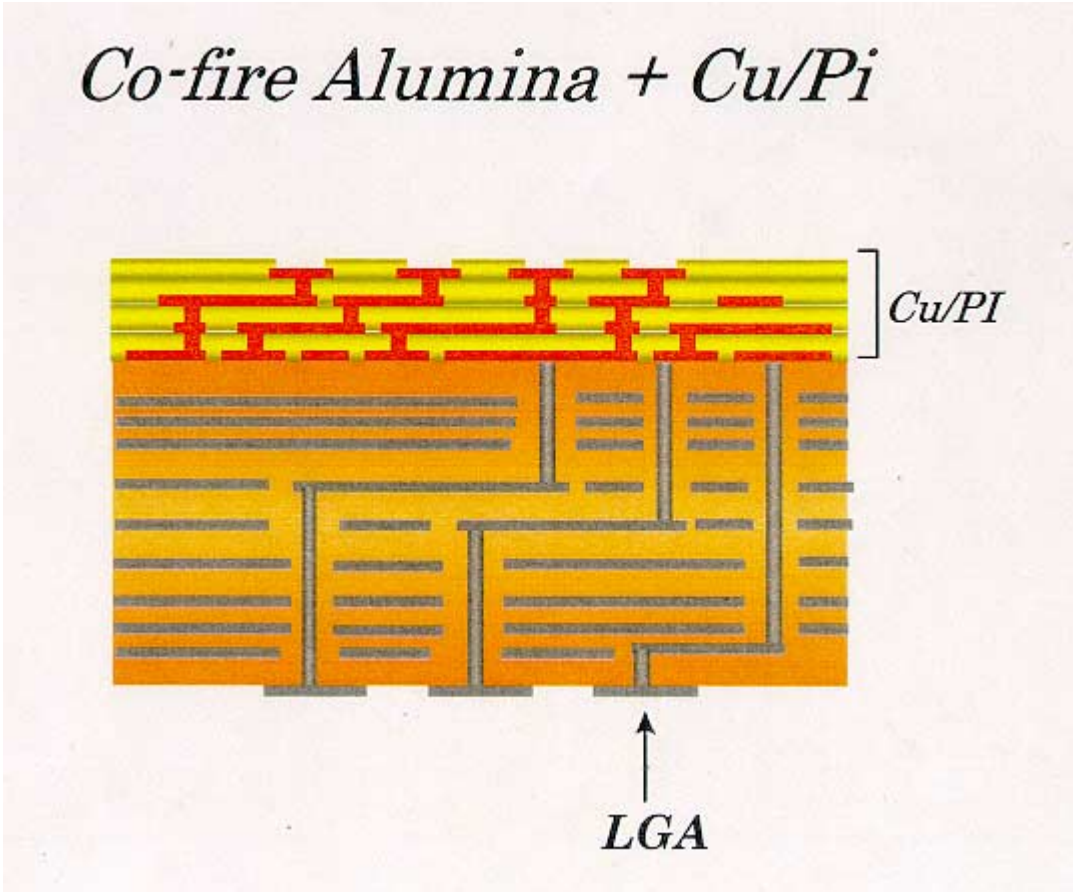
Future Space Transformer Technologies

- MLC with Multiple-layer Thin Film (MLC-MTF)
- AlN Substrate with Multiple-layer Thin Film
- Organic Build-up
- Glass Ceramic

MLC with Multi-layer Thin Film

- Thin-film build-up occurs after co-firing process
- Polyimide (PI) thin film build-up on Al_2O_3 Ceramic by spin coating
- Cu metallization on PI thin film by photopatterning
- Fine line width and via dimensions

MLC-MTF Illustration

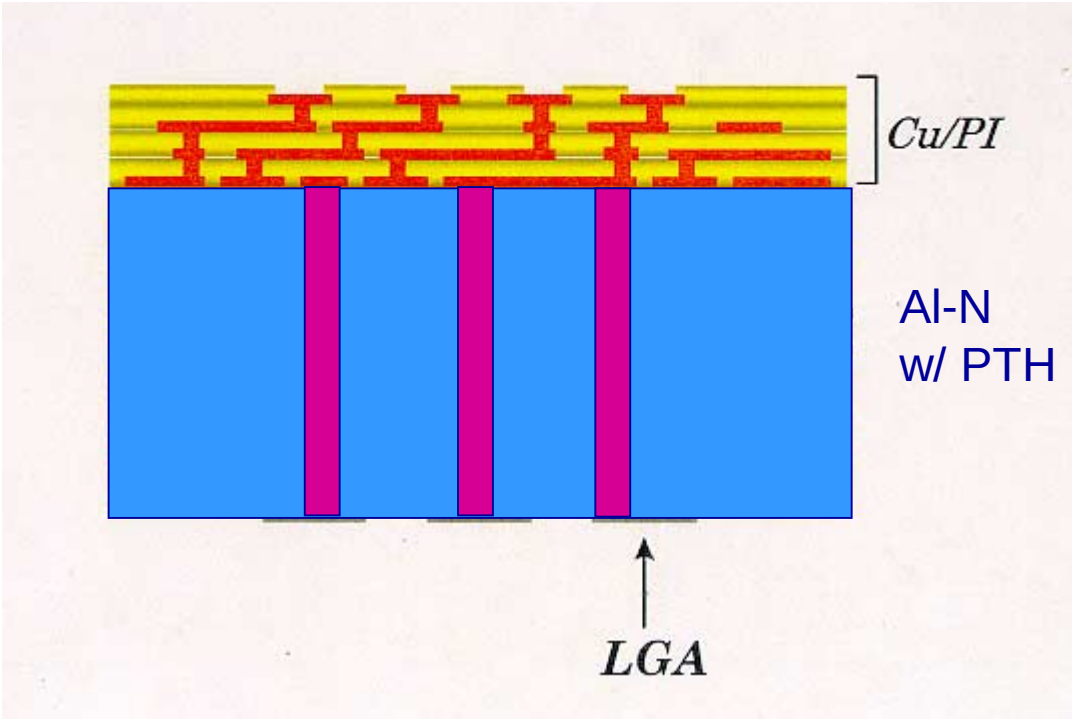


Courtesy of NTK

AlN Substrate with MTF

- Polyimide (PI) thin film build-up on AlN substrate
- Cu metallization on PI thin film by photopatterning
- No internal layers exist in AlN; PTH (Plated Through Hole) vias
- Fine line width and via dimensions
- Excellent heat dissipation

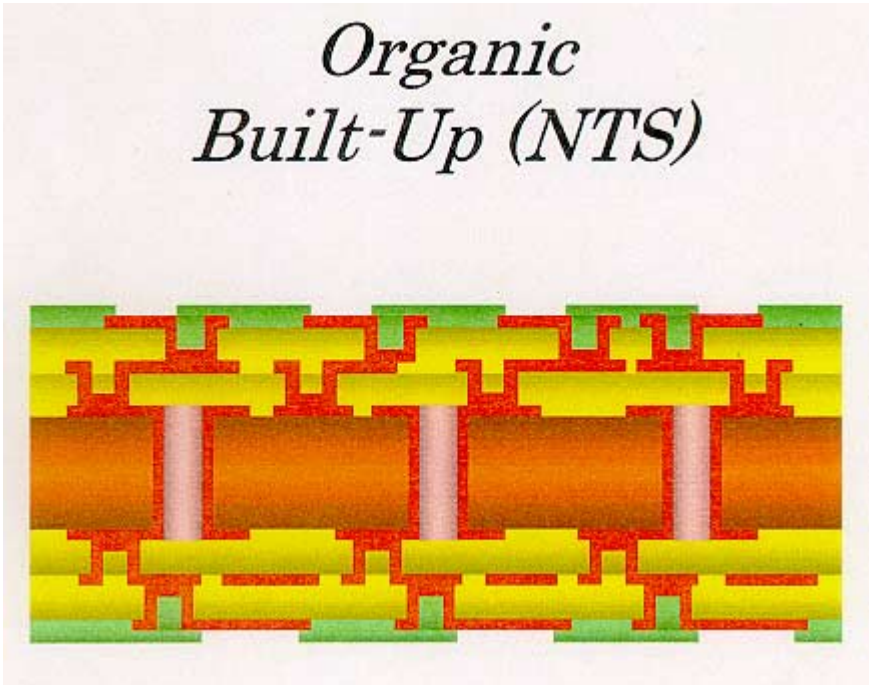
AlN with MTF Illustration



Organic Build-up Solution

- Organic build-up on both sides of a core
- Cu metallization; line pattern defined by photopatterning
- Via formation by laser drilling or photolithography at build-up; PTH through core
- Fine line width and via dimensions

Organic Build-up Illustration

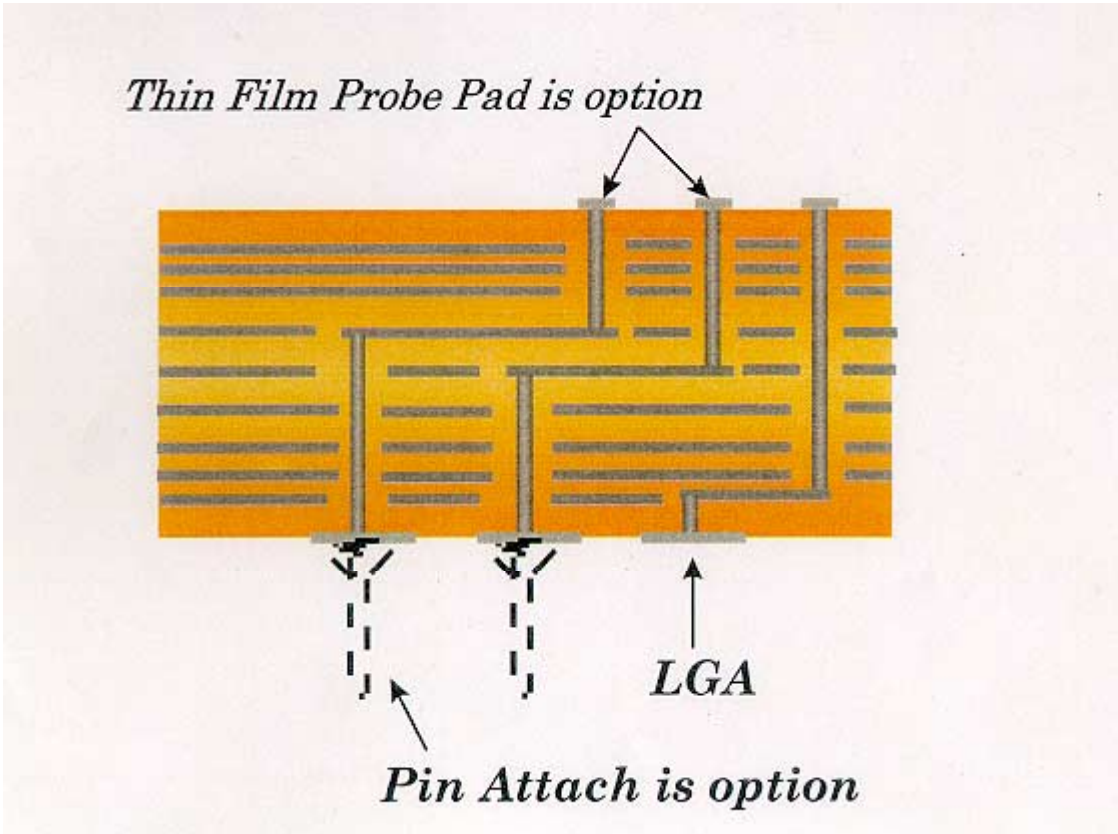


Courtesy of NTK

Glass Ceramic

- Low Temperature Co-fired Ceramic with Cu metallization
- Manufacturing flow very similar to MLC (HTCC)
- Lower co-firing temperature (<1000^{o}C) allows Cu to be used as conductor

Glass Ceramic Illustration



Courtesy of NTK

Technology Comparison

	MLC-MTF	AlN-MTF	Organic Build-up	Glass Ceramic
Conductor	W/Mo; Cu for TF	W in PTH; Cu for TF	Cu	Cu
Dielectric Constant	9.2-9.6	8.8	3.6	5.3
Power Delivery	Fair	Poor	Fair	Good
Routing Capability	Good	Good	Good	Fair
Structural Integrity	Fair	Fair	Poor	Good
Thermal Conductivity	Good	Excellent	Poor	Fair
CTE mismatch with PCB	Fair	Fair	Poor	Good
Throughput Time	Poor	Fair	Good	Fair

Summary

- A space transformer is a major component of a probe card. It provides pitch reduction, high routing density and localized mid-frequency decoupling.
- A space transformer and a microprocessor package have very different design driving factors. An optimal package design may not be a good space transformer.
- With accelerating microprocessor performance, future space transformer technologies are necessary. MLC-MTF, AlN-MTF, Organic build-up, and glass ceramic are all contenders to be the next generation technology.