Lucent Technologies
Bell Labs Innovations

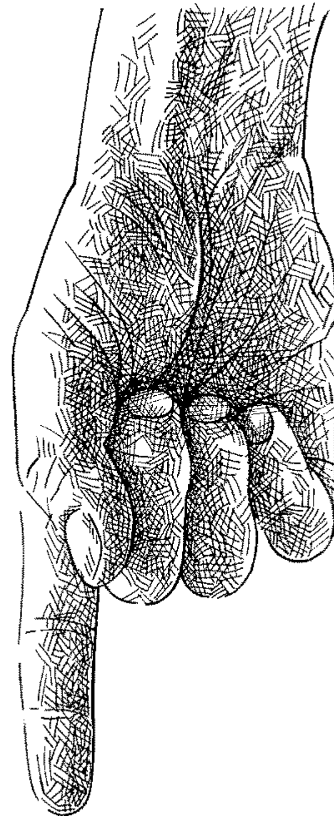
Alternatives to Vertical Probing

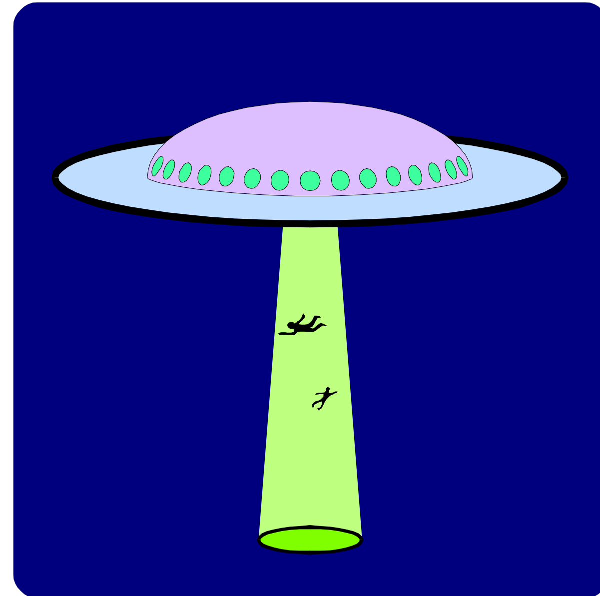
Philip W. Seitzer
Distinguished Member of Technical Staff
Equipment Engineering & Development
Lucent Technologies, Allentown, PA

Outline

- Vertical Probing Background - what is it?
- Implementation Issues when Probing ASICs
- Some Alternatives to Vertical Probe
- Cost/Benefit Analysis Methodology
- Recommendations

I. What Is Vertical Probe?





Vertical Probes

DEFINITION

Vertical Probing:

- Probing to enable a complete electrical test on a device in wafer form...

— on solder bumps...

— in an X-Y array.

Cerprobe "Cobra" Probe

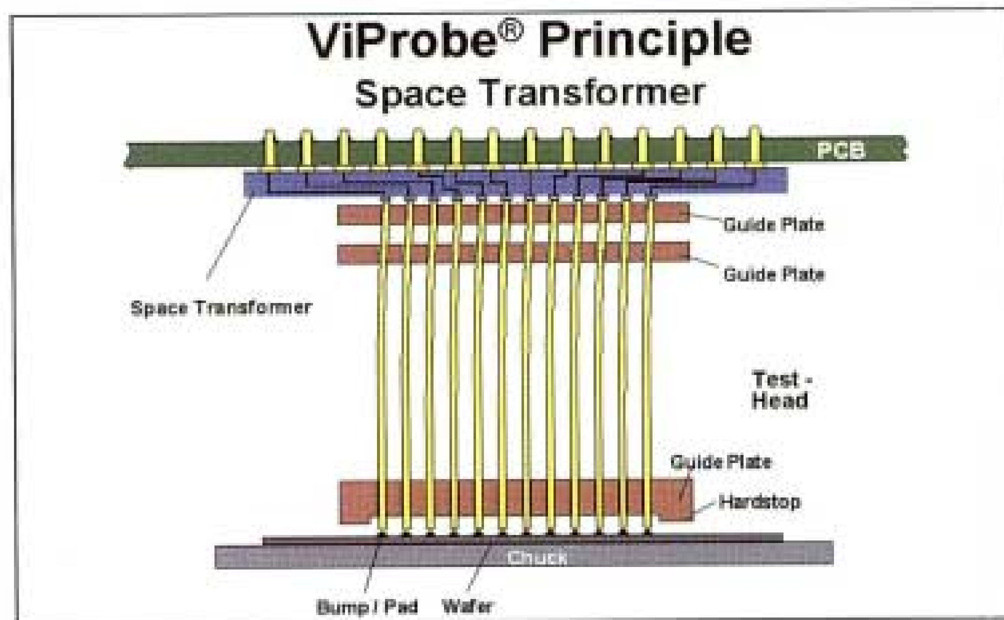


Figure 1. Cross-section view of the ViProbe® replaceable probe head illustrates the plate technology that positions the probe wire for controlled buckling and maximum flexibility. Controlled buckling is the key to consistent contact force and proper scrub action of the probe tips.

Courtesy of Cerprobe

Allentown Wafer Probe

Lucent Technologies
Bell Labs Innovations

Why Do We Do It??

- Example:
  - Package and assembly costs $100.00
  - Cost to vertical probe one die is $1.00
  - Each bad die found at probe saves $99.00
  - It is cheaper to probe if more than 1% of the un-probed die would be defective.

Allentown Wafer Probe

Lucent Technologies
Bell Labs Innovations

II. So What is the Problem?

- Testing ASICs (Application Specific Integrated Circuits) presents challenges to implementing vertical probe.

Characteristics of ASIC products

- Driven by customer needs
- Small volumes
- Low profit margins
- Many have short product life-cycles but a few have long ones
- Huge number of non-standard bond pad/ bump arrangements and package types

Allentown
Wafer Probe

Lucent Technologies
Bell Labs Innovations

Characteristics of ASIC production

- Short <u>concept-to-final-product</u> interval
  - Pressure on designer to cut design cycle
    - Use design elements that may not be characterized
  - Pressure on test engineer to “prepare test quickly”
    - Use test routines that worked for him before
    - Skip tests that require time to debug
  - Pressure on production to get it out the door

Major Issues with Vertical Probe in the ASIC Test Environment

- Design issues
- Implementation issues
- Production Issues

Allentown Wafer Probe

Lucent Technologies
Bell Labs Innovations

Vertical Probe Design Issues

- Cost vs. performance tradeoff
- Delivery interval for vertical probe cards
- Difficulty in correcting design or fabrication errors

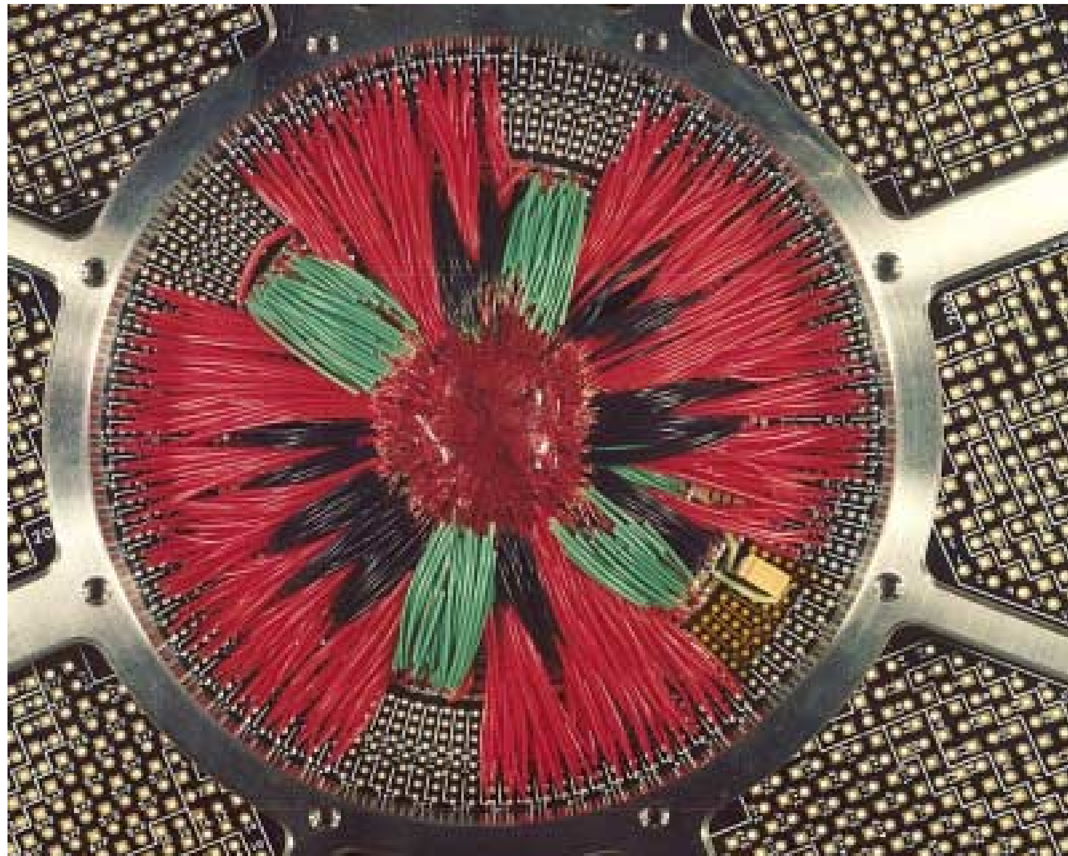
Allentown Wafer Probe

Lucent Technologies
Bell Labs Innovations

Cost vs. Performance Tradeoff

- Space Transformer - two options
  - Multi-layer ceramic > 1 GHz bandwidth
    - $120K , 12-14 weeks for 1280 I/O
    - Can not correct design errors
  - Wired <= 600-800 MHz bandwidth
    - $25-35K, 8-10 weeks for 1280 I/O
    - Wiring is fragile

Wired Space Transformer



Allentown
Wafer Probe

Lucent Technologies
Bell Labs Innovations

Delivery Interval Issue

- Typical probe delivery time:
  - 8-10 weeks for wired space transformer
  - 12-15 weeks for ceramic space transformer
- Desired interval from probe design completion to first prototype probe: 2-3 weeks
  - Probe card design is always late
  - First wafers are usually early
  - Standard cantilever probes meet or beat this interval

Allentown Wafer Probe

Lucent Technologies
Bell Labs Innovations

Correcting Errors is Difficult

- There is no way to modify a ceramic space transformer.
- Wired space transformers are very hard to rewire:
  - The wire you want will be on the bottom.
  - You will break some others getting at it.
  - It will be too short to reach the correct pad.

Allentown Wafer Probe

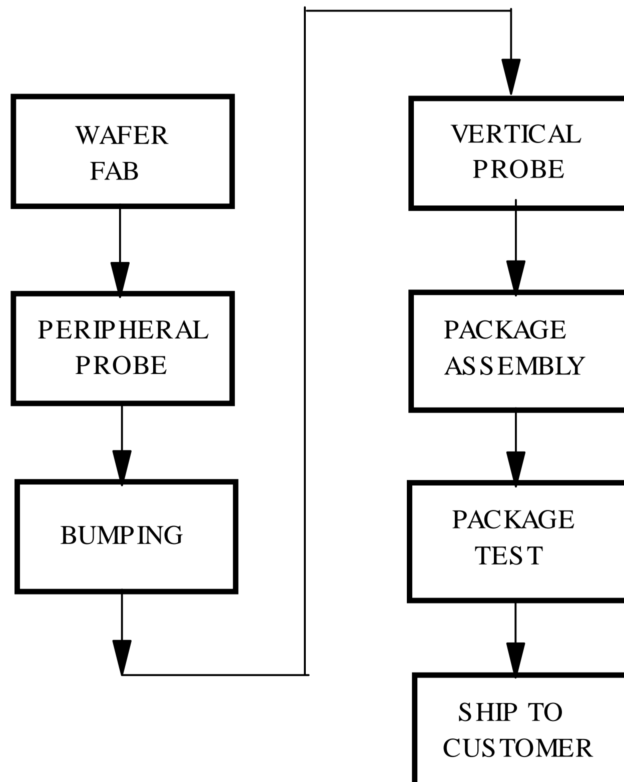
Lucent Technologies
Bell Labs Innovations

Implementation Issues

- Most Automatic Test Generation Programs do not handle contact arrays well.
  - Manual intervention and wiring assignment required (prone to errors).
- Debugging a Vertical Probe test program can be difficult and frustrating.
- Position of vertical probe in the manufacturing process adds to cycle time.
  - May add lots of “frequent flyer miles.”

Allentown Wafer Probe

Flip-Chip Process Flow



Multiple test "opportunities" at different locations may add to cycle time.

Allentown Wafer Probe

Lucent Technologies
Bell Labs Innovations

Production Issues

- Testers tend to require many Input/Output channels (= EXPENSIVE).
- Lengthy setup time.
  - Probability of an open probe is high.
- Handling of some product is a safety issue.
  - Lead replacement is under investigation.

Allentown
Wafer Probe

Lucent Technologies
Bell Labs Innovations

Production Issues (con’t)

- Probe Cleaning and Repair Procedures are new and may be unproved.
- “Vertical Probing is different than normal probing”
  - Training, Documentation, Hand-holding, etc. etc.

Lucent Technologies
Bell Labs Innovations

III. Alternatives to Vertical Probing

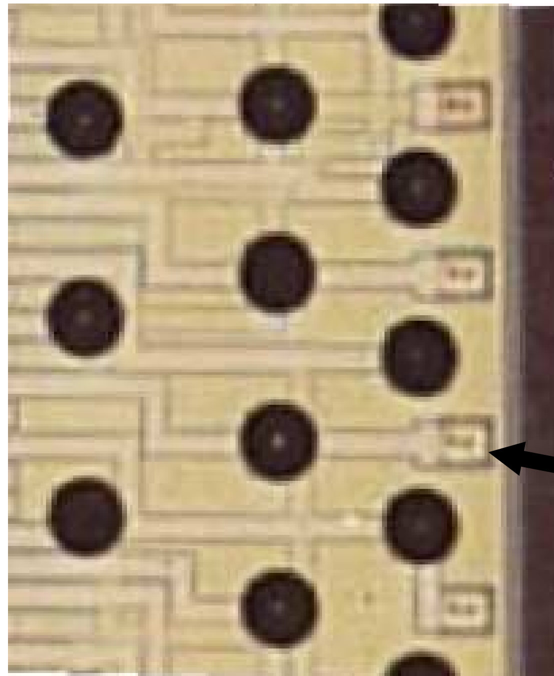
Don’t Probe at All (cut & go)

- May make sense, especially when the package is inexpensive.
- High priority prototype methodology - it’s faster to “eat the defects” at package test.
- May not be possible (Known Good Die with quality requirements).

Allentown
Wafer Probe

Lucent Technologies
Bell Labs Innovations

Implement Peripheral Probe Pads



Probe Pad

Peripheral Probe Pads

- Designed to use traditional cantilever probes.
- Electrically connected to the I/Os needed to test.
- Power & Ground connections provided.
- Enable electrical test before bumps are applied.
  - Earlier feedback to wafer fab.
  - Prevents bumping a dead wafer.
- Add to silicon real-estate requirement.

Allentown Wafer Probe

Lucent Technologies
Bell Labs Innovations

Probe Only Selected Bumps

- Cantilever probe cards, with flat tips, can cover an array, up to 100-150 bumps.
  - Less expensive than vertical probe.
  - Easier to maintain & use.
- Requires that probe causes minimal damage.
- Gets harder to do as bump spacing decreases.

Both probe methods produce an incomplete test:

- Not every single solder bump is tested.
- The trick is to maximize the test effectiveness using the available I/O pins.
- Good design and test techniques reduce the risk to practically zero.

Design & Test Techniques

- Maximize fault coverage using fewer pins
  - Built-in Self Test
  - JTAG
  - Boundary Scan
  - IDDQ test

Built-in Self Test

- The device has enough capability to verify its own integrity (it tests itself).
- The results of self-testing are reported (go or no-go) on a few I/O pins.
- Techniques are in infancy, especially in analog and RF worlds.

JTAG

- Form of Design for Test.
- IEEE defined “serial port” function uses few pins.
  - State of device is set-up serially.
  - Clock cycles exercise entire part.
  - Final state shifted out and compared to expected state.
- JTAG logic will add some complexity / chip area.

Boundary Scan

- Another form of Design for Test.
- Logic is added to create a long shift register incorporating I/O buffers and internal nodes.
- States of I/Os and some internal nodes are shifted out through a few pins.
- Shift register adds complexity / chip area.

IDDQ testing

- Test technique that applies to many digital designs.
- Power supply current of device measured when in a known steady-state condition.
- Compared to historical results to determine existence of internal defects.

Allentown
Wafer Probe

Lucent Technologies
Bell Labs Innovations

Vertical Probe Options

- Design For Test
  - Probe peripheral pads using good test practices to maximize fault coverage and have some dropout at package test
- Perform full test using a vertical probe

THE CHOICE DEPENDS ON ECONOMICS AND TEST EFFECTIVENESS

Allentown Wafer Probe

Lucent Technologies
Bell Labs Innovations

IV. Cost/Benefit Economics

- Must understand the TOTAL cost to probe a die:
  - Capital cost of tester & probe card
  - Transportation & labor expenses
  - Engineering costs to implement vertical probe
- Must quantify the cost of not probing:
  - Dropout at package test (test effectiveness)
  - Cost of packaging
- Customer requirements may dictate the choice.

V. Recommendations

- For lower I/O devices (<100-150) use a cantilever probe.
- Apply good design and test practices to allow probing a subset of the total I/O bumps.
- Decide to vertically probe or not based on economics.