

Probing Process Analysis and Continuous Improvement



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Overview

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- **Analyze the current probing process**
- **Present technique for measuring process variations**
- **Show examples of real customer data**
- **Identify key process parameters (Report Card)**



Process Complexity is Increasing

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- **Multi-Dut testing**
- **Larger card probe arrays**
- **High pin count probe cards**
- **High probing loads**
- **Test at temperature**
- **New probe card technologies**
- **Smaller pads and tighter pitches**
- **Pad damage concerns**



Process Variation Knowledge

Critical to Process Improvement

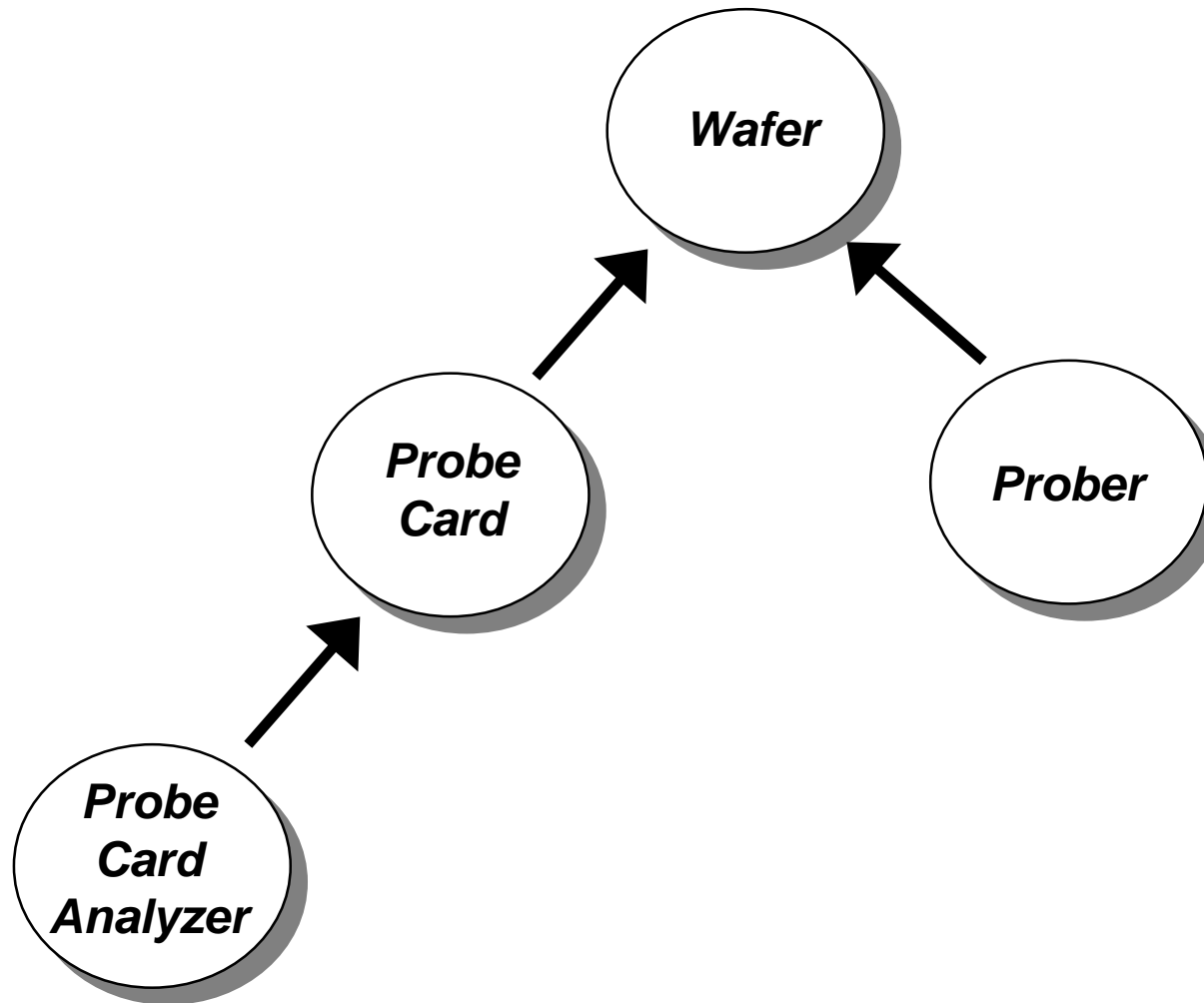
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“Understanding of variation, including appreciation of a stable system, and understanding of special causes and common causes of variation, are essential for management of a system”

Edwards Deming: *The Deming System of Profound Knowledge*

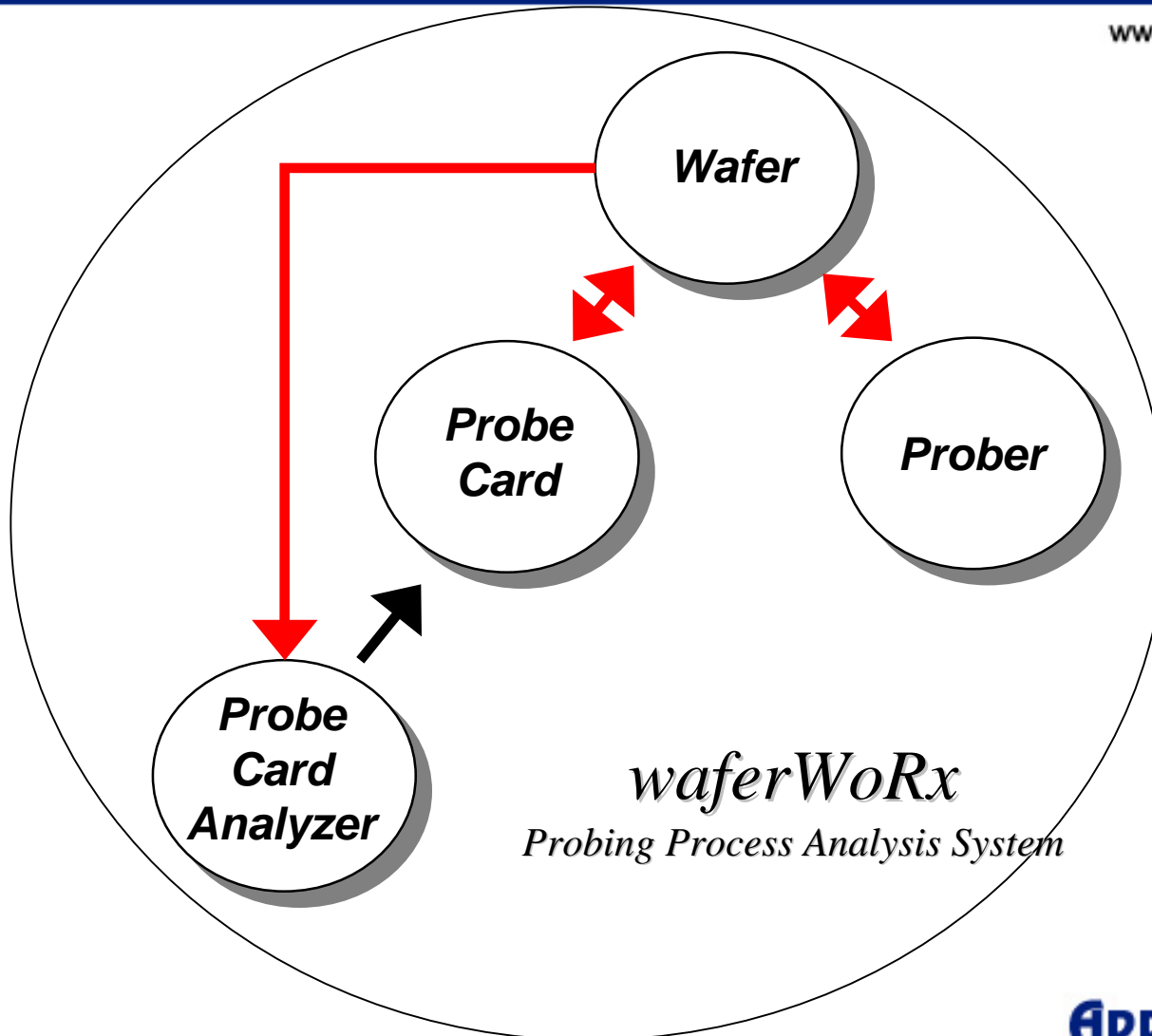
Current Process

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Closed Loop Process

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Analyzing the Variation

Single Wafer Probing Analysis Steps

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Step 1: Measure Scrub properties

- Measure Scrub Relative to Pad Position

Step 2: Die Pattern Analysis

- Die Model Fit: Touchdown Variation

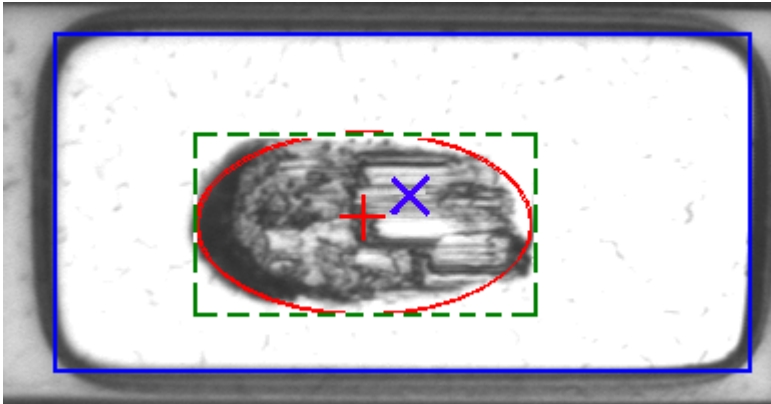
Step 3: Wafer Pattern Analysis

- Wafer Model Fit: Prober / Probe Card Analysis

Measure Scrub Properties

Step 1: Measure Scrub Relative to Pad Position

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× Center of the passivation opening

+ Center of the scrub mark

○ Scrub Mark Area / Size

□ Bounding Box of the scrub mark

□ Passivation opening size

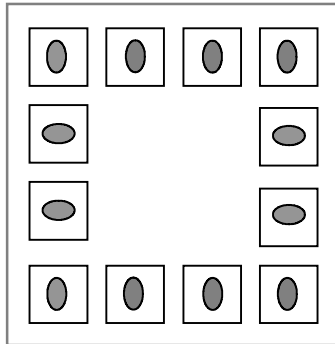
- Position of scrub mark
- Size of scrub mark
- Angle of scrub mark
- Size of passivation opening
- Pad damaged
- Scrub mark distance from the edge of the pad.
- ... Over 40 total parameters

Die / DUT Pattern Analysis

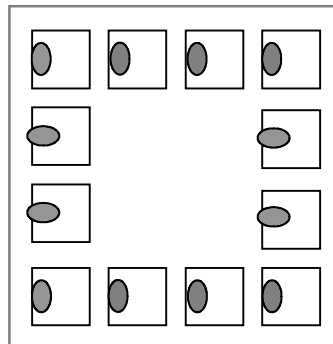
Step 2: Die Model Fit

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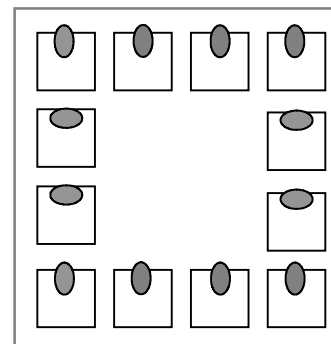
No Error



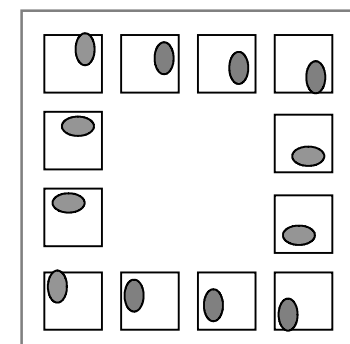
X Error



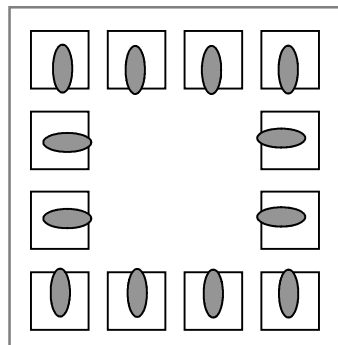
Y Error



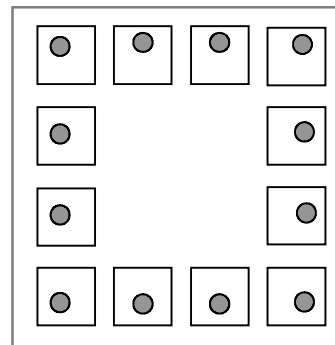
Yaw Error (theta)



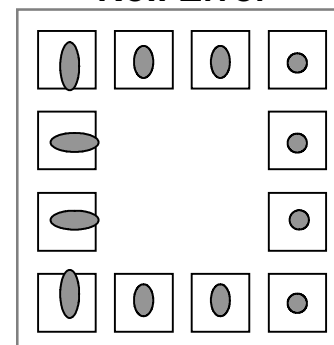
Large Overtravel & Card Array Scaling



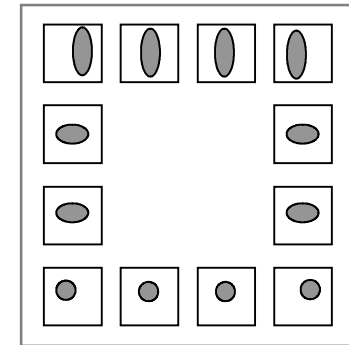
Small Overtravel & Card Array Scaling



Parallelism & Stage Deflection
Roll Error



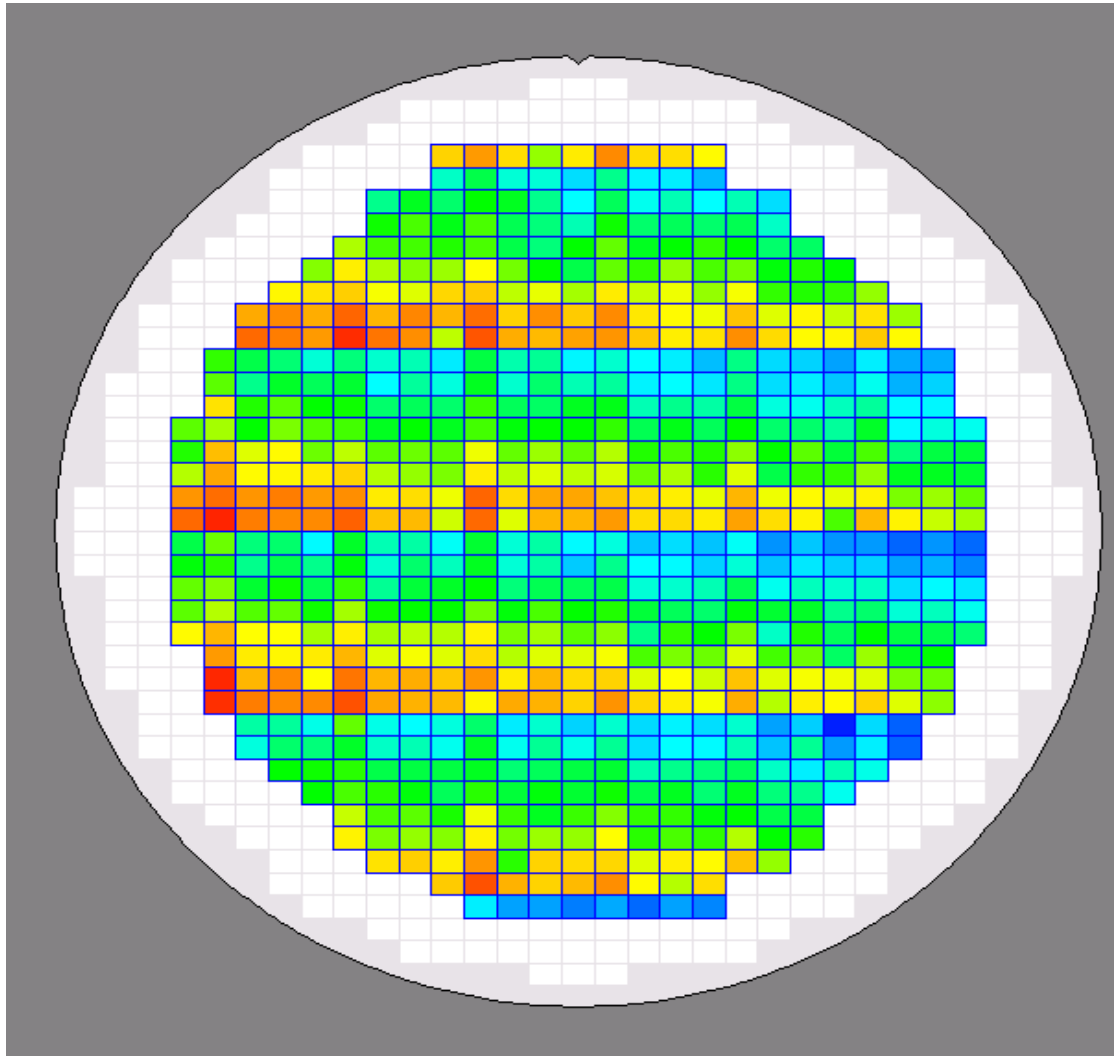
Parallelism & Stage Deflection
Pitch Error



Wafer Pattern Analysis

Step 3: Wafer Model Fit

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Wafer Model Fit

- 1) Setup: X,Y Offset
- 2) Setup : Card Parallelism
- 3) Setup : Card Theta
- 4) Setup: Wafer to Stage Theta
- 5) Stage: Overtravel Variation
- 6) Stage: X,Y Stage Stepping
- 7) Stage Deflection
- 8) Probe Card Accuracy
- 9) Probe Card Repeatability



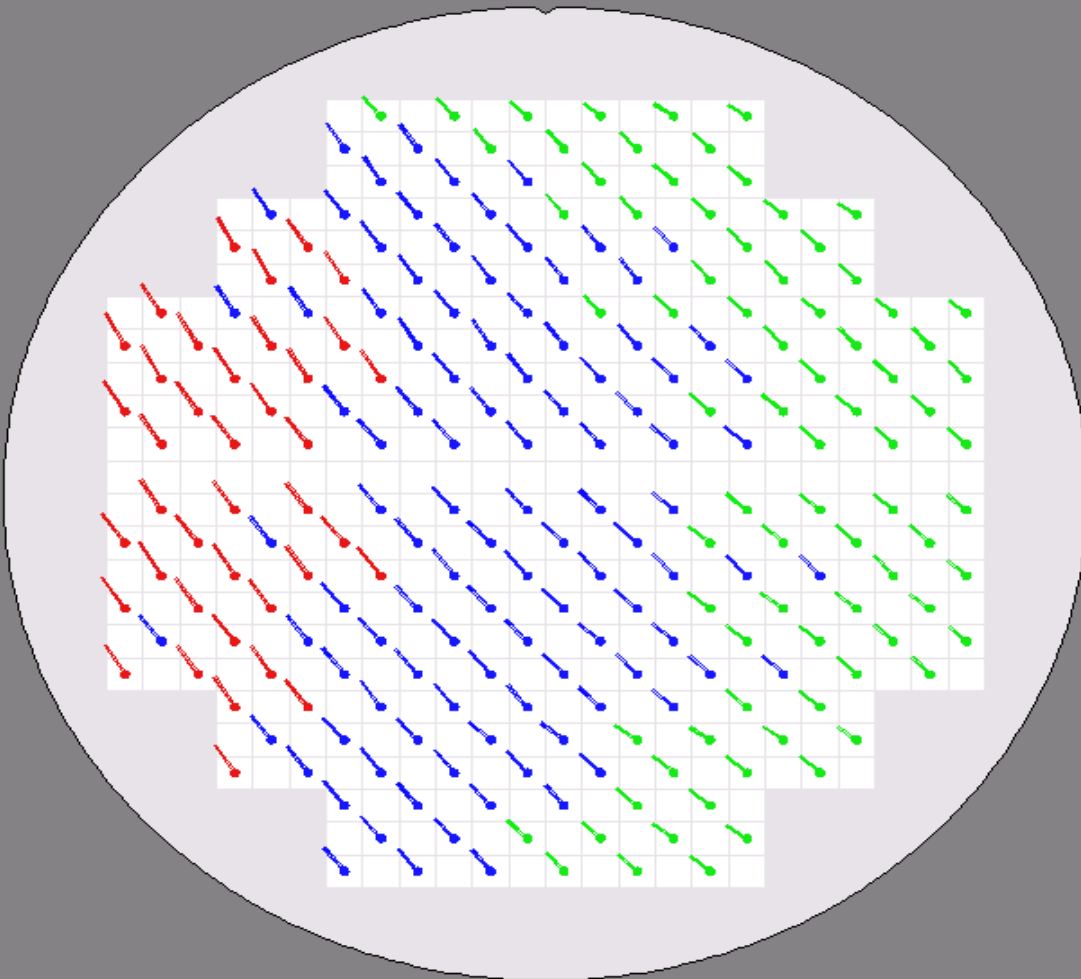
Examples

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1. Setup X,Y Offset
2. Setup Wafer to Stage
3. Stage Stepping Accuracy
4. Deflection & Card Parallelism
5. Multi-Dut Probe Card
Performance at Temperature

Setup - X, Y Offset

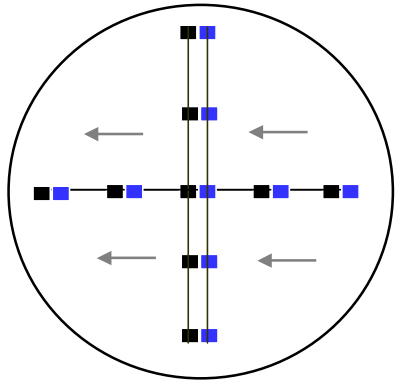
Example # 1



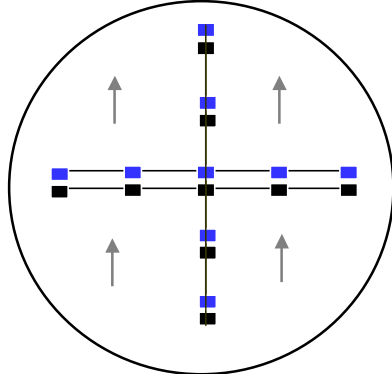
Pass 0
Fail 0
Near 0
Max 21.74
Min 9.24
Ave 14.72
Rng 12.50
Stdev 2.72

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X Error



Y Error



X,Y Setup Error

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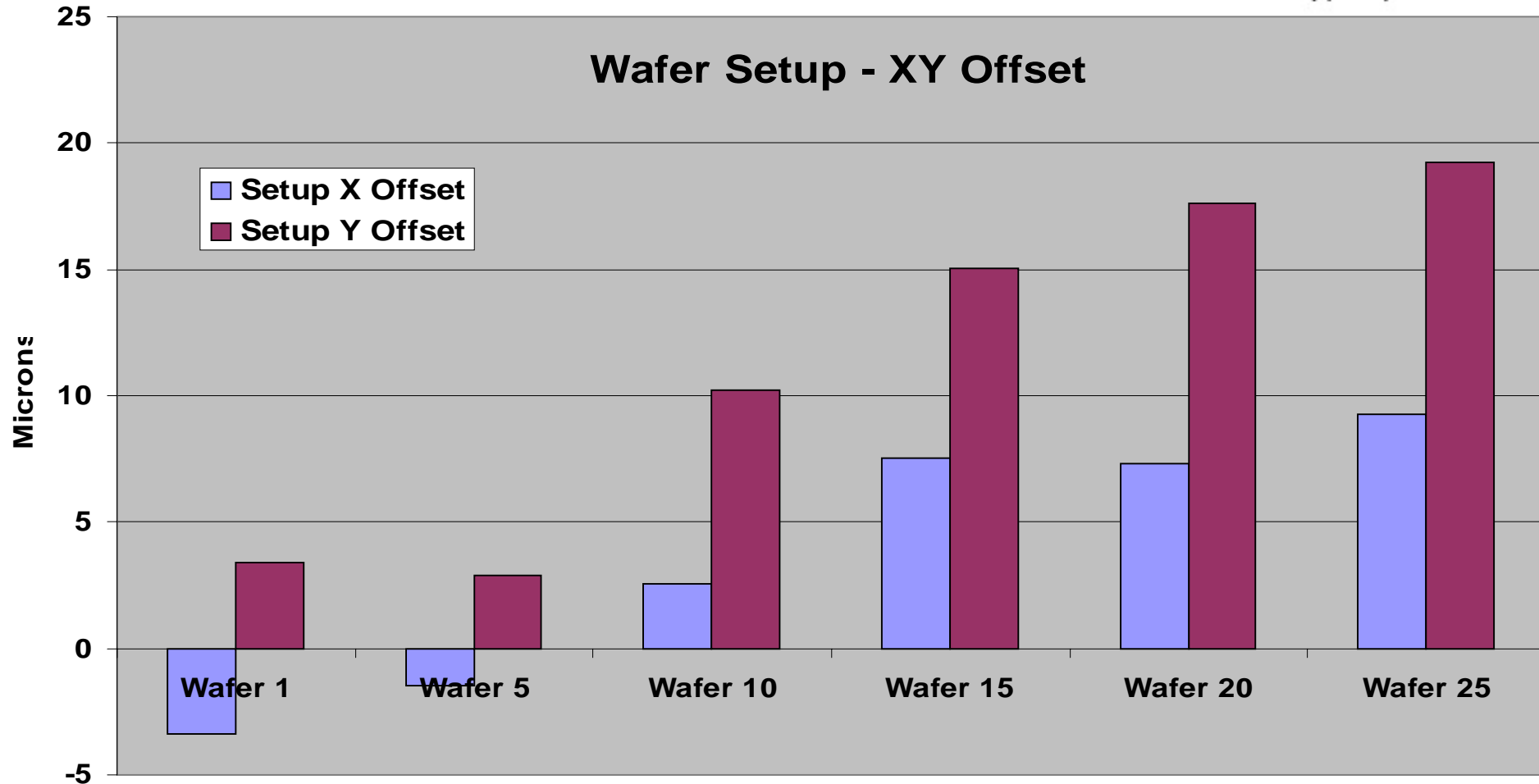
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Setup - X, Y Offset

Example # 1

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Wafer Setup - XY Offset



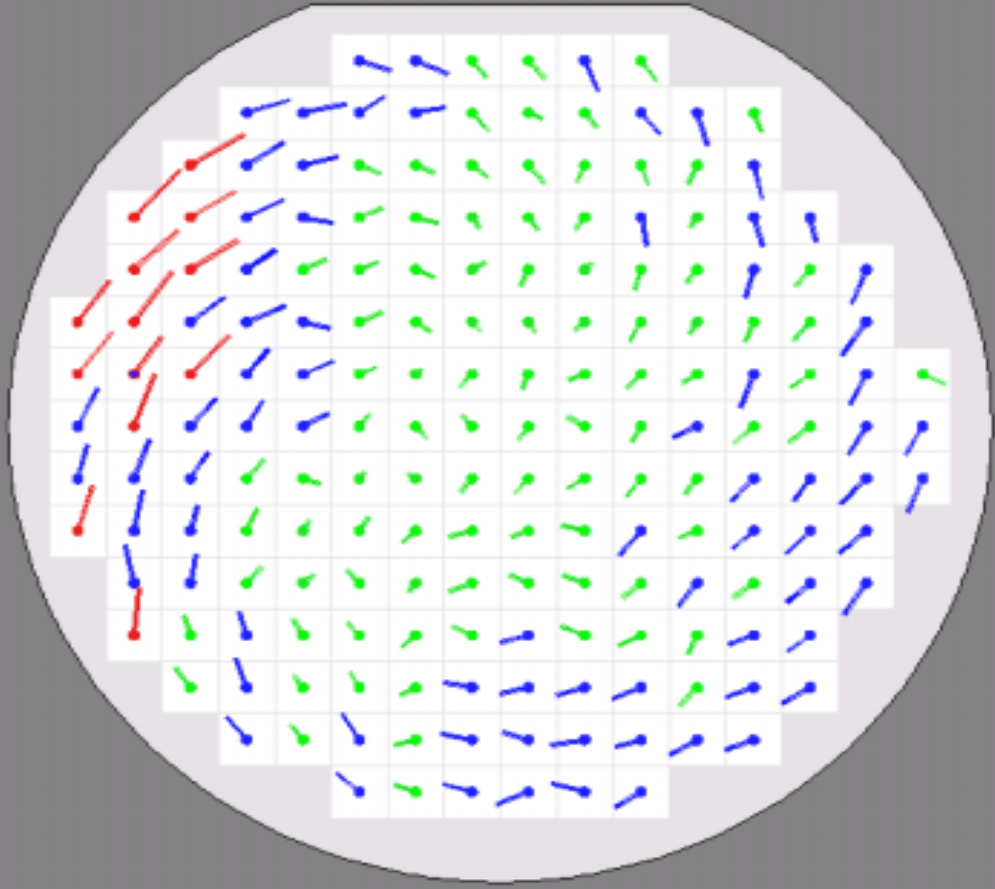
Setup Wafer to Stage

Example # 2

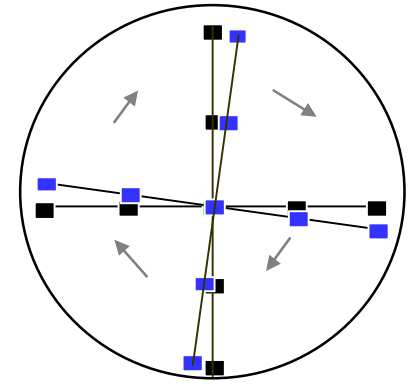


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Wafer Alignment

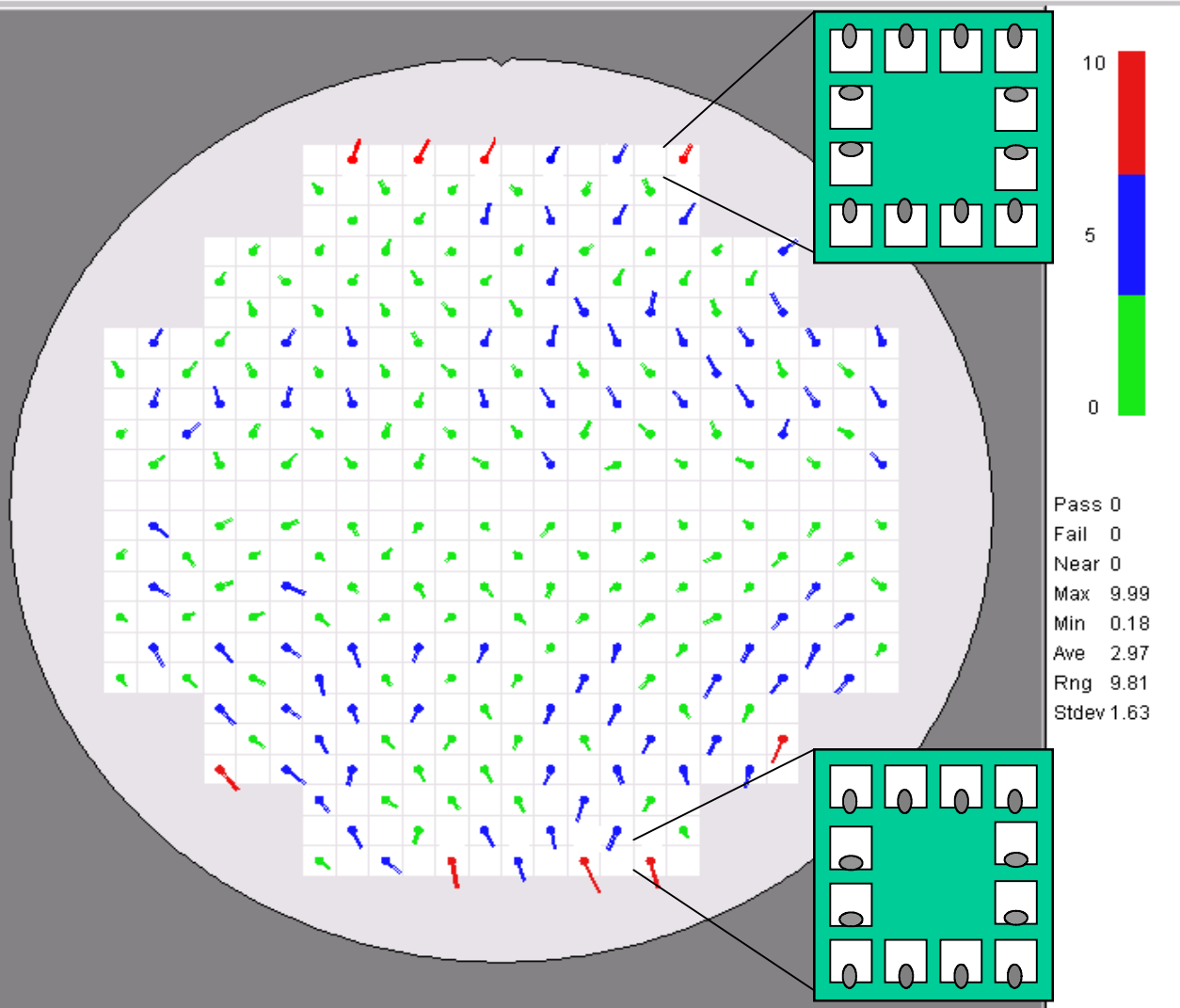


Pass 0
Fail 0
Near 0
Max 4.66
Min 0.10
Ave 1.85
Rng 4.56
Stdev 0.88



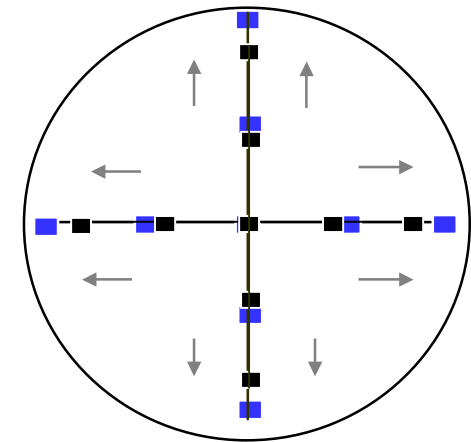
Stage Stepping Accuracy

Example # 3



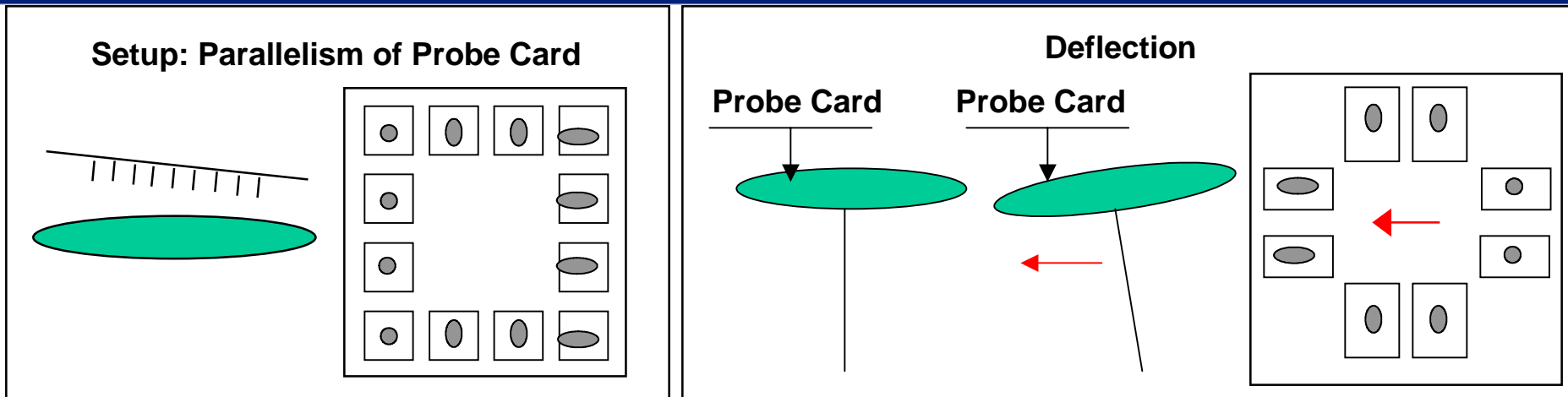
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Scaling & Stepping Errors



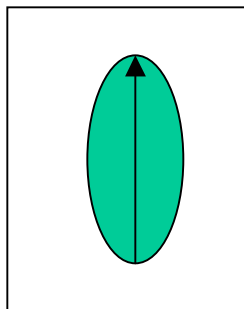
Deflection & Card Parallelism

Example # 4

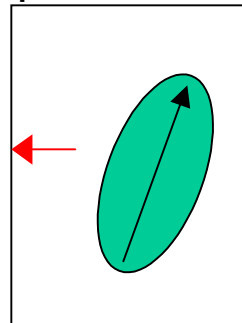


Deflection: Probe Card / Probe Dependent

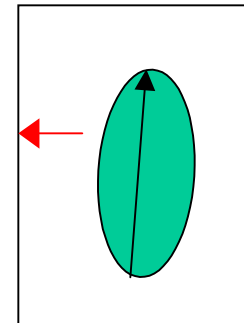
Normal Scrub



Stage Translation
Expected Scrub

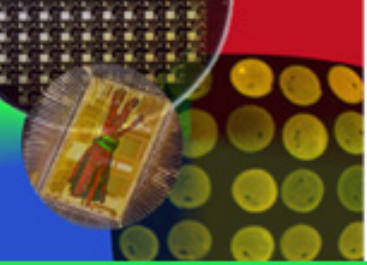


Actual Scrub

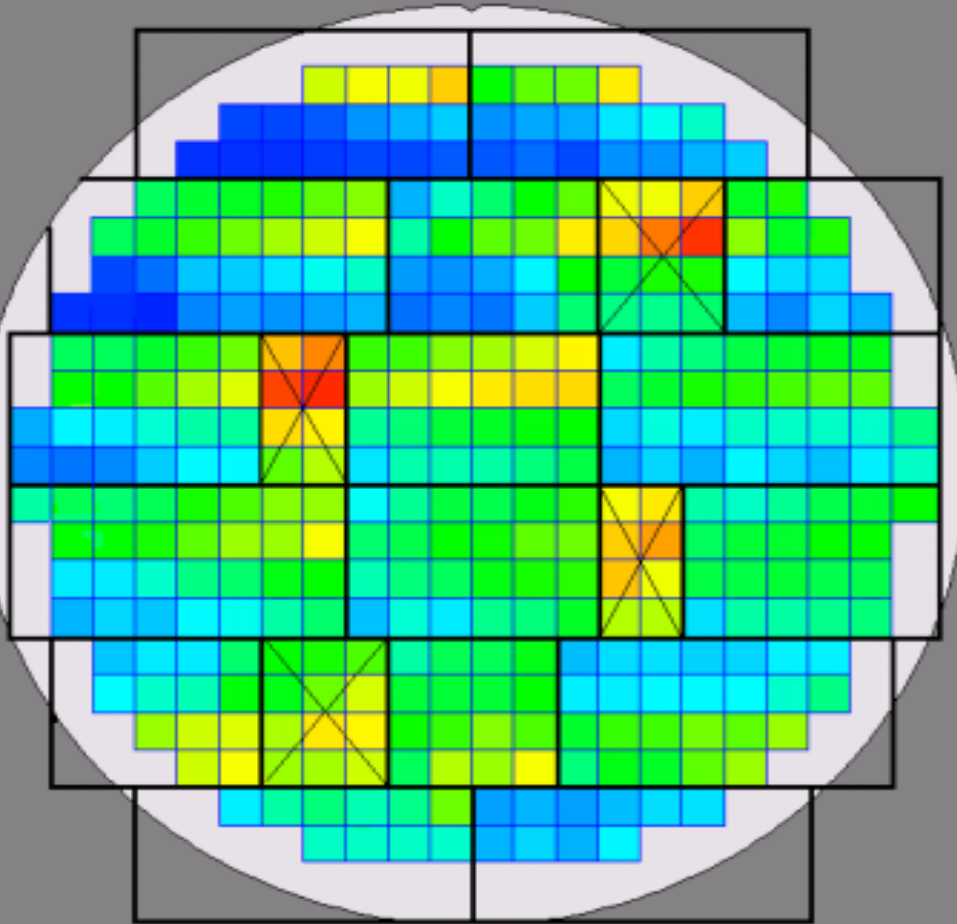


Deflection & Card Parallelism

Example # 4



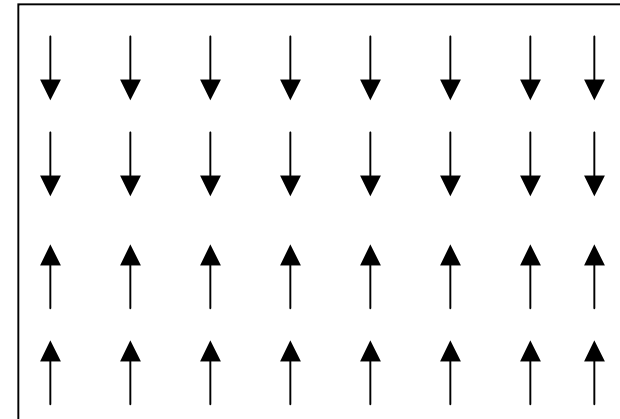
Scrub Major Length



Pass 0
Fail 0
Near 0
Max 58.84
Min 18.38
Ave 36.03
Rng 40.46
Stdev 7.68

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Probe Card

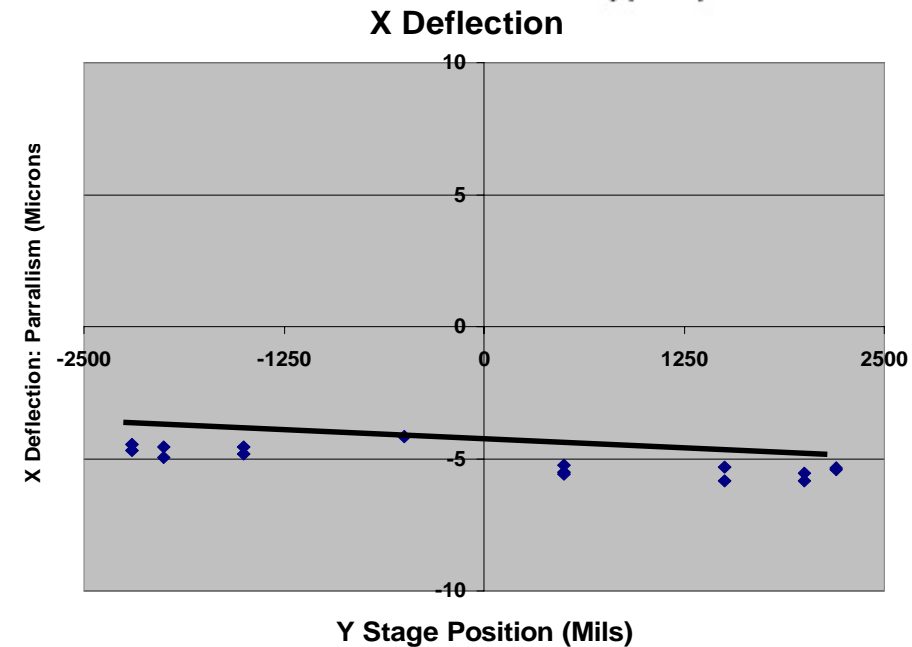
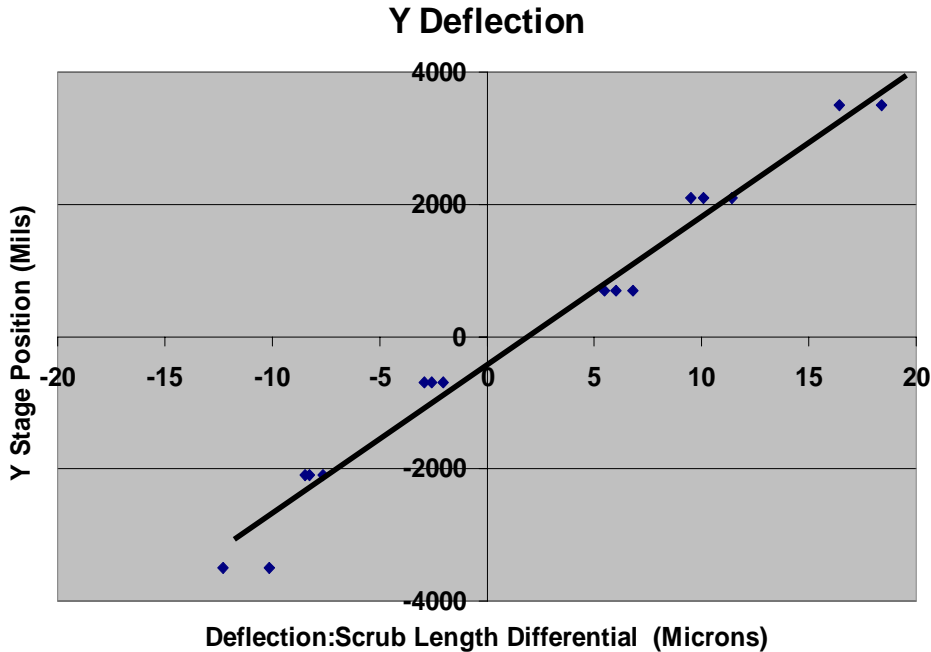


- 32 DUT (4x8)
- Cantilever

Deflection & Card Parallelism

Example # 4

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	Microns
Card Pitch	5.1
Card Roll	3.8
Max Y Deflection	15.2
Max X Deflection	1.3

Multi-Dut at Temperature

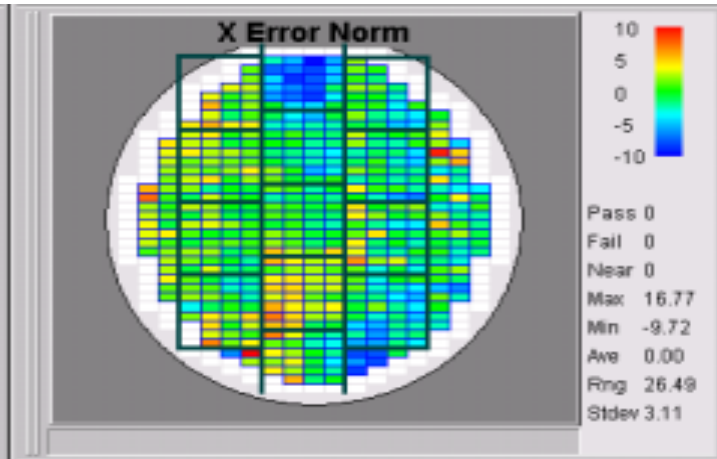
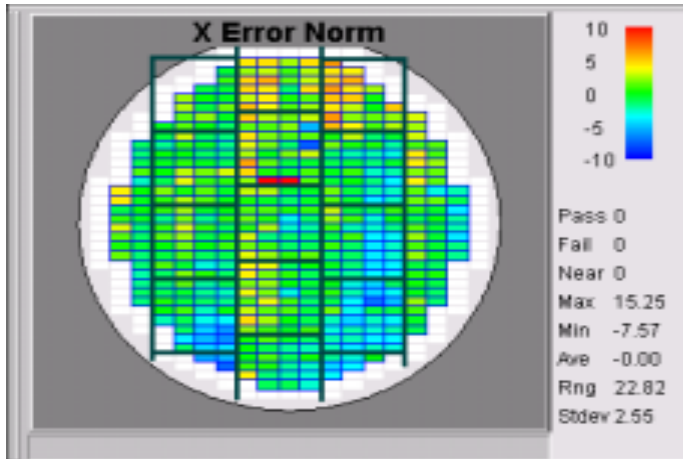
Example # 5

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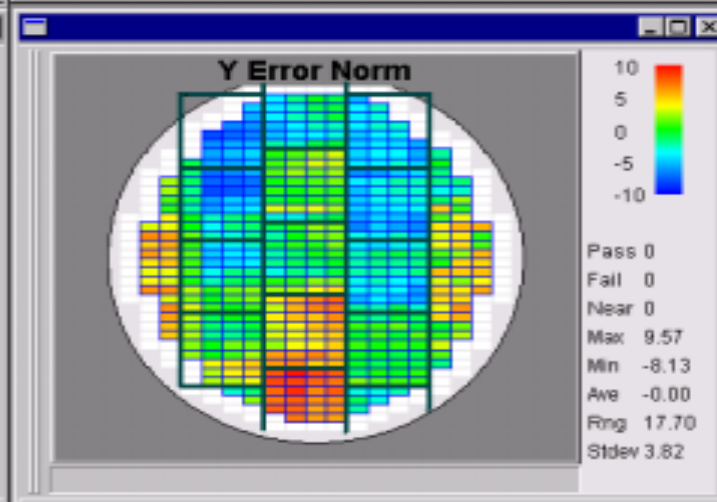
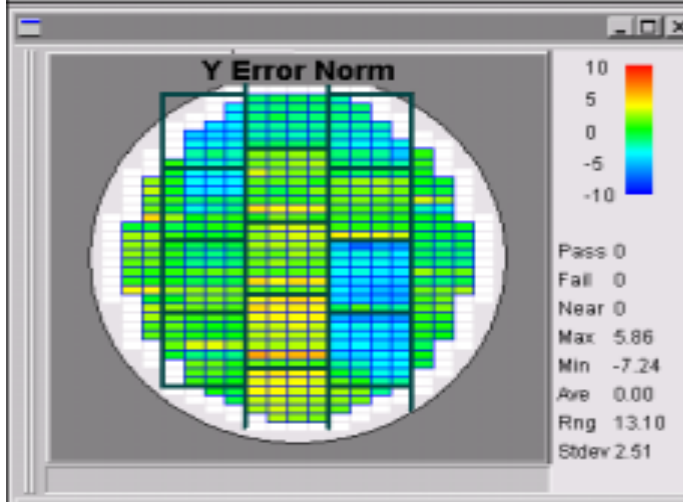
Ambient

135 C

X



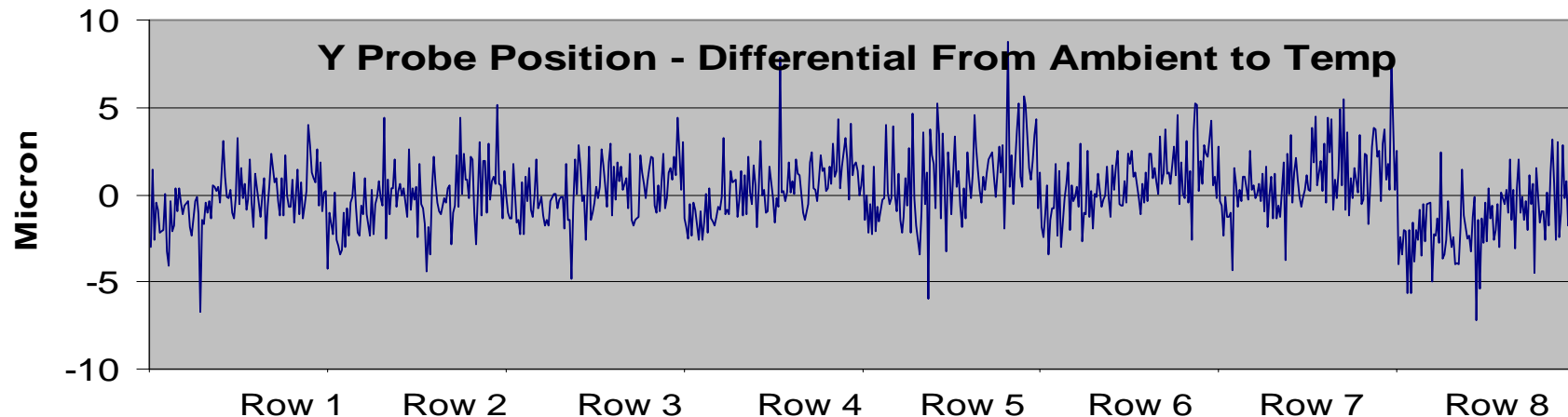
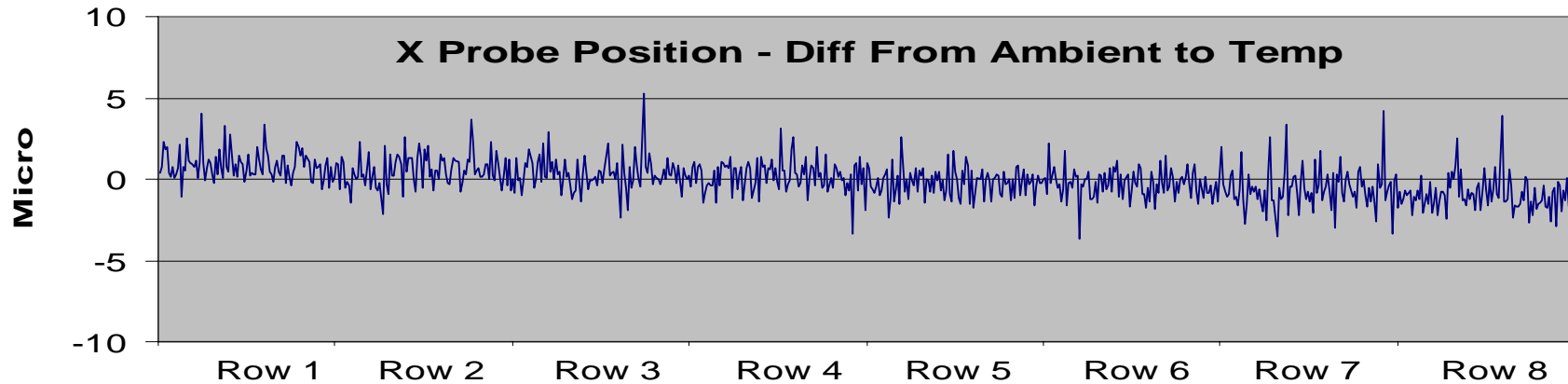
Y



Multi-Dut at Temperature

Example # 5 - Probe Position Differential

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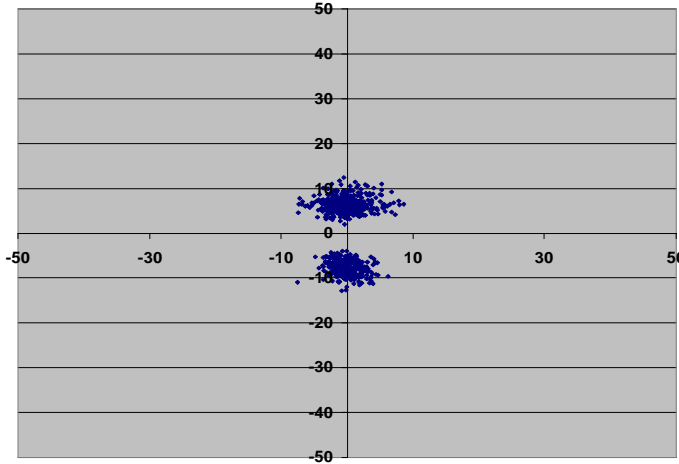
Multi-DUT at Temperature

Example # 5 - Probe Card Performance

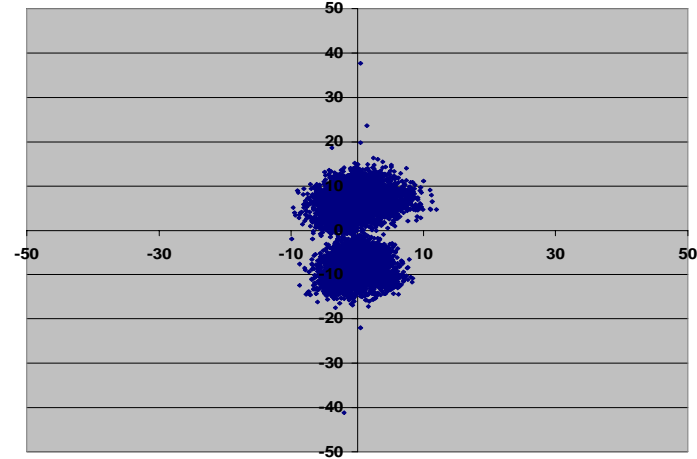
www.appliedprecision.com

Ambient

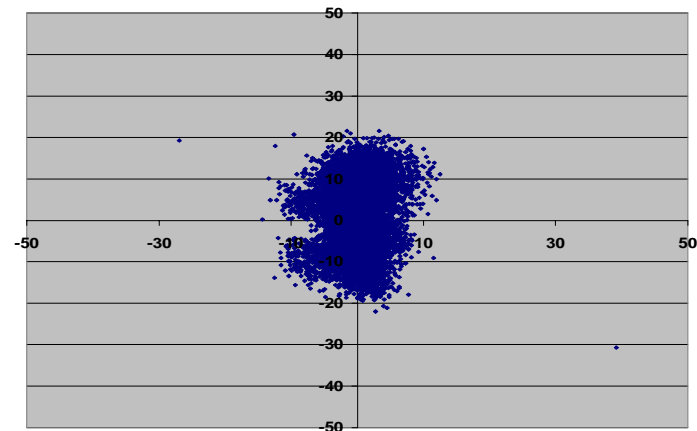
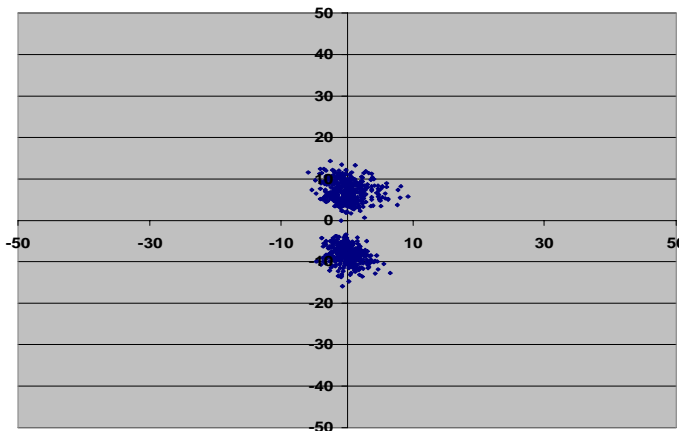
Probe Card



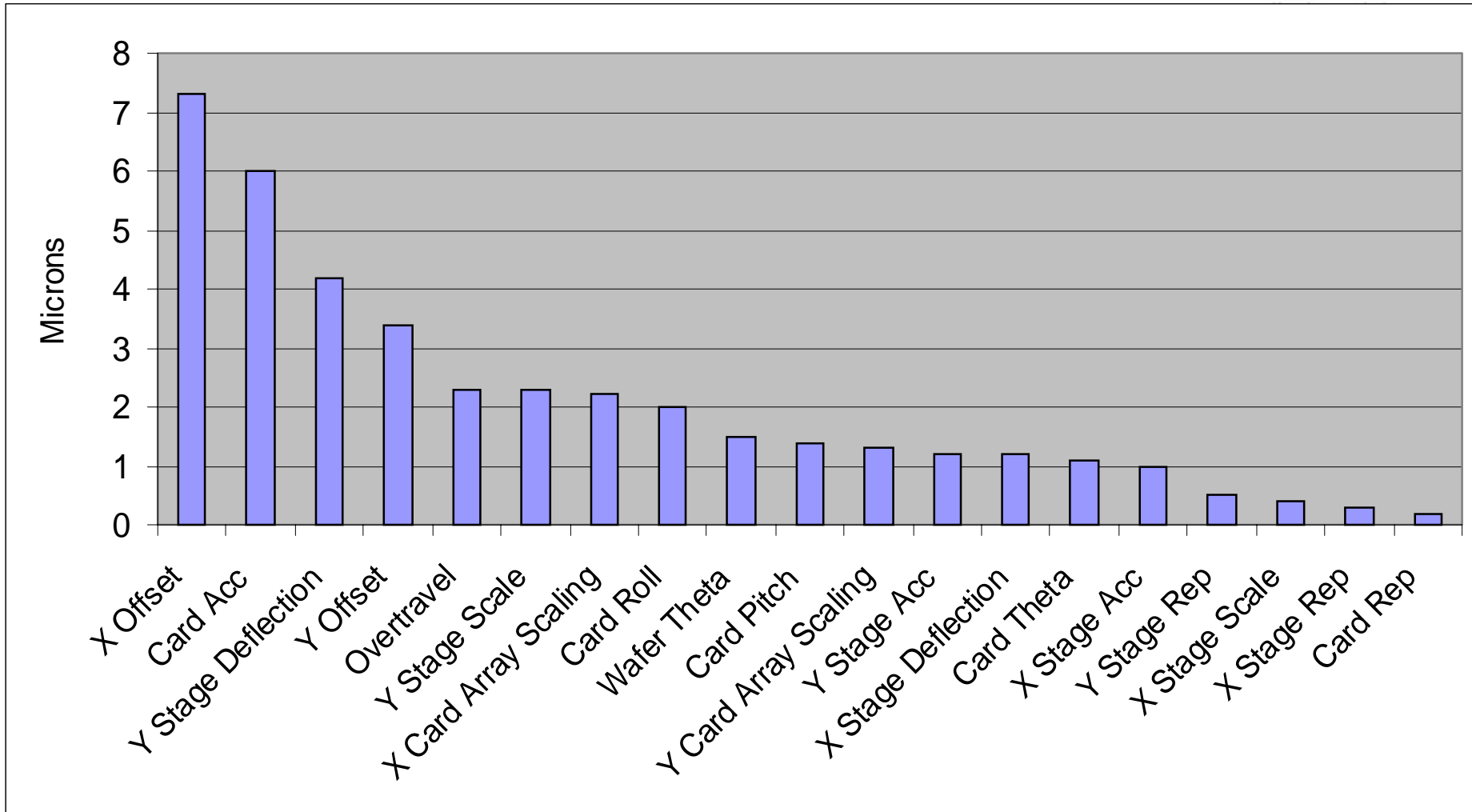
Scrub Marks



135° C



Process Report Card





What If?

Calculate Process Capability (Cpk)

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- Calculate a overall process Capability #
 - $Cpk = \text{Spec Width} / \text{Process Spread}$
 - $Cpk = \text{Pad Size} / (v1+v2+v3+v4\dots)$
- Process Improvement Evaluation
 - What if X,Y Setup variation is improved?
 - What if the probe card is more accurate?
 - What if the Pad size is changed?
 - What if the prober has a stiffer stage?
 - What if...



Conclusions

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- View the probing process as one system
- Measure the variations in the process
- Focus on the key parameters that influence the process
- Continually evaluate improvements or changes to the process



Acknowledgements

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Engineering Technician
Micron
- Bob Heiligenberg
Semiconductor Product Line Manager
Applied Precision Inc.
- Ryan Hardie
waferWoRx Project Manager
Applied Precision Inc.
- Ron Metzger
Test Engineer
Applied Precision Inc.