Thermal Characterization at Wafer Test: Experiments and Numerical Modeling

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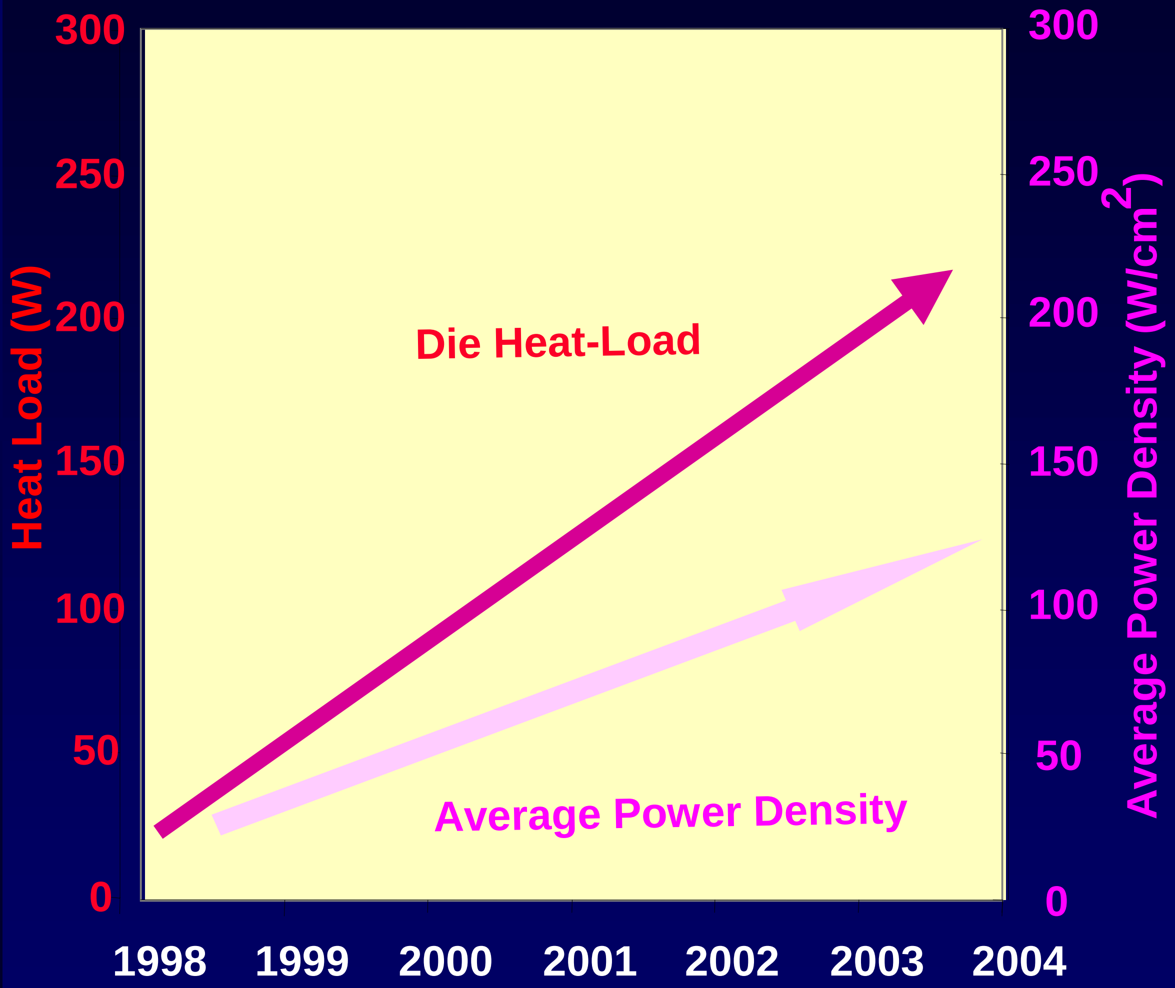
Outline

- Industry Power Trends
- Power Dissipation Perspective
- Thermal Solution Approach at Wafer Sort
- Thermal Test Chip Experiments
- Thermal Test Chip Modeling
- Conclusions

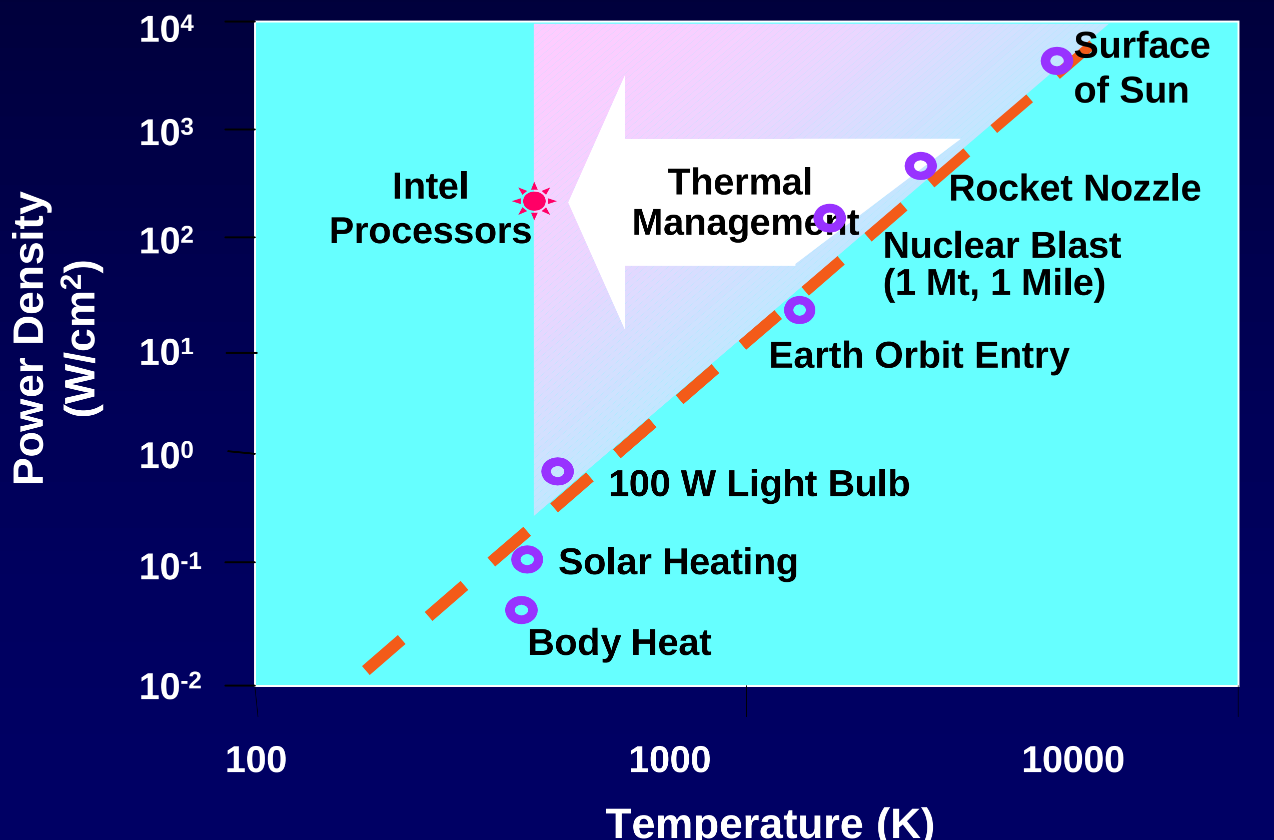
Semiconductor Industry Power Trends (Seri Lee)



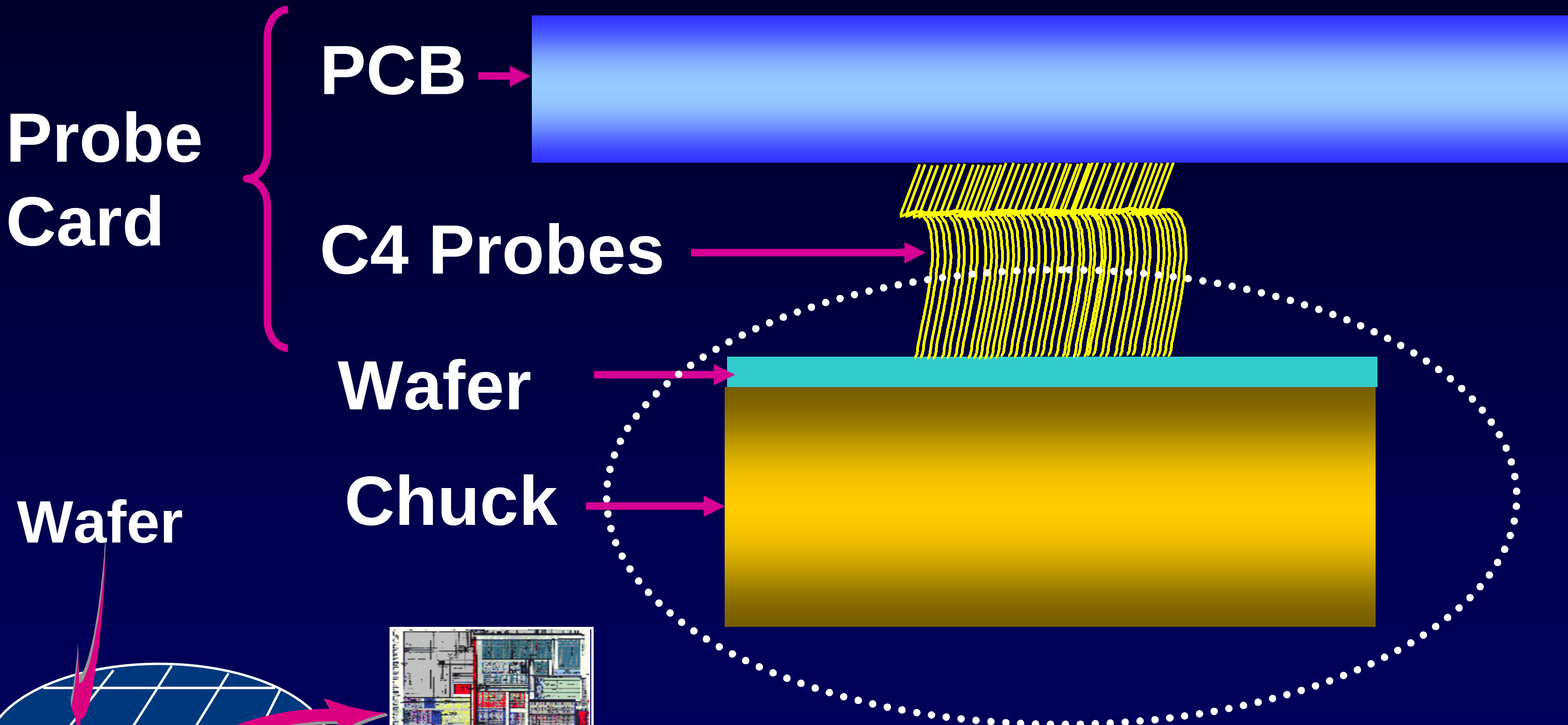
If trends continue, device power will approach 250 W and average power density will approach 150W/cm^2 in the next few years.

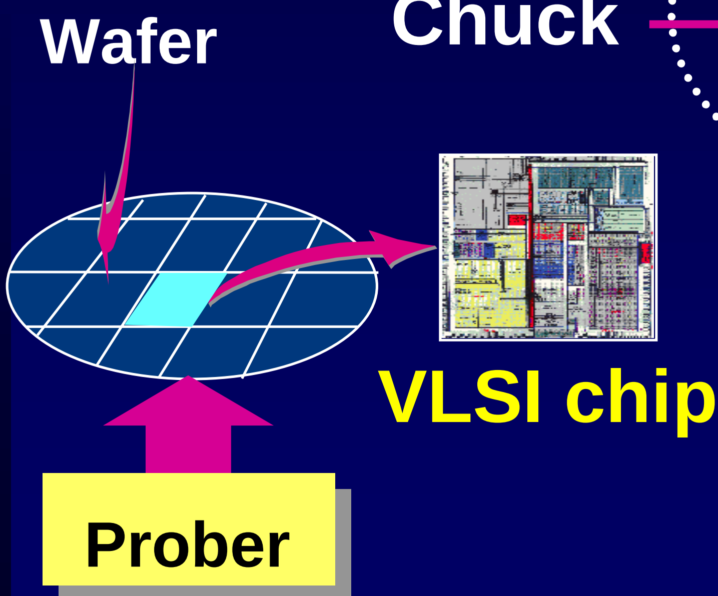
Power Dissipation Perspective (Seri Lee)

- A goal at wafer sort is to dissipate a large power density, while maintaining a relatively cold die temperature (Tj).



Thermal System at Wafer Test





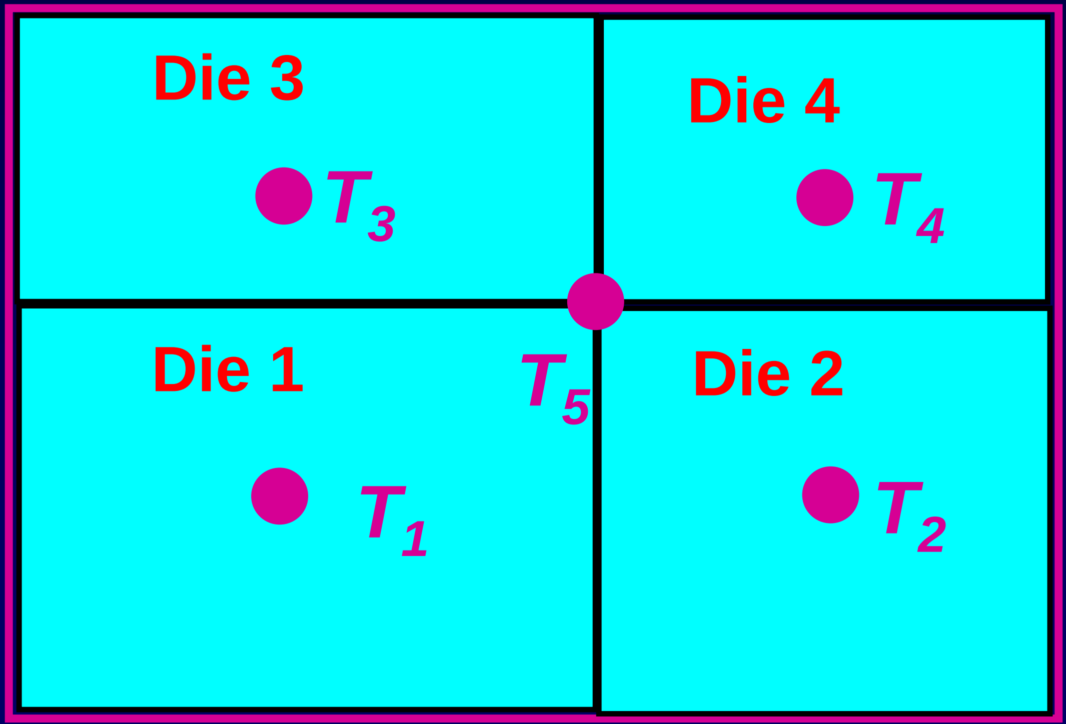
What is the Tjrise of the die that is powered?

Thermal Solution Approach

- Collect thermal data with a test chip to
  - Characterize Tj as a function of different variables
  - Quantify Tj improvement caused by changing wafer sort system
  - Calibrate thermal simulation models
- Create thermal simulation models to
  - Predict Tj of real product prior to first silicon (N+2 generations)
  - Understand Tj sensitivity to different variables
  - Explore potential benefits of changes without executing physical measurements

Thermal Test Chip

- The Thermal Test Chip is composed of 4 subdie
  - Each subdie contains a heater which can be powered independently of the other subdie
  - There are 5 temperature sensors, T_i: one in each of the four subdie and a fifth in between the subdie

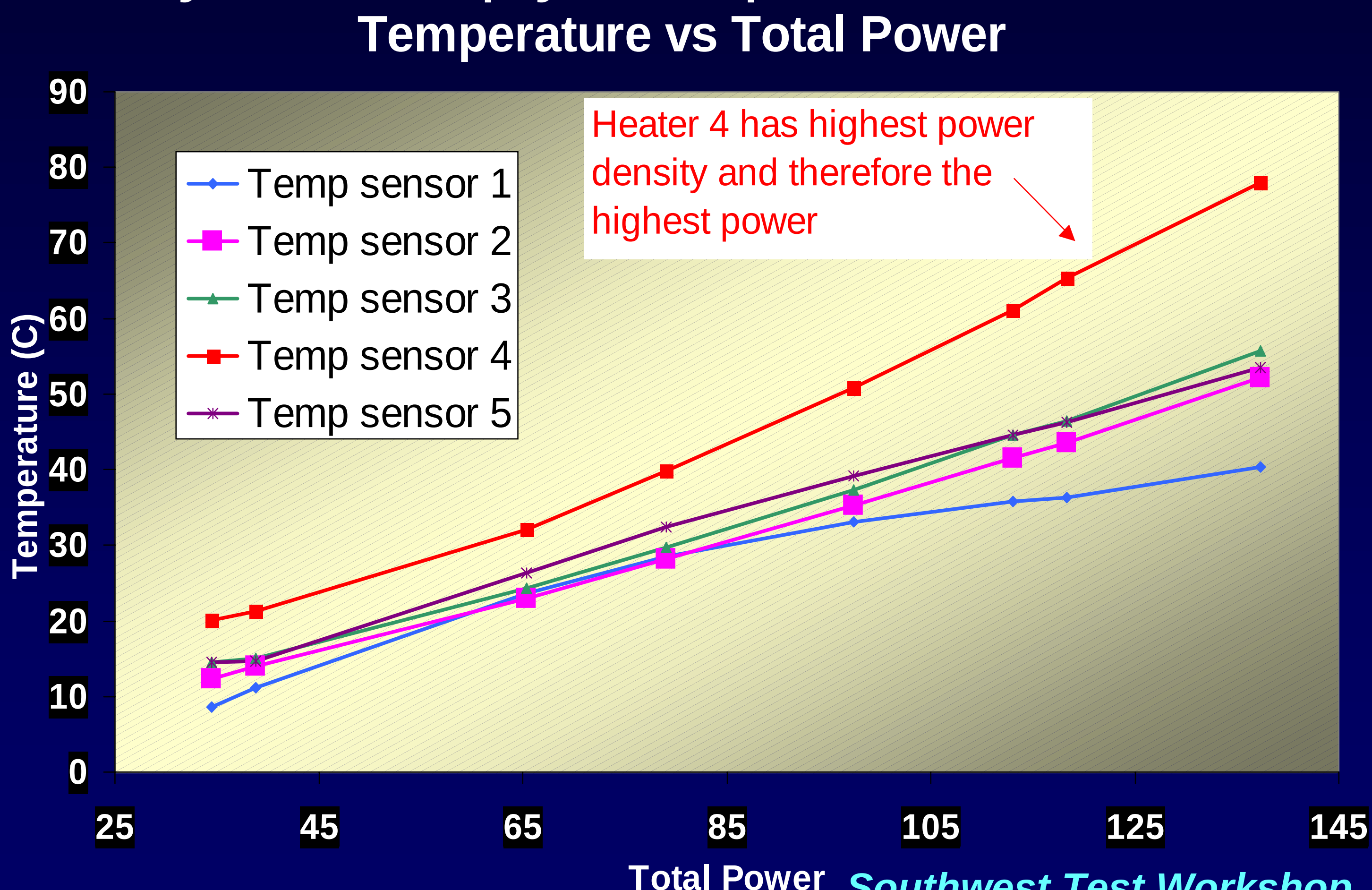


● =Temperature sensor

	Area (cm2)
die 1	1.5
die 2	0.9
die 3	1.1
die 4	0.6
total	4.2

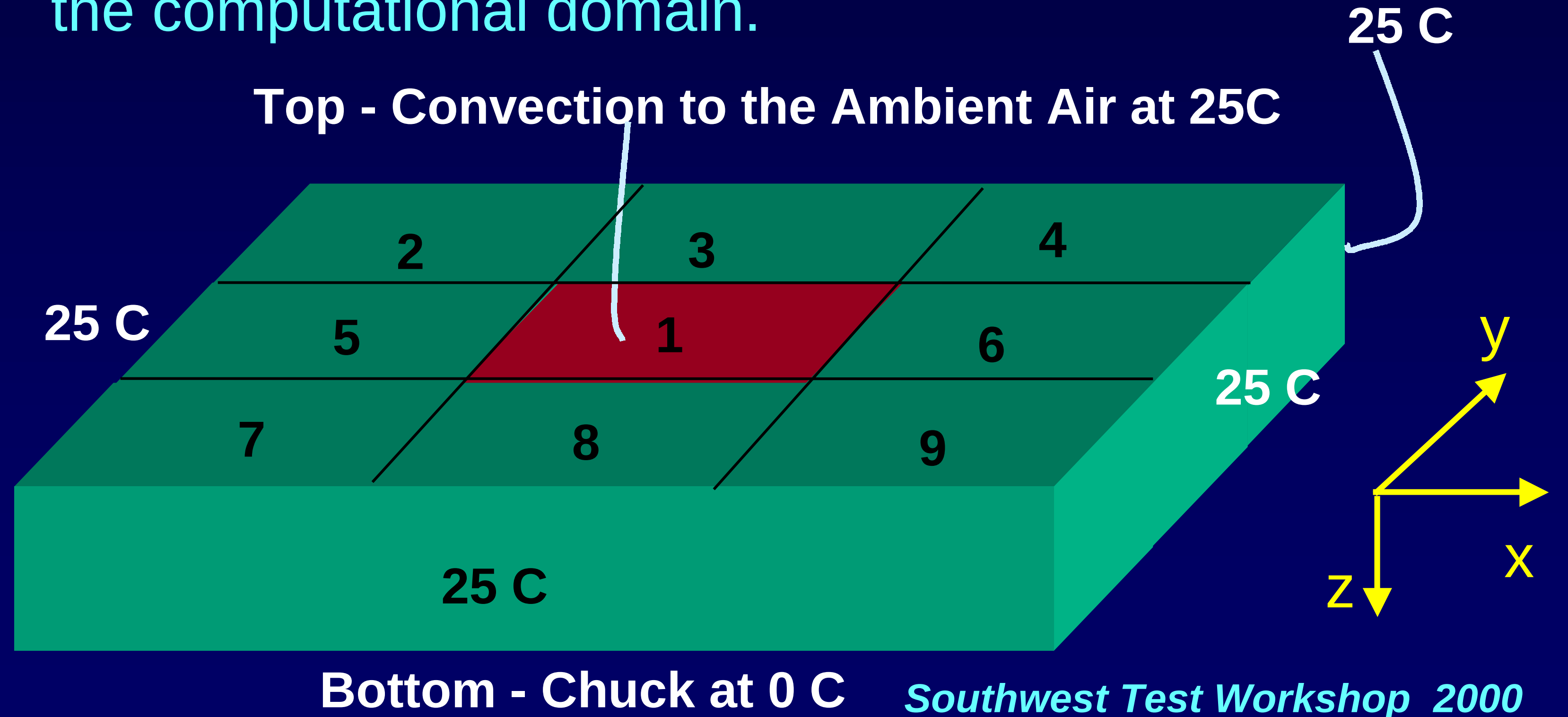
Temperature vs Power: Non-uniform Power Density (Thermal Test Chip Data)

- Die temperature depends on local power density, not simply total power



Creation of Simulation Models

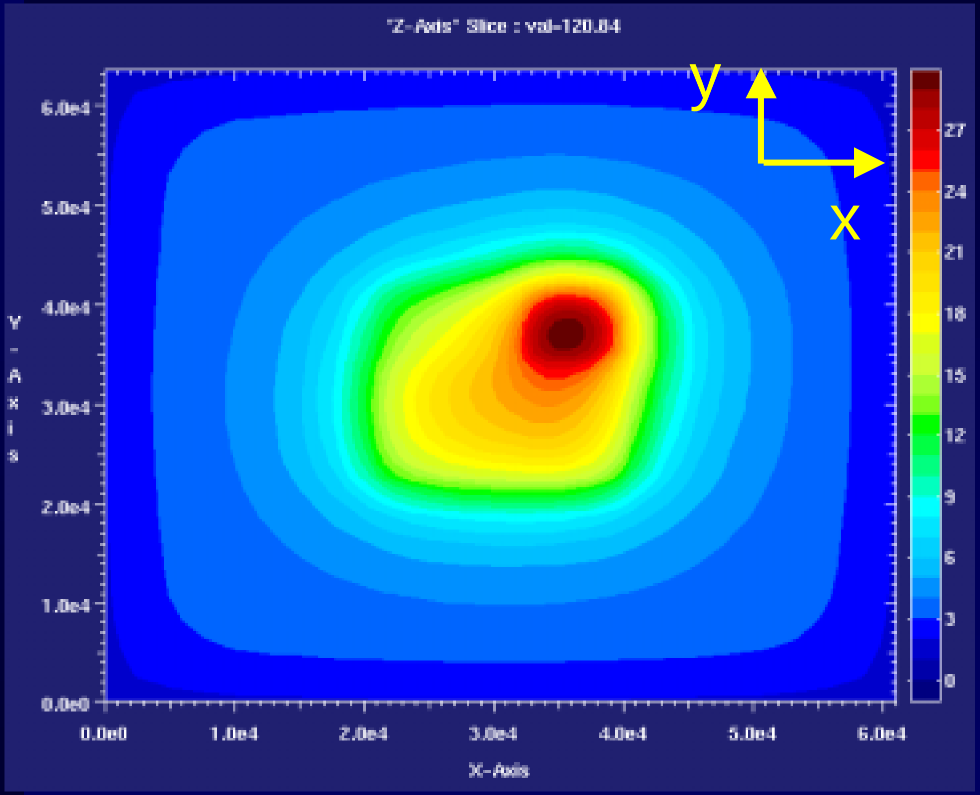
- Simulations were done by using Intel internal tool TPRsim (Temperature Simulation for Performance and Reliability)
- Provides junction temperature based on estimated functional unit blocks power dissipation across the die
- 8 dies surrounding powered die are included as part of the computational domain.



Thermal Characterization Data

All 4 heaters are powered (Low Power)

Simulations



Max Simulated temp = 29.78 C

Difference ~ 6 %

Example 1:

53 W

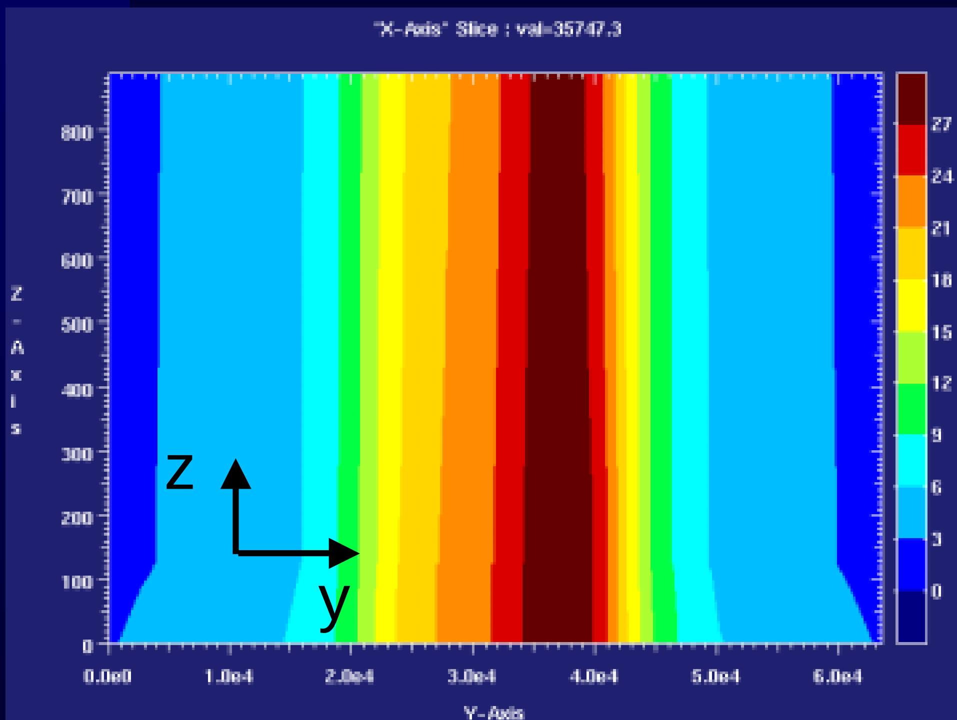
15 W/cm^2

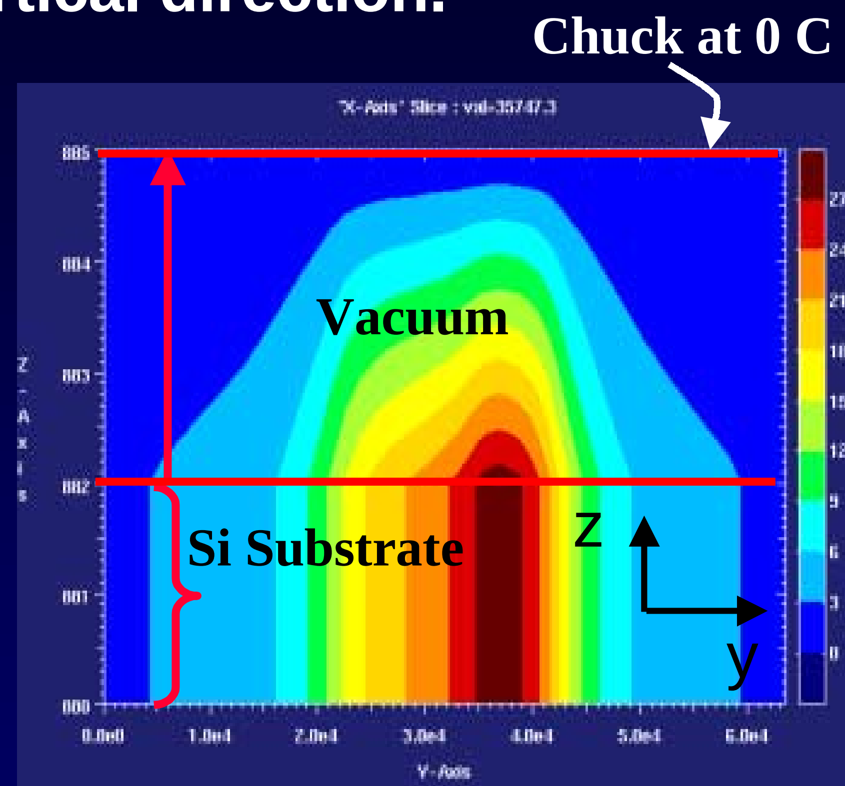
heater 3 **sensor 3** 7 W 8 W/cm^2 17 °C	**heater 4** **sensor 4** 17 W 28 W/cm^2 28 °C
heater 1 **sensor 1** 16 W 12 W/cm^2 21 °C 22 °C **sensor 5**	**heater 2** **sensor 2** 13 W 14 W/cm^2 20 °C

(Experimental Measurements)

Temperature in yz plane (constant x)

- **Heat transfer in the lateral direction is much less significant than in the vertical direction.**

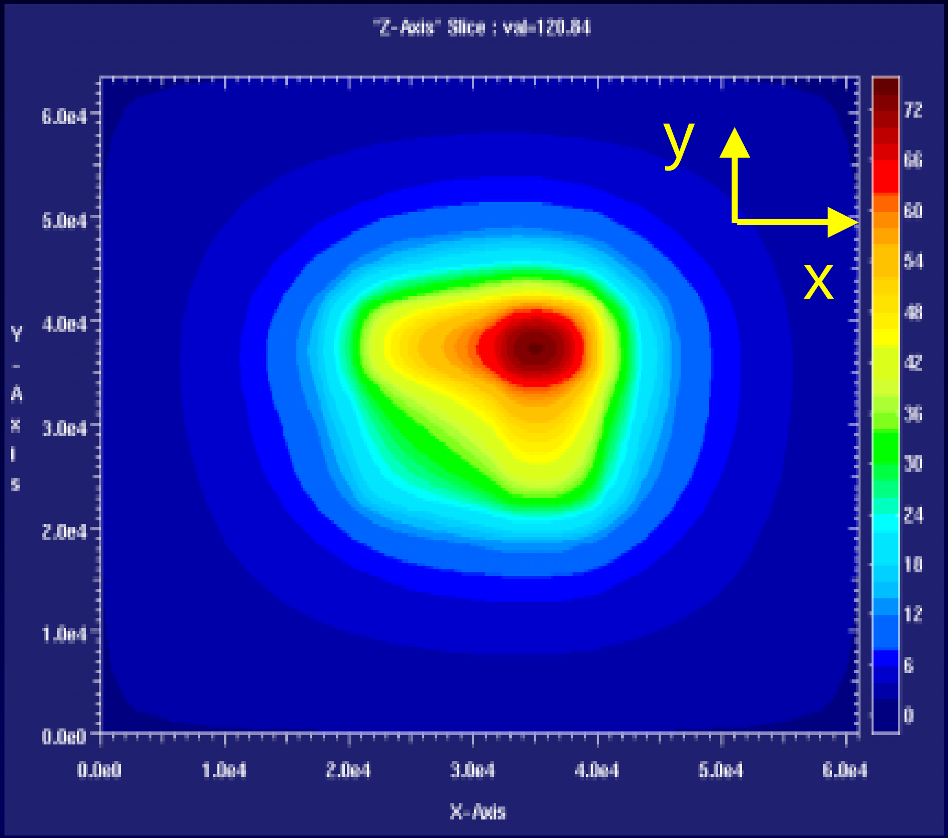




Sharp temp gradient between Si substrate bottom and top of the Chuck

Zmin = 880 , Zmax = 884.99

When all 4 heaters are powered (High Power)



Example 2:

138 W

37 W/cm²

heater 3 sensor 3 38 W 44 W/cm² 56 °C	heater 4 sensor 4 44 W 75W/cm² 78 °C
heater 1 sensor 1 53 °C sensor 5 22 W 16 W/cm² 40 °C	heater 2 sensor 2 34 W 37 W/cm² 52 °C

Max Simulated temp = 74.39 C

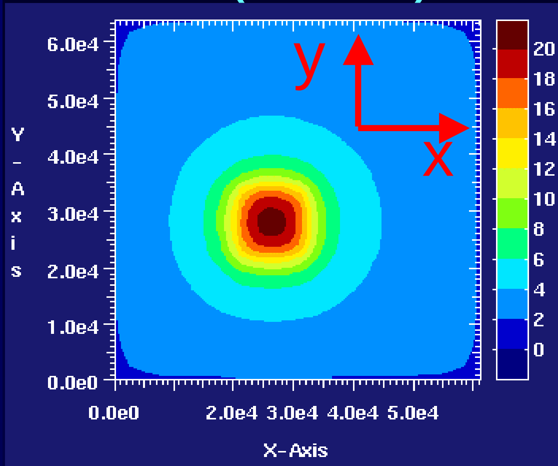
(Experimental Measurements)

Difference between model and experiment = 4.6%

Simulations data from the model compares to experiment within 6%.

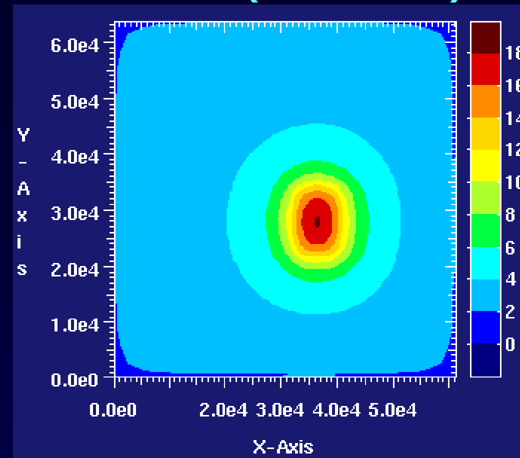
Uniform Power Dissipation of 14.5 W/cm^2

Heater 1 (1.5 cm^2)



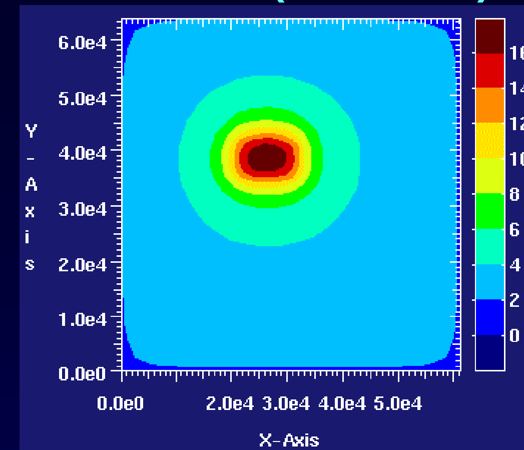
Max Tjrise = 21.03 C

Heater 2 (0.96 cm^2)



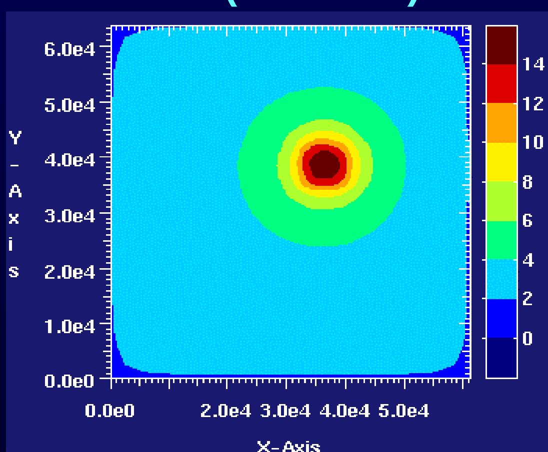
Max Tjrise = 18.3 C

Heater 3 (1.05 cm^2)



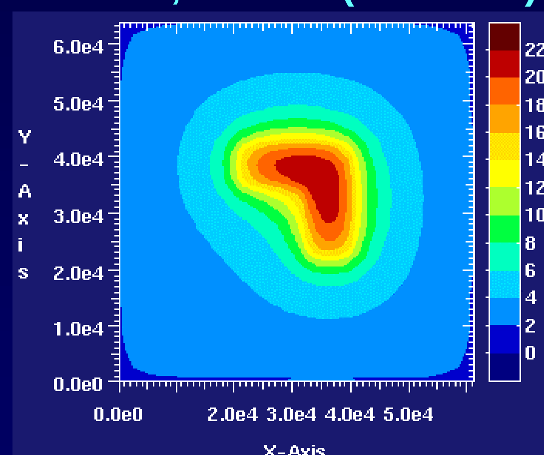
Max Tjrise = 17.84 C

Heater 4 (0.6 cm^2)



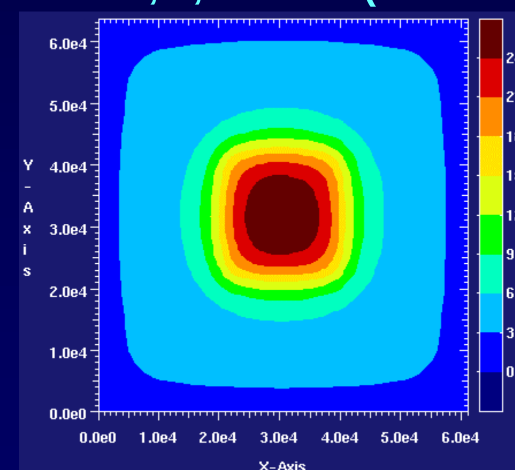
Max Tjrise = 15.7519 C

Heater 2, 3 and 4 (2.7 cm^2)



Max Tjrise = 22.0105 C

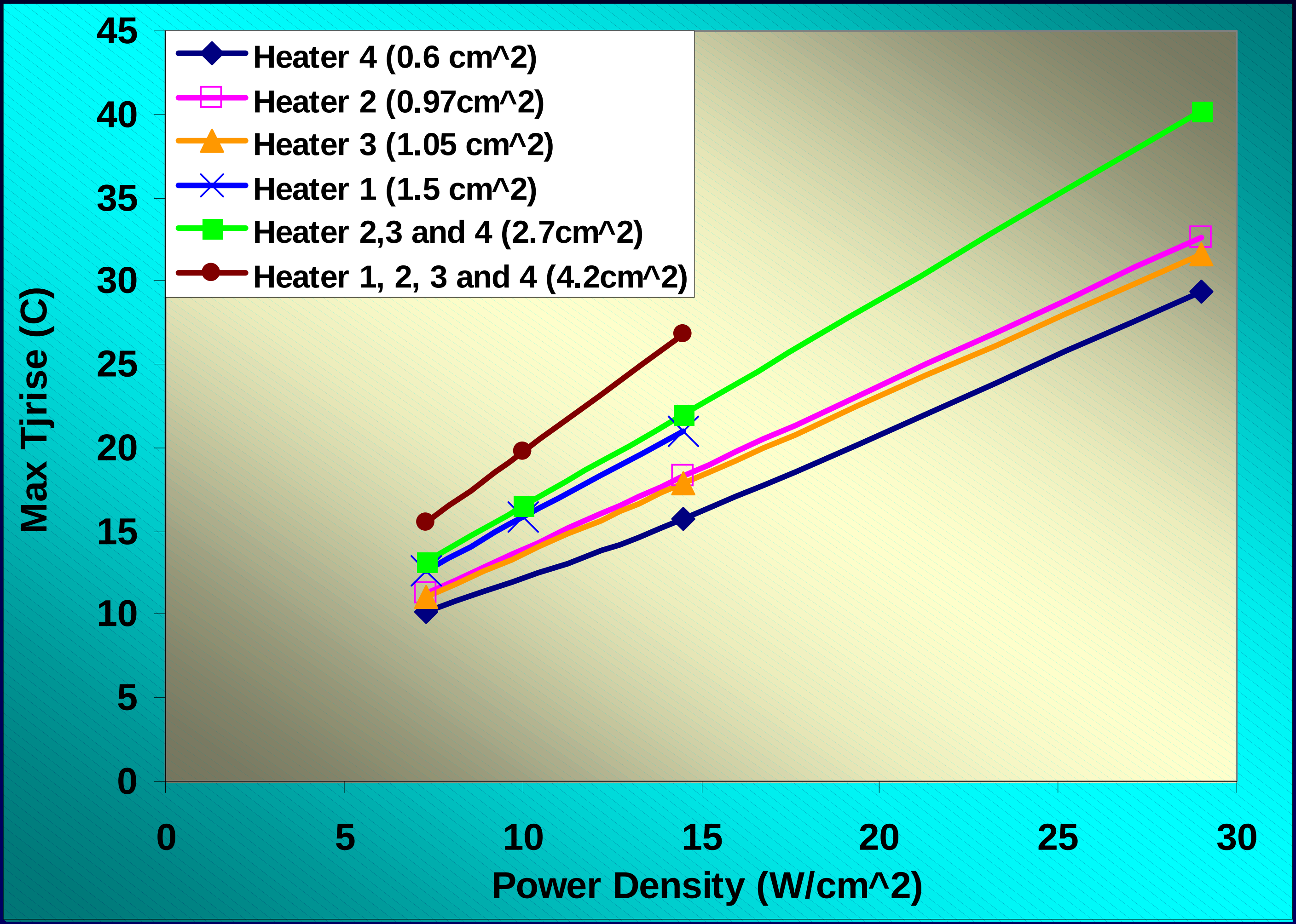
Heater 1, 2, 3 and 4 (4.2 cm^2)



Max Tjrise = 26.825 C

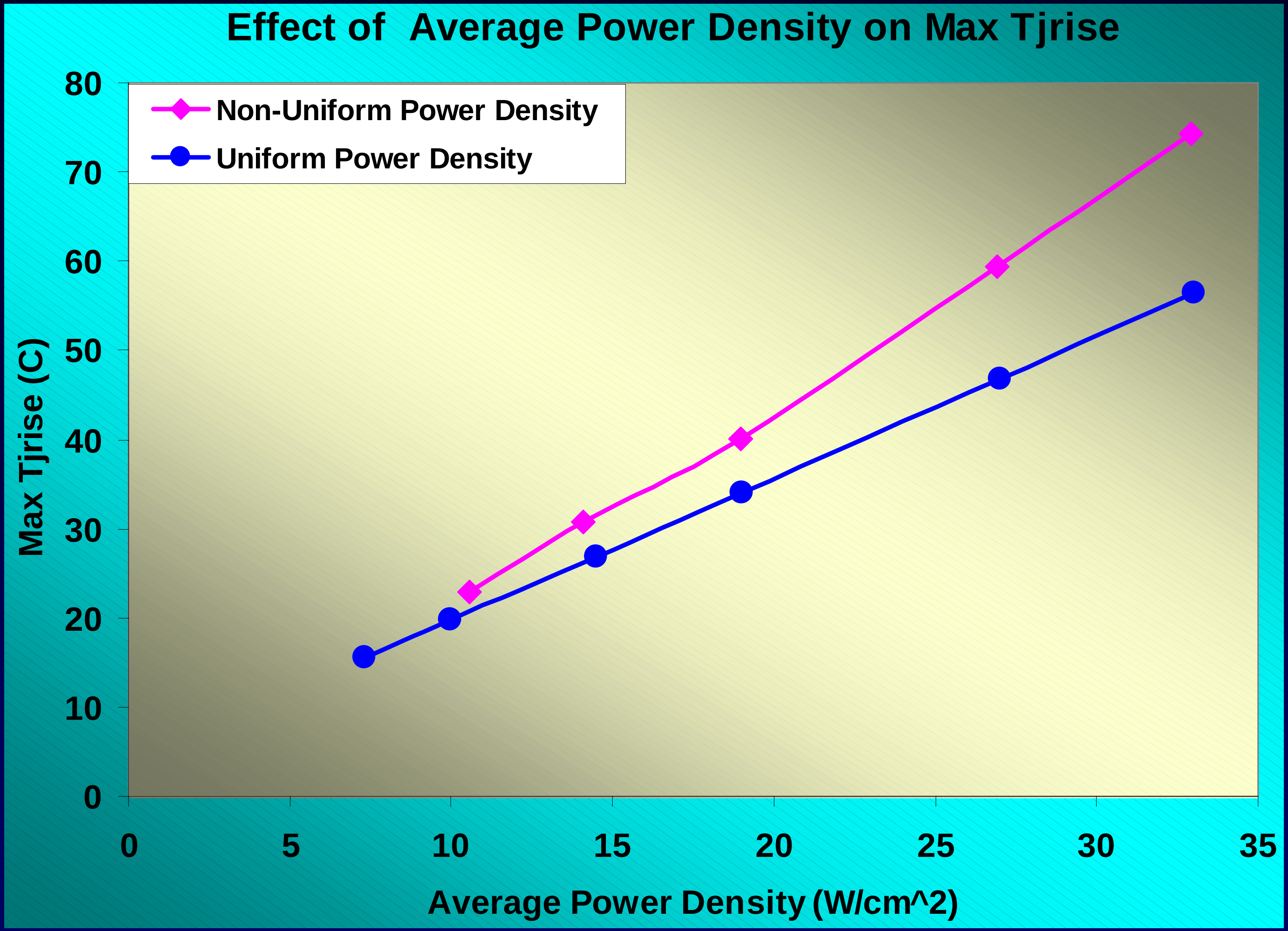
Heaters with same power density acts like a common heat source for heat dissipation.

Effect of Uniform Power Density and Die Size



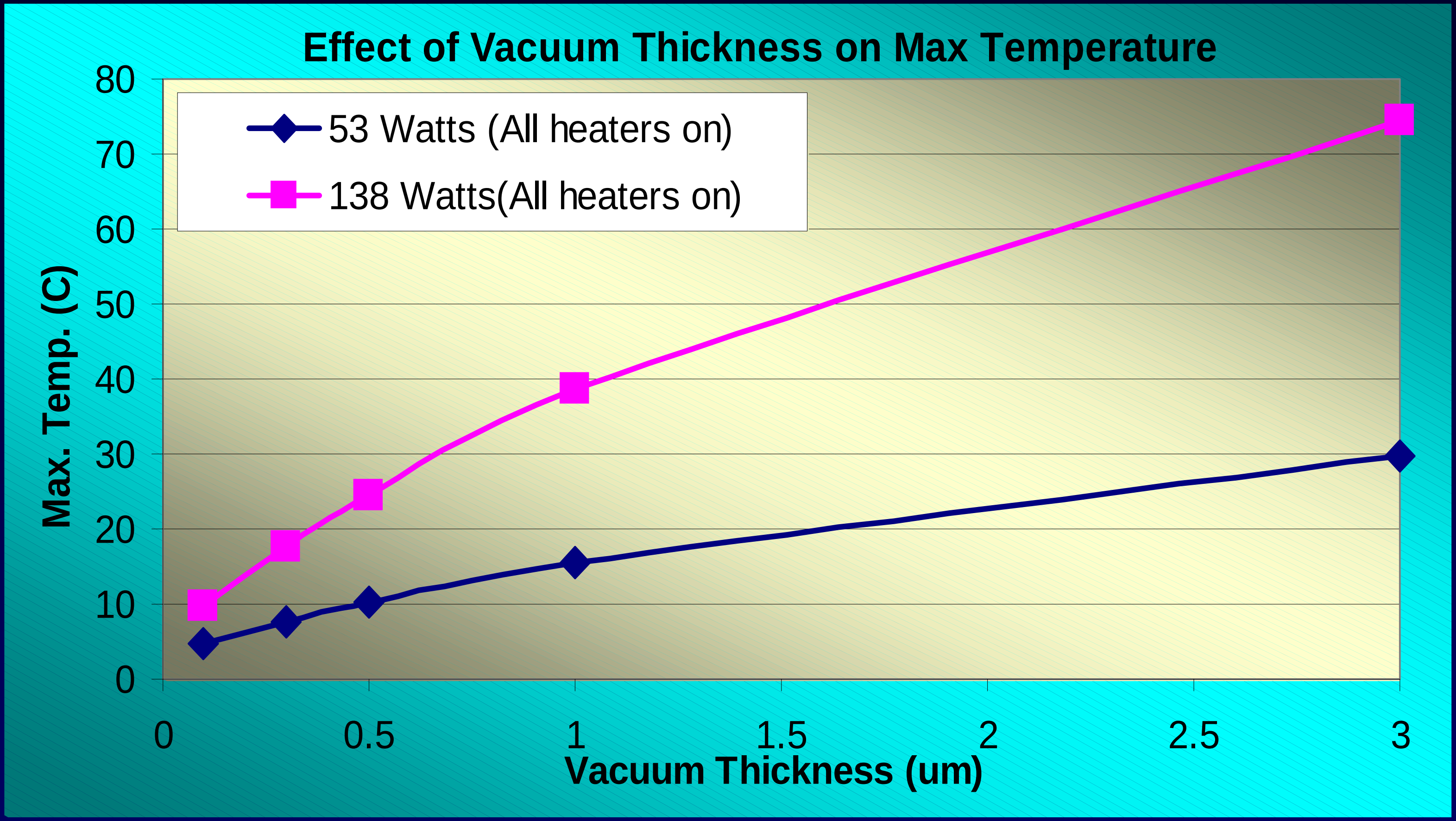
At the same uniform power density, increasing the die size increases max Tjrise.

Uniform vs. Non-Uniform Power Dissipation



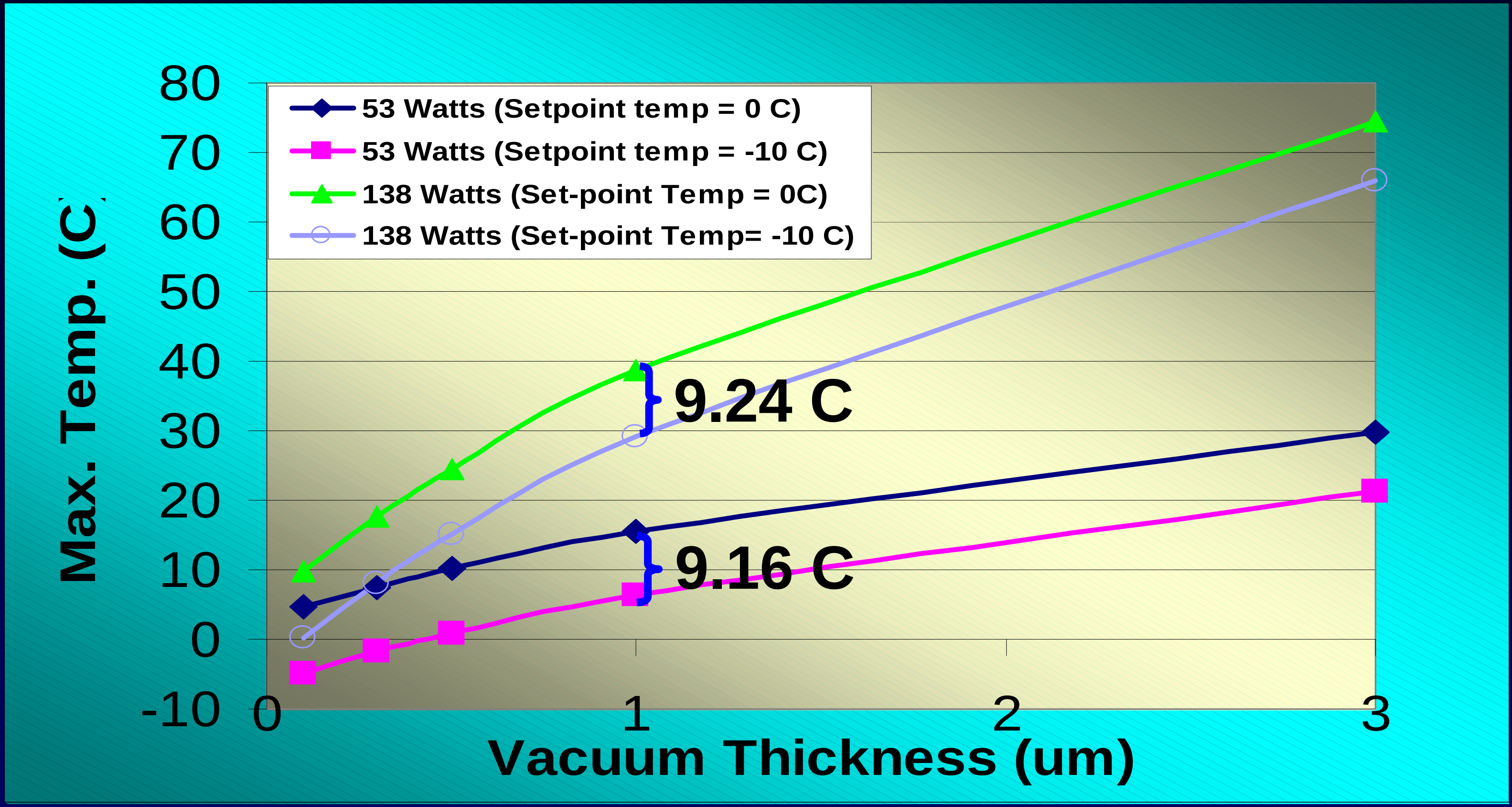
At the same average power density, max Tjrise for a non-uniform power density is higher than the uniform power density.

Effect of Vacuum Thickness on Tj



Decreasing vacuum thickness decreases max Tjrise keeping the vacuum thermal conductivity constant.

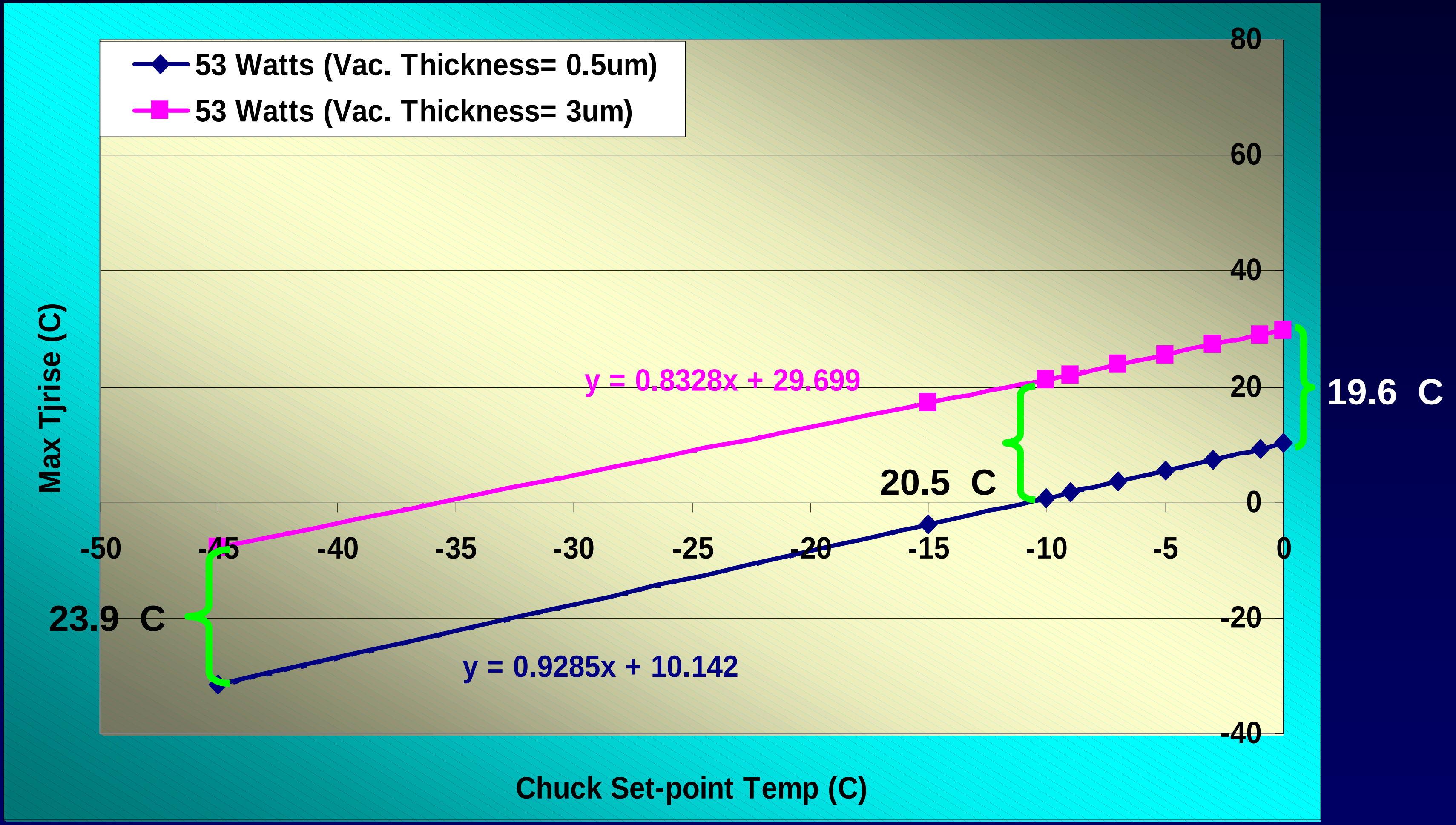
Effect of Vacuum Thickness and Chuck Set-point Temp. on Tj



Changing the vacuum thickness from 0.1um to 3um and then, decreasing the set-point temperature of the chuck top from 0 C to -10 C decreases the Tjrise by ~ 9 C.

Effect of Chuck Set-point Temp. on Max Tjrise

All 4 heaters powered (Low Power)



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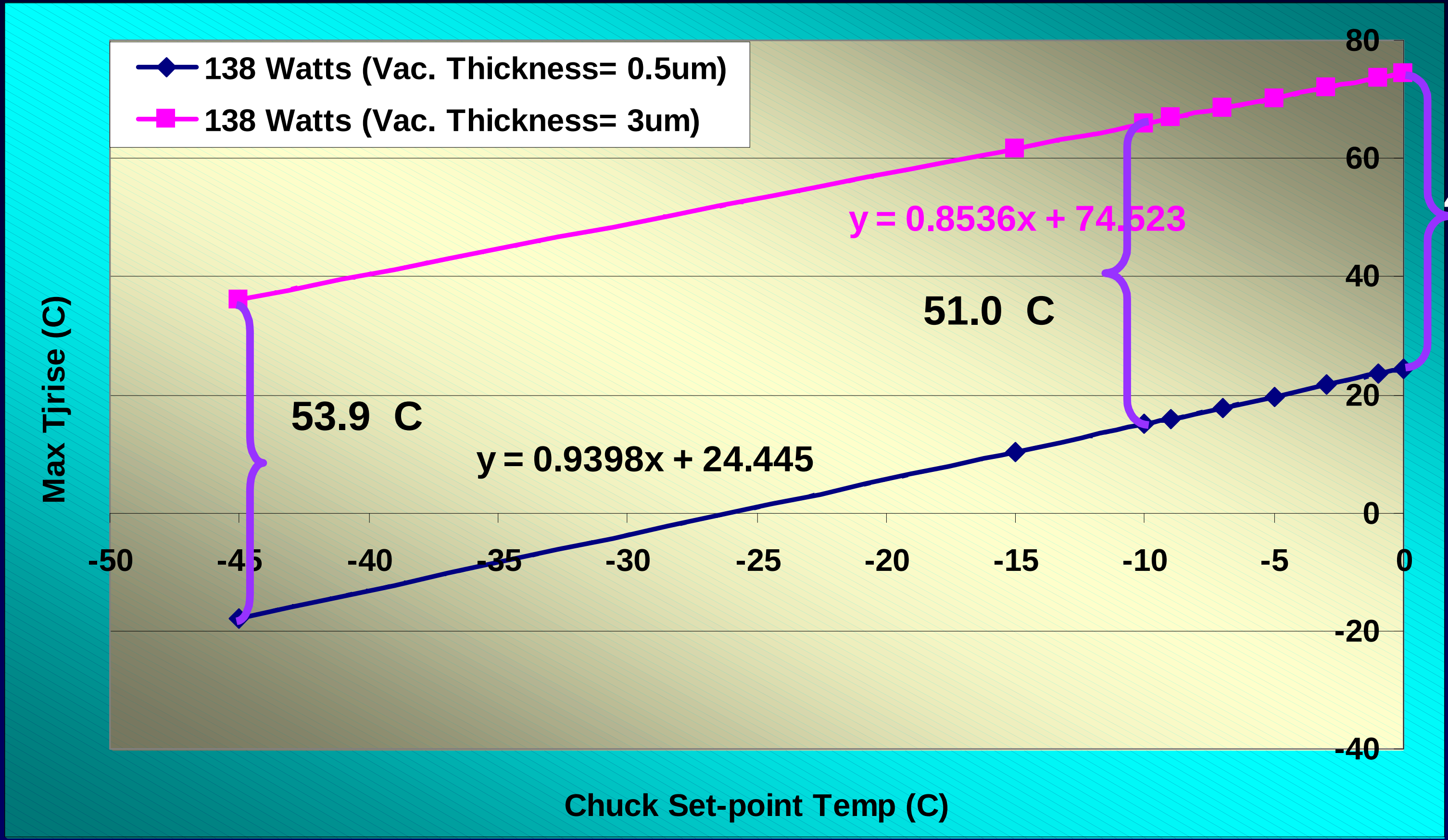
Effect of Chuck Set-point Temp. on Max Tjrise

All 4 heaters powered (High Power)



As the set-point temperature decreases, the max Tjrise decreases at a higher rate.

Summary and Conclusions

- A Thermal Test Chip is being used to collect empirical die temperature data under controlled conditions
- Thermal simulation models have been created and correlated to experimental data within 6%
- Sensitivity studies have been done assessing effects of
  - lowering chuck set-point temp.
  - modulating the thickness of the vacuum conductivity.
- Sharp Temperature gradient between the bottom of the Si substrate and the top of the chuck
  - Thermal Interface is one of the most critical parameter to determine max Tjrise.
  - Decreasing thermal interface thickness decreases max Tjrise.
- For the same average power density case, the non-uniform power dissipation case has a higher max Tjrise than the uniform power dissipation case.
- Decreasing the set-point temperature of the top of the chuck decreases max Tjrise.

Next Steps

- Next steps: look at effects of
  - alternate thermal interface material
  - wafer and prober chuck roughness
- Expected outcome
  - better understanding of gaps between future thermal needs and solutions
  - improved wafer sort thermal solutions