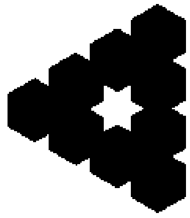

Impact of DFT Techniques on Wafer Probe

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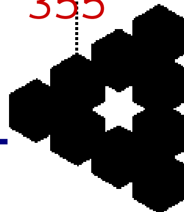
LogicVision®
The Embedded Test Company™

Agenda

- Introduction
- Test Roadmap
- Cost Factors
- DFT Options
- Embedded Test
- Impact on Probe
- Summary & Conclusions

1999 ITRS Test Roadmap

	'99	'01	'03	'05	'08	'11	'14
Technology node	180nm	130nm	130nm	100nm	70nm	50nm	35nm
DUT Period (ps)	830	700	580	500	400	340	260
Tester OTA (ps)	200	160	130	100	100	100	100
DUT req'd Accuracy (ps)	42	35	29	25	20	17	13
Max Pin-Count	768	1024	1024	1024	1280	1408	1472
Vector Count (M)	64	128	256	512	1024	4096	4096
Supply Current (A)	200	220	242	266	293	322	355



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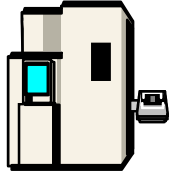
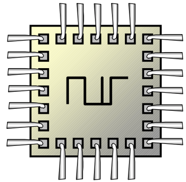
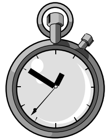
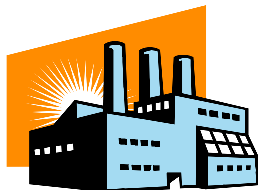
Test - Cost Factors









- ATE
  - Tester Complexity
- Tooling Costs
  - Probe Cards, Load Boards
- Test Time
  - Parametrics, Scan, Load time,…..
- Test Development Effort
  - Vector generation, program complexity, debug
- Test factors affecting Yield
  - ATE accuracy, analysis time
- Overall Manufacturing Costs

Test Cost Estimates

Failure Anal. 10%

Debug 20%

ATE & Tooling 40%

Test Dev. 30%

High End ATE - Cost Factors

- Timing Subsystem
  - OTA < 100ps (driven by functional vectors)
  - System clocks approaching 1Ghz
  - Timing flexibility is costly
- Pin Count
  - Flip Chip roadmap to 1500 - 3000 functional I/O’s
- Pattern Sources
  - Large Scan and Functional Memory requirements
  - Memory pattern generator / analog sources
  - At-speed multiplex -- cost & accuracy challenge

Tester Costs: High-End System

Tester Cost Trends

- Logic ATE cost/pin essentially flat for last 20+ years
  - $5K - $10K/pin -- high end
  - $2K - $4K/pin -- low end
- Features and Capabilities have increased dramatically
  - Frequency, timing flexibility, accuracy, vectors
- ATE costs have scaled with increasing pincount

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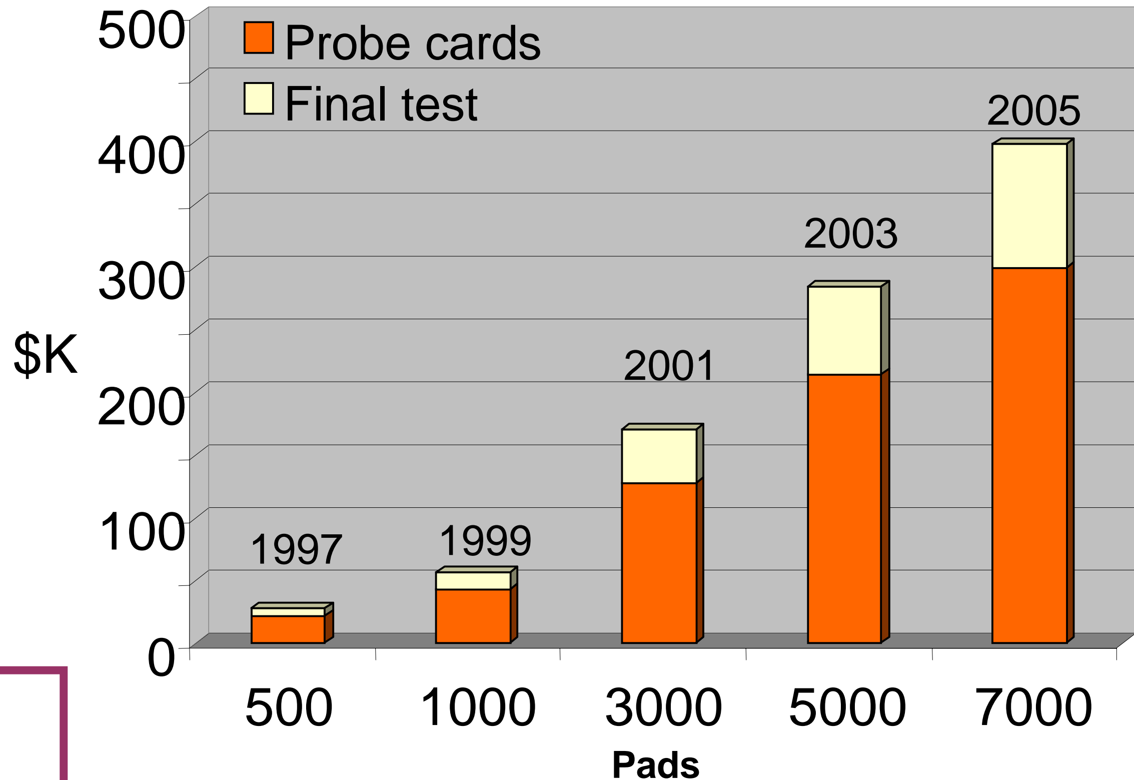
Tooling Costs

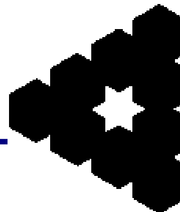
Probe Costs

Epoxy:	$10-$20/pin
Cobra:	$30-$60/pin
Membrane:	$40-$80/pin

Probe Card costs scale with pincount



Flip-chip example:
Cost = $57 total/pin



What is being done about it?

- Captives / Internal Solutions:
  - IBM - committed for decades to LSSD, WRPG, BIST
  - Texas Instruments - VLCT (low cost tester) project
  - Others………..
- Commercial:
  - Fluence / Credence - BIST (Memory & Analog)
  - Mentor Graphics - BIST (Logic & Memory)
  - Synopsis - BIST (Memory)
  - LogicVision - Embedded Test (Memory, Logic & Analog BIST)

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Conventional Functional Test

CPU
Tester O.S.

Power Supplies
Timing
Formatting
Vectors
Pattern Control
Memory APG
Clocks

High pincount Interface & probecard

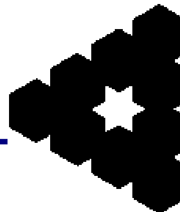
Logic
Logic
µP
Mixed Signal
Core
Memory
Logic
Memory
Memory
Logic

Challenges:

Expensive H/W
Difficult to deliver accuracy

High density
High Bandwidth

Accessibility to functions
Test Re-use difficult



SCAN Methodologies

CPU
Tester O.S.

Power Supplies
Timing
Formatting
Vectors
Pattern Control
Memory APG
Clocks
SCAN memory

High pincount Interface & probecard

Increased accessibility & fault coverage

Logic
Logic
µP
Mixed Signal
Core
Memory
Logic
Memory
Memory
Logic

Challenges:

More expensive H/W
Difficult to deliver accuracy

High density
High Bandwidth

Test Re-use difficult
Memory Test is SLOW

Test Time for Scan

Test time = (M flops/ **N** scan chains) x #vectors × 1/$\mathbf{f_{CLK}}$

- ATPG scan: targeted, efficient, but N and f_{CLK} limited by pins & ATE

f_{CLK} =20MHz

N=32

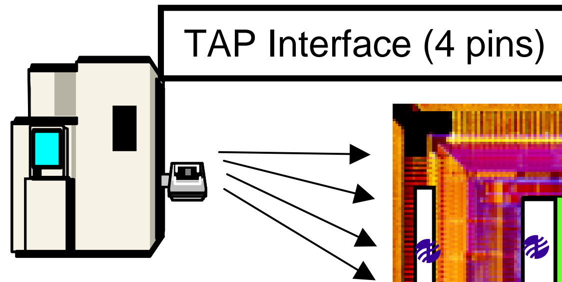
Scan chain

Scan chain

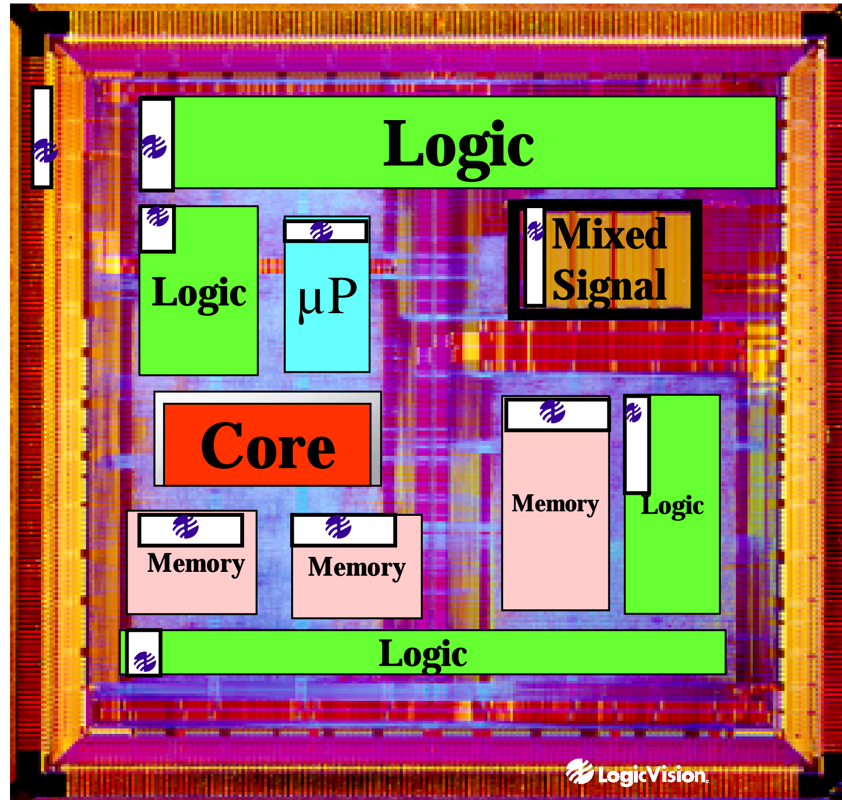
Scan chain

scan chains limited

Embedded Test Solution



Low Cost Digital Tester
- Power Supplies
- Clocks
- TAP support
- Test Control
- Min. vectors/error catch

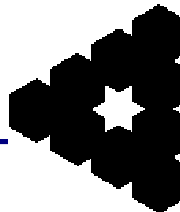


Reduced pin Interface

No complex timing

Minimal Vector Memory

No Limits to # scan chains



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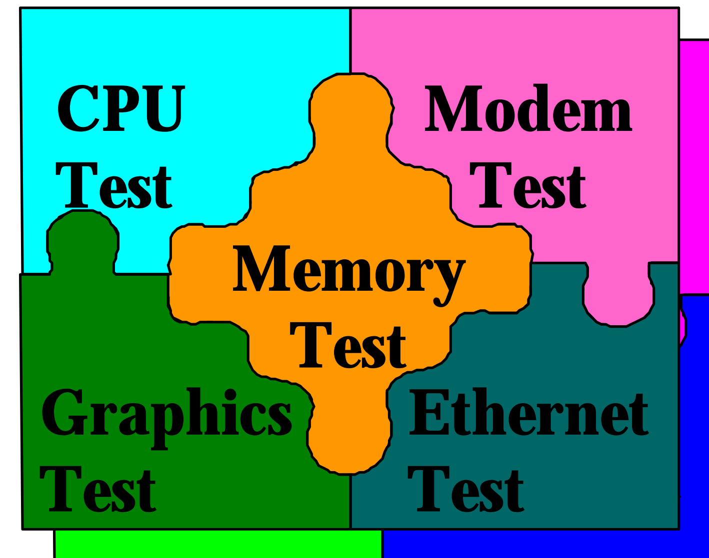
Test Time for LogicBist

Test time = (M flops/ **N** scan chains) x #vectors $\times$ 1/$\mathbf{f_{CLK}}$

- BIST scan: unlimited chains and scales with f_{SYS}

Embedded Test Enables

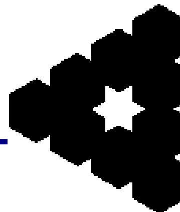
- On-chip Test at Speed
  - Independent of tester performance
- Power management during test
- High-bandwidth internal access
  - Increased fault coverage
- Re-use at test
  - Test Structures tied to cores
  - Speeds test development
- Reduced test cost
  - Lower cost ATE
  - Test with reduced pin-count



The Cost Trade-offs

Cheaper Tester
Cheaper Fixtures
Lower Dev. Costs

1 - 2% extra silicon
Full Scan



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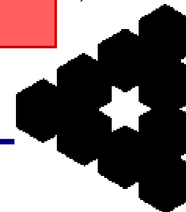
Final Manufacturing

- Higher Performance
- Lower Cost
- Improved Debug
- Re-use test with silicon cores

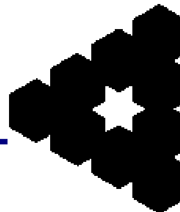


Why is Embedded Test ROI so compelling?

A $50+ Million Per Year potential saving

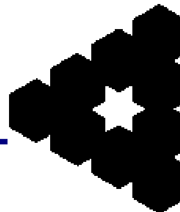
Typical Customer

Revenue	$4,000 M
Total Test Costs (5% of Rev.)	$200 M

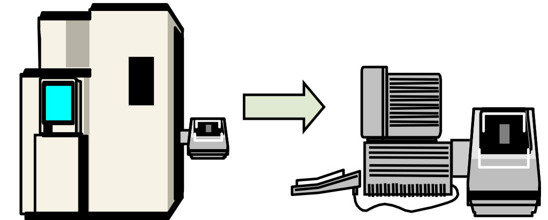


Tester Costs: High-End System

Reducing the Tester Cost



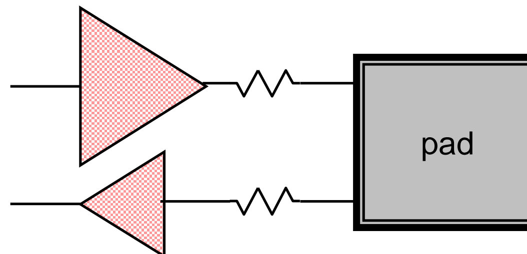
Embedded Test Reduces ATE complexity

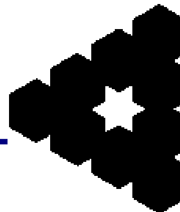


- No High Speed clock card
  - *Embedded Clock Generator*
- No complex tester timing sub-system
  - *only tck supplied*
- Minimum Memory required
  - *Use Looping/Repeat Constructs*
- No requirement for APG
  - *Memory Bist Controller generates test on chip*
- Reduced # of I/O's and/or pin electronics complexity
  - *Embedded I/O Test*

What about the I/O pins?

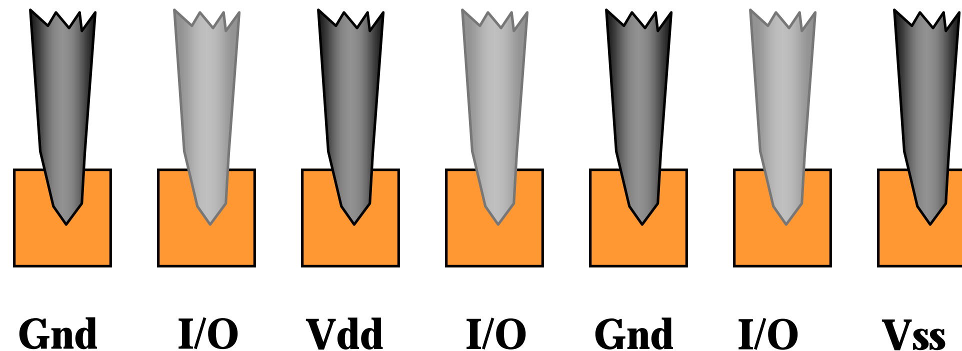
- Embedded I/O Tests
  - Probe Test
    - Low speed Functional wrap using Bscan
      (All pins must have I/O capability)
    - I/O Leakage (already proven in silicon)
  - Final Test
    - More complex I/O tests to follow





What About the Power?

- The I/O buffers can be off during embedded test.
  - Lower demand for dynamic power delivery
- Internal cores can be tested in parallel.
  - Optimize test time
  - Optimize power consumption.
- With design planning, pad pitch can be relaxed.
  - Alternate signal pins with power pins

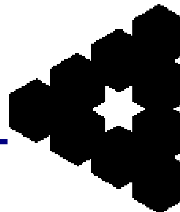


Epoxy probe card savings

Cost per probe card ($K)

Pads	All probed	JTAG+Pwr (20% of pads)
300	3.6	0.8
600	7.2	1.6
900	10.8	2.2
1200	14.4	3
1500	18	3.7

- Probe Vdd/Vss & JTAG
  - Power pins are 20-60% of total
- Fewer Probe Card headaches



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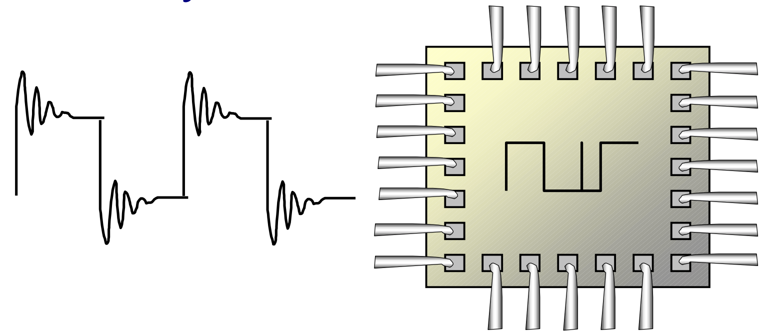
Test Engineering Impact

- Hardware Impact at Sort
  - Reduced probe count (only 4 TAP, clocks, V_{DD}/GND)
  - Can go to higher levels of parallel test
  - Focus shifts to clean power delivery



- Software Impact
  - Simpler test program
  - Faster test development
  - Faster load time (very few vectors)
  - Debug tools work in the designer's language

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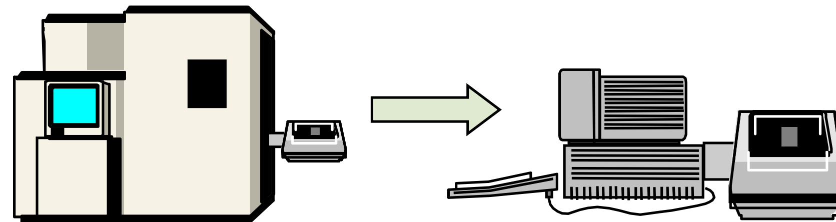
Embedded Test Summary

- Embedded Test Enables:
  - Reduced Tester Complexity / lower cost ATE
  - Reduced Pincount at Probe / lower fixture cost
  - Reduced Pad Pitch Requirements
  - Higher levels of parallel test / shorter test times
  - At-Speed test without At-Speed ATE
  - Leverage into burn-in, package test, board & system test



- Challenges:
  - Verify ROI pays for increased silicon (e.g. $50M vs. 1% ?)
  - I/O test strategy (solutions available)

Conclusions

- “If we keep doing the same things, we’ll keep getting the same results.”
  - Test Costs will continue to rise unless we change the approach.
- Moving the test “burden” to the silicon:
  - Off-loads the tester
  - Minimizes the ATE-DUT (freq. x pins) bandwidth demand
  - Solves the Roadmap challenges facing ATE suppliers
- The BIST silicon overhead is becoming insignificant as SOC designs scale-up
  - 1-2% more Silicon is cheaper than Capital + Tooling costs

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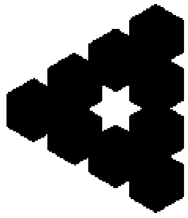

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