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Multi-Square Probe Card

(for Multi-DUT Testing of Peripheral Pad Layout Devices)

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Agenda

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1. Background of Multi-Square Development
2. Market Demand for Multi-Die Testing
3. Multi-Square Overview
4. Structure
5. Probe Needle Specification Review
6. Results of Reliability Test
7. Summary

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Background

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- Parallel test at wafer probe lowers test costs through reduced average test time per die.
- This technique is used extensively for memory test due to long test times.
- DRAM die pad patterns (i.e. LOC) and lead counts allow for highly parallel epoxy-cantilever probe cards.
- Logic, mixed-signal, and SOC device pad patterns (peripheral) and lead counts present significant challenges for efficient multi-die probing.
- The number of wafer touchdowns and ATE throughput is impacted by the die pattern of multi-DUT probe cards.
- MJC has developed Multi-Square to provide high efficiency die probe patterns for parallel test of peripheral pad ICs.

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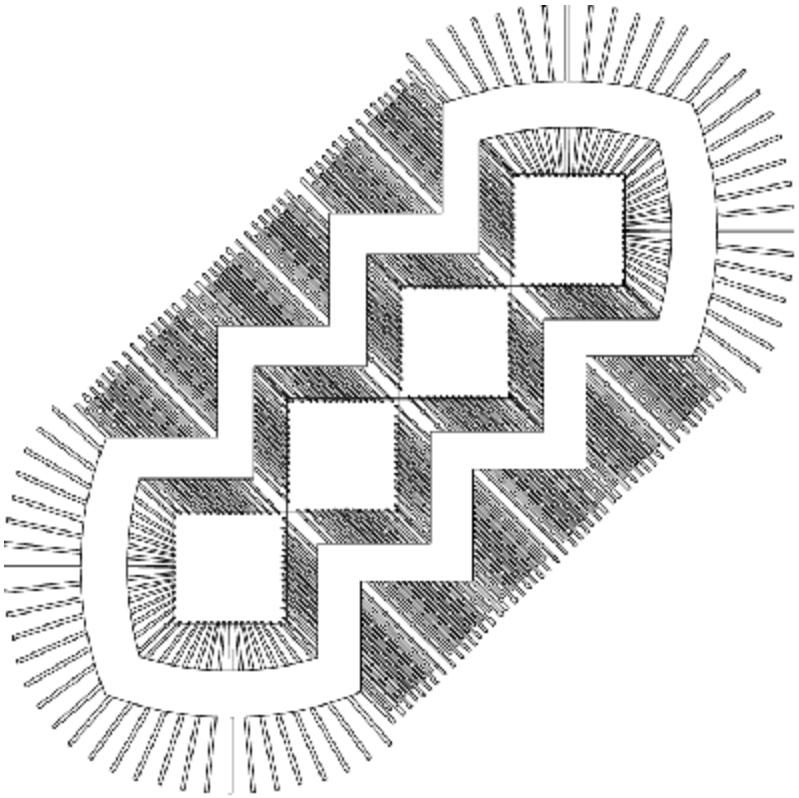

Typical 4 DUT probe card design

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Multi-Die Test

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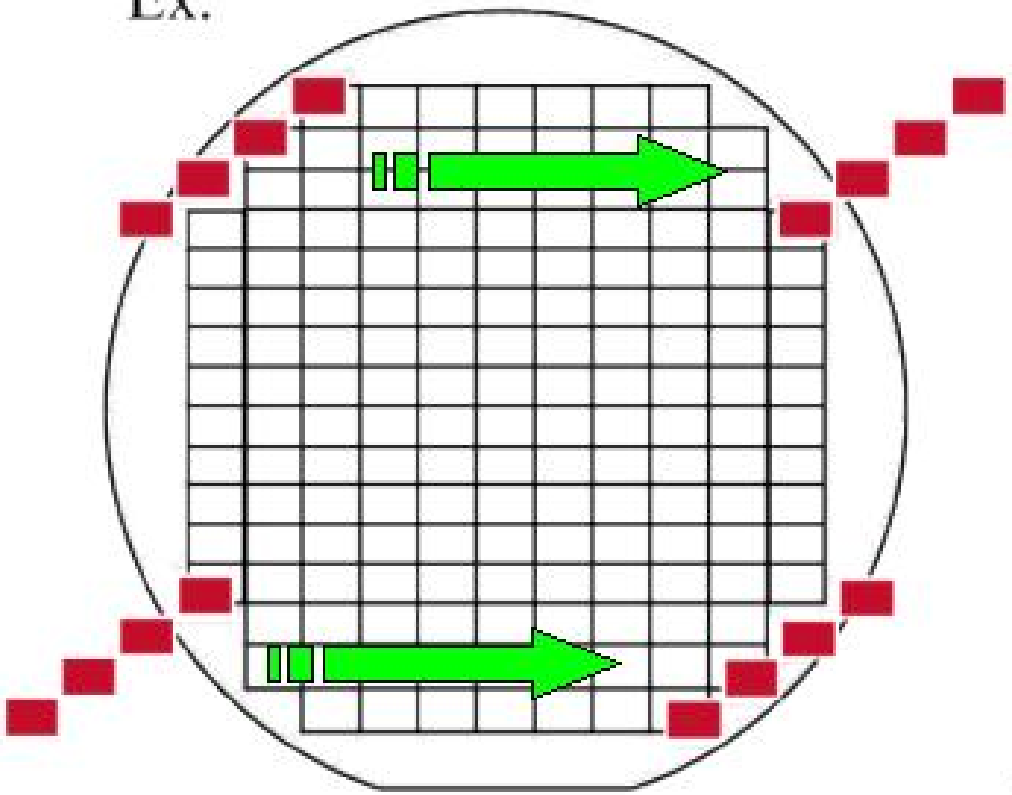
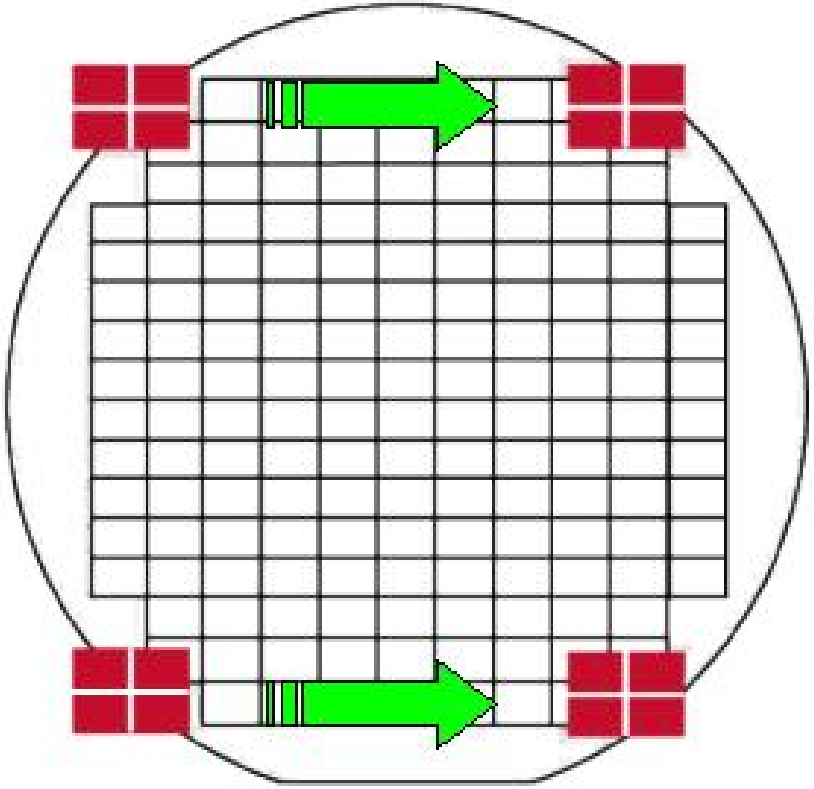
Diagonal 4 DUT

Ex.



52 touchdowns

Multi-Square 4 DUT



46 touchdowns

12% efficiency improvement with 2x2 DUT probe pattern

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Diagonal Probe Angle Creates a Finer Needle Pitch Requirement

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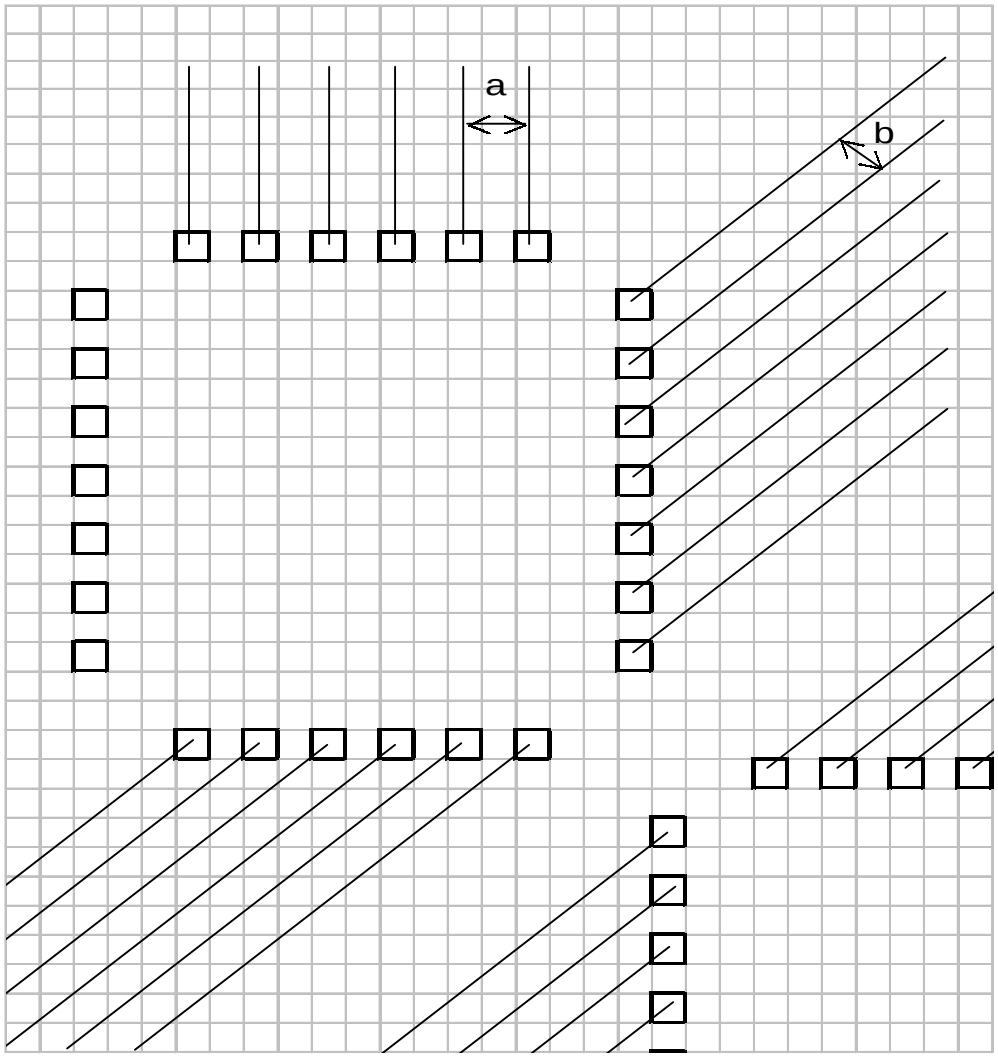

For a 45^{o} approach angle:

$b = a/\sqrt{2}$

Example: die pitch (a) of 60 µm,
b = 42 µm.

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Multi-Square 2x2

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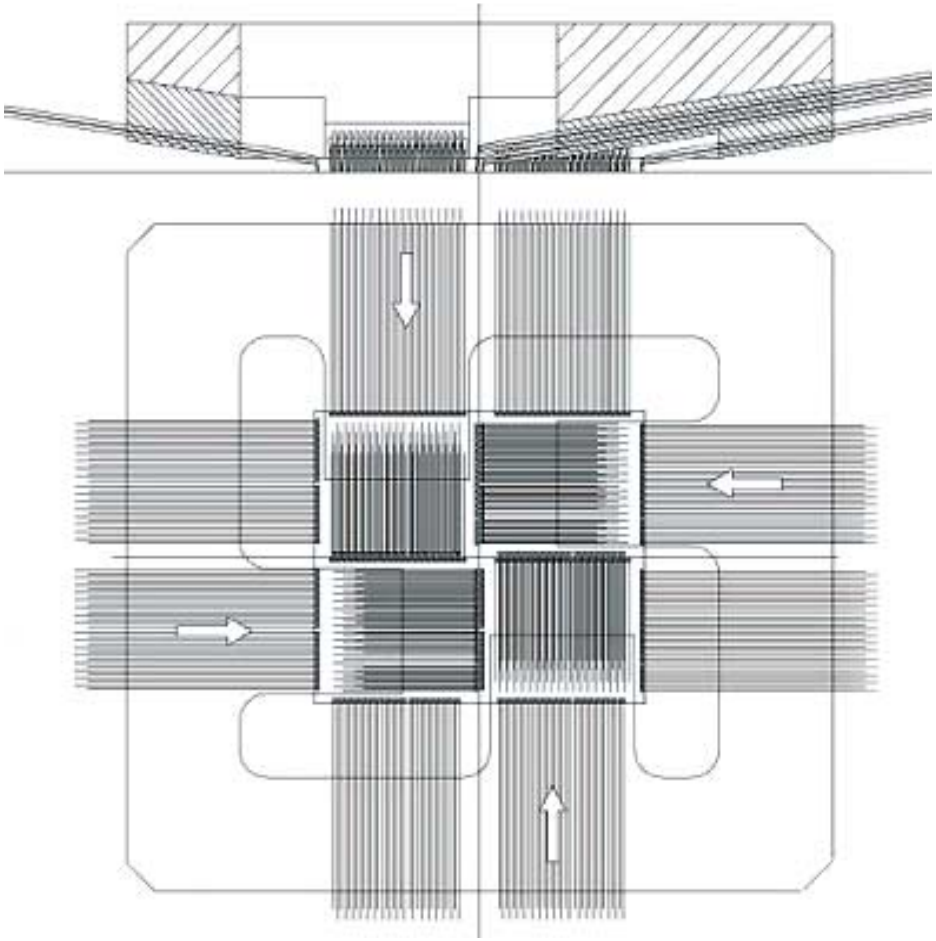
2x2 parallel DUT probing pattern



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Multi-Square 2x2

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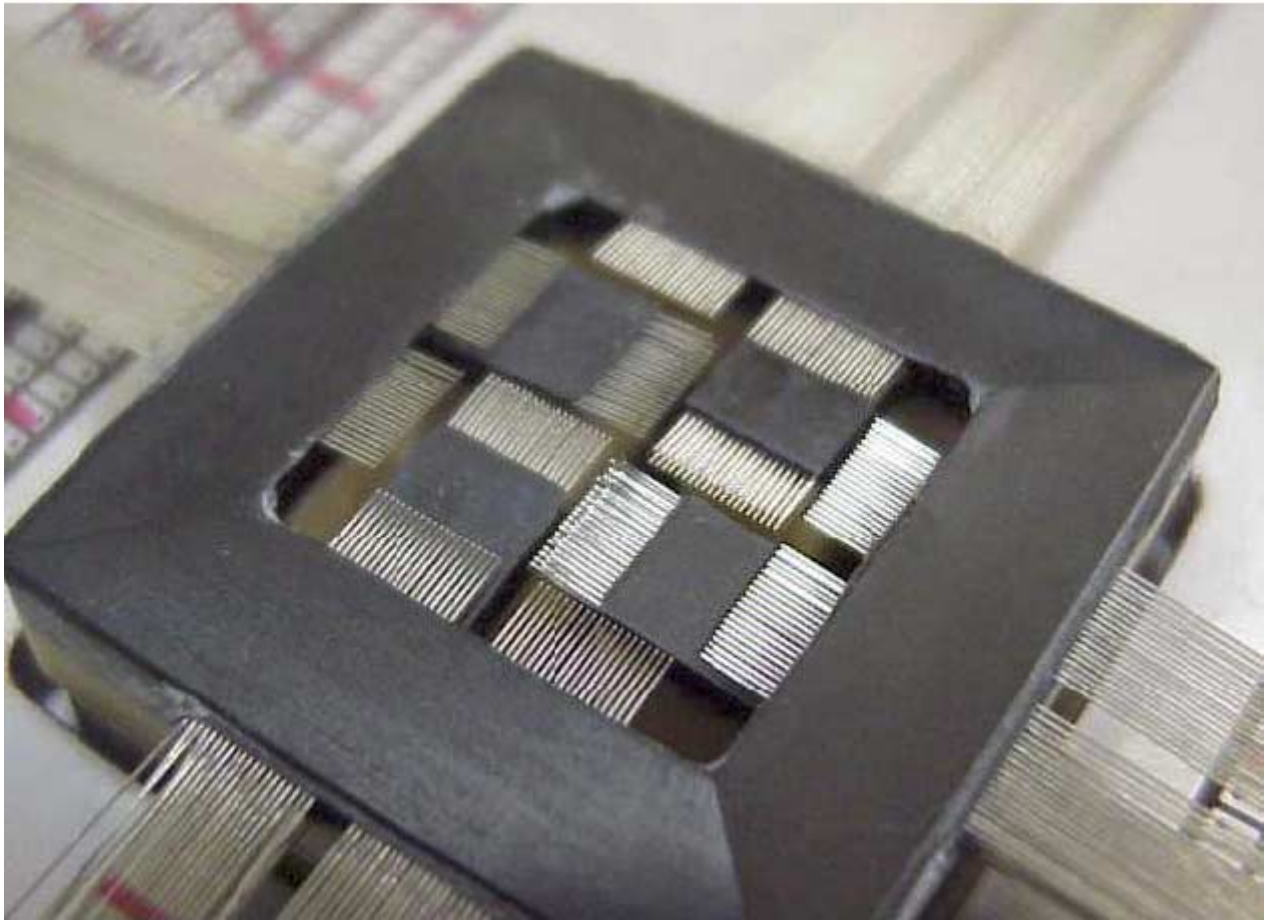

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Multi-Square 2x2

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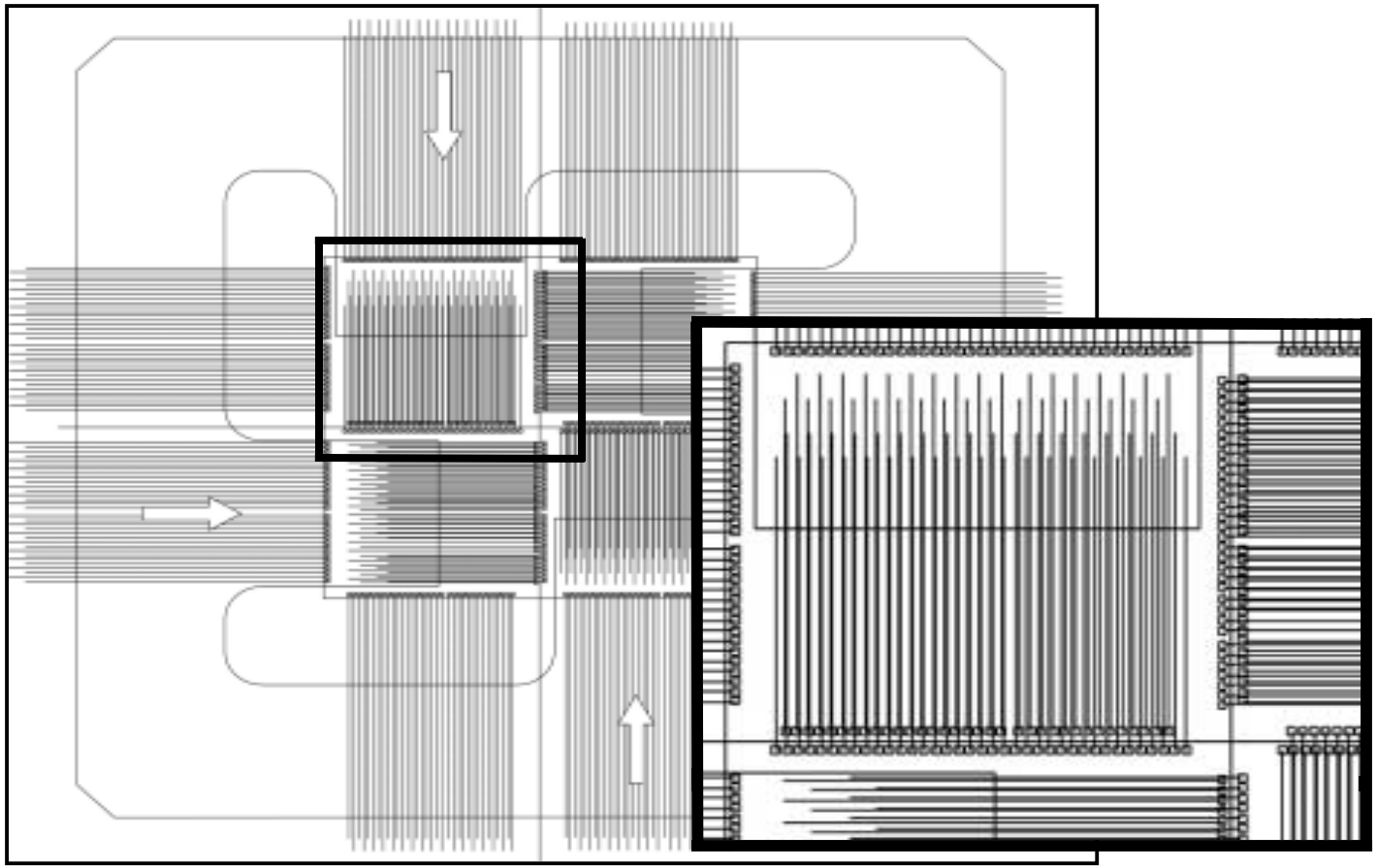

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Multi-Square In-line (1x2, 4, or 8)

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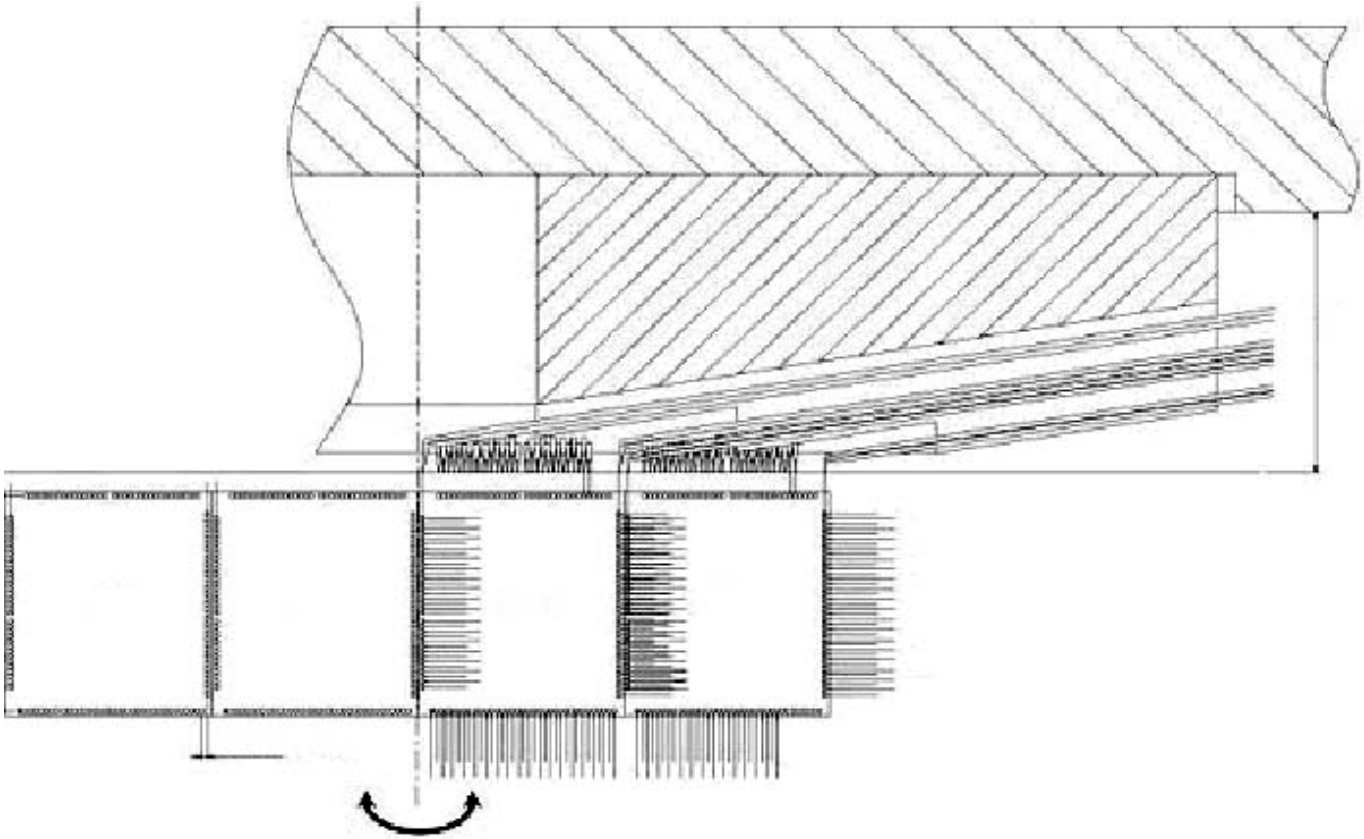

Symmetric

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Multi-Square 1x4

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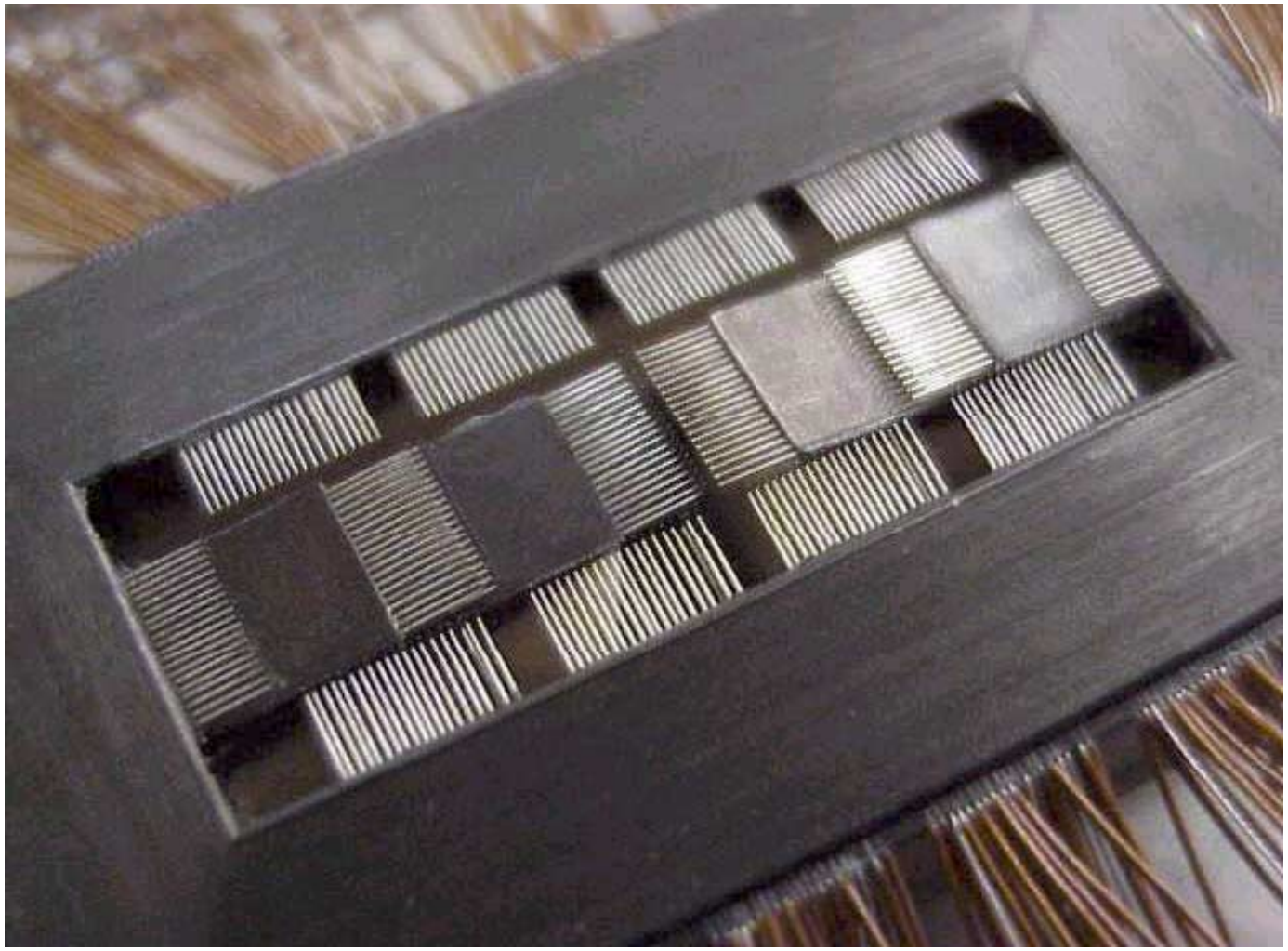

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Multi-Square 1x8

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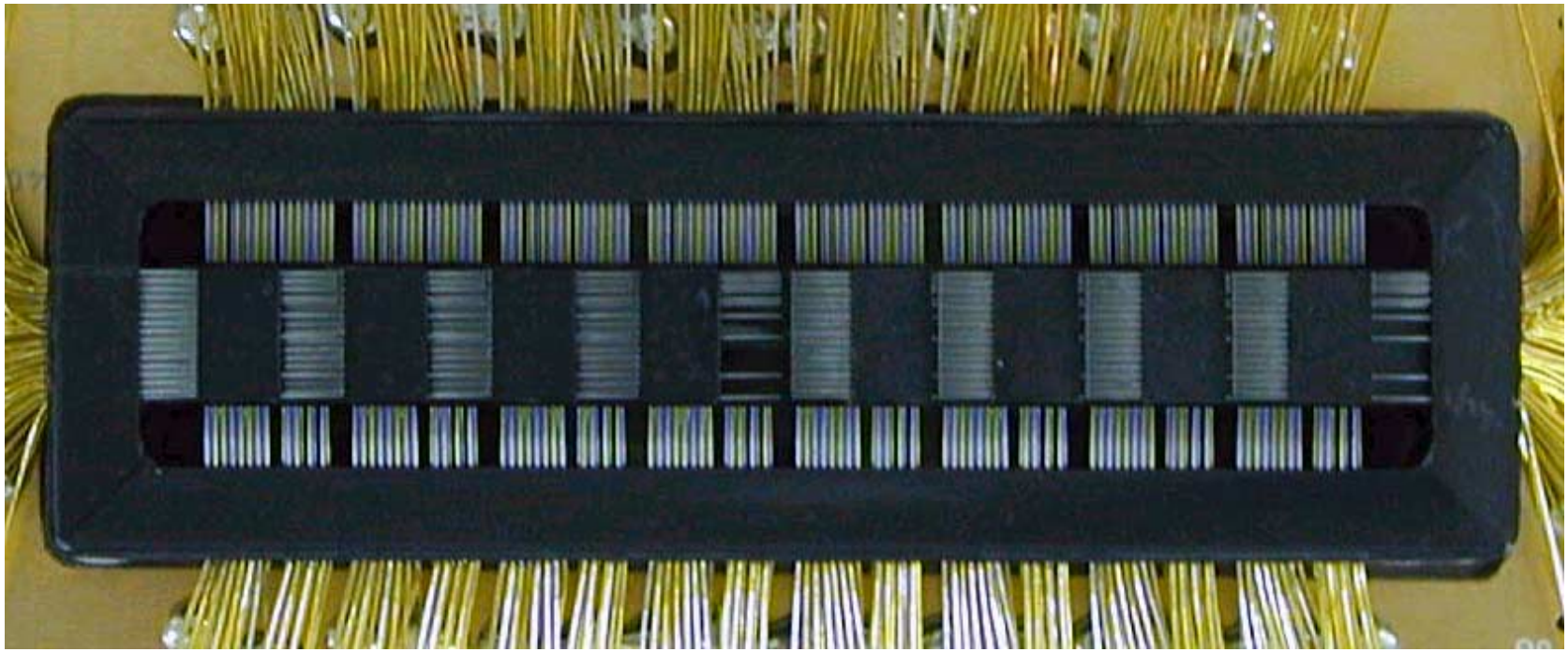

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Structure

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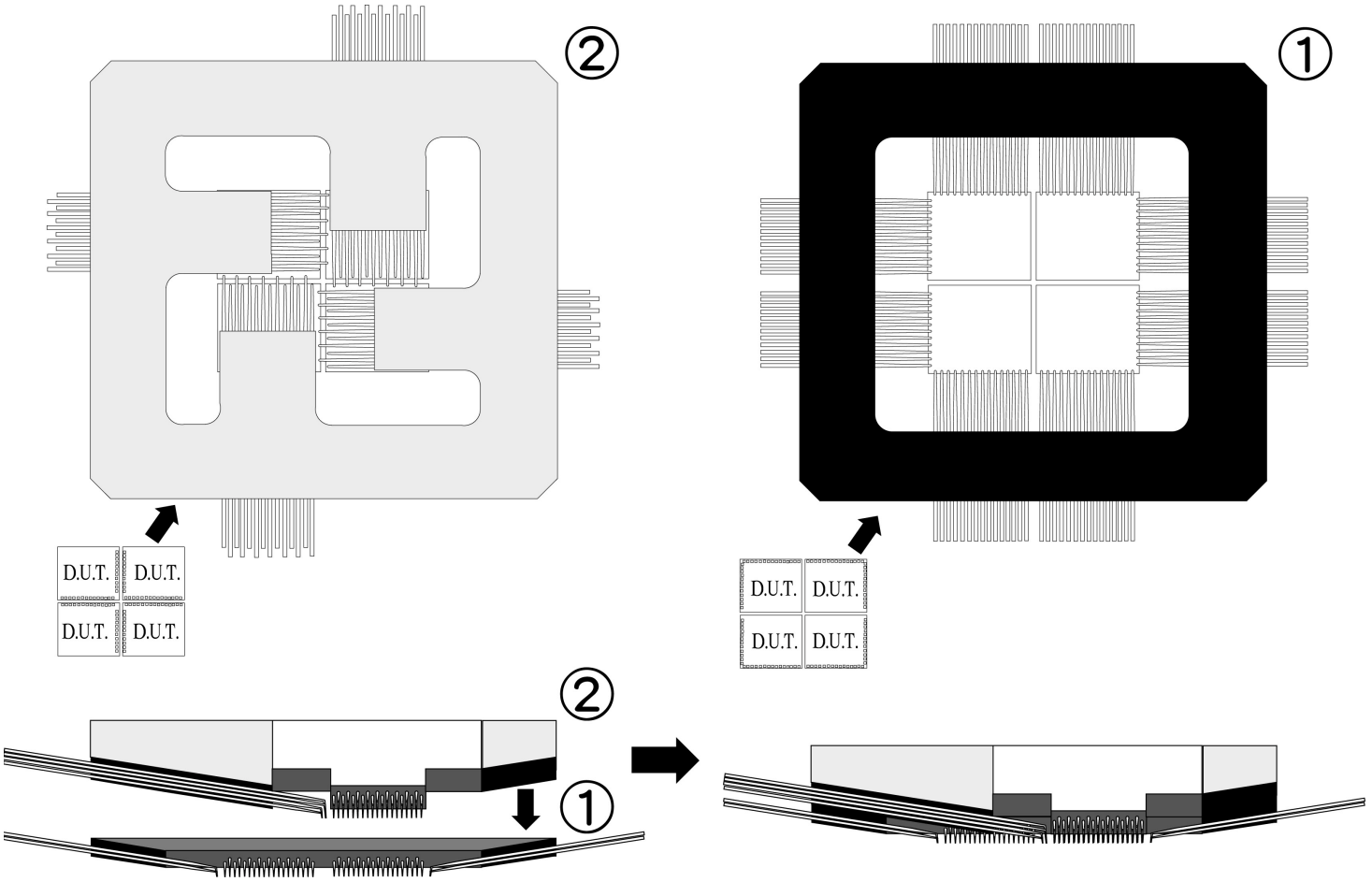

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1x4 Stiffener

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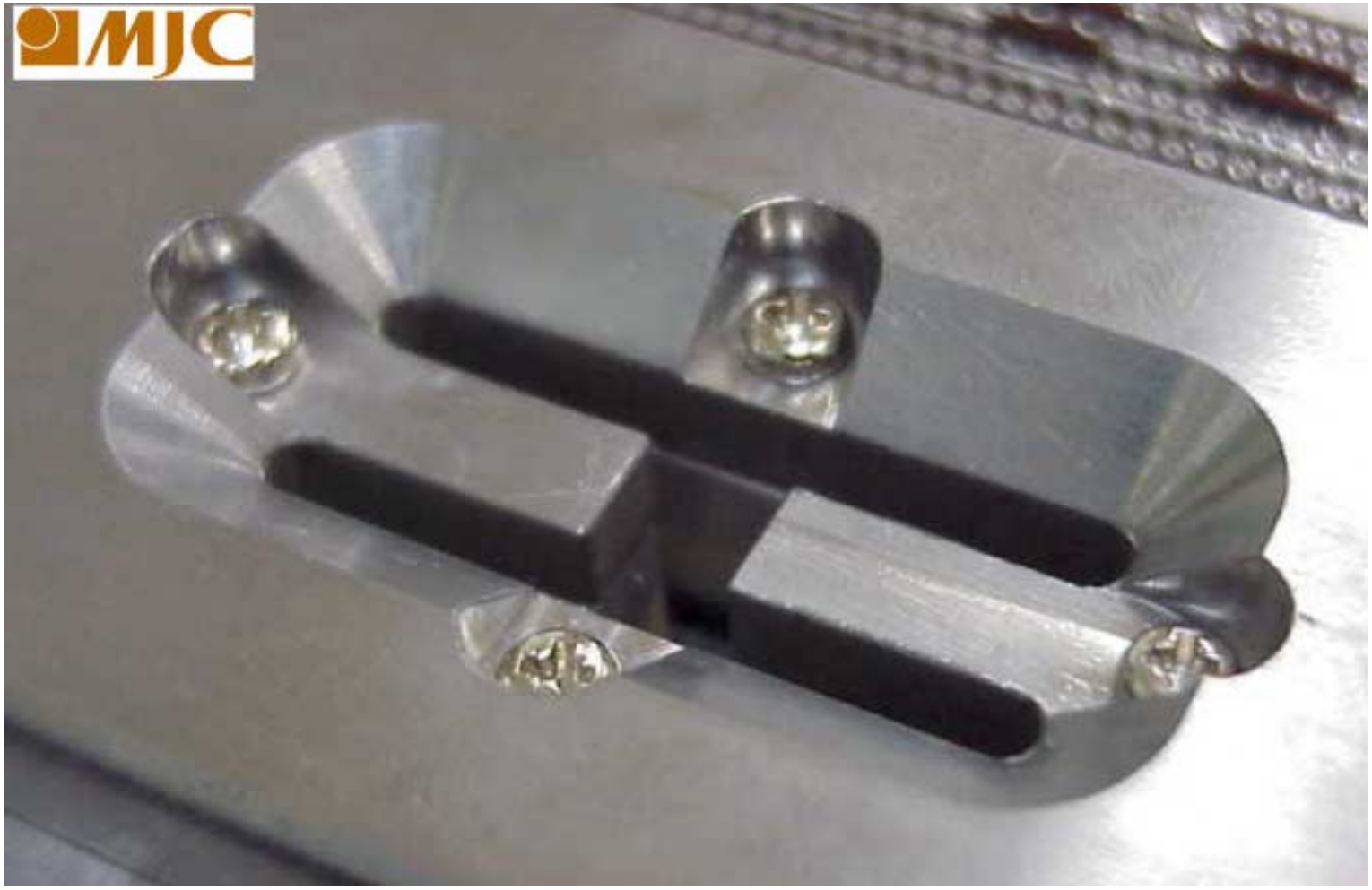

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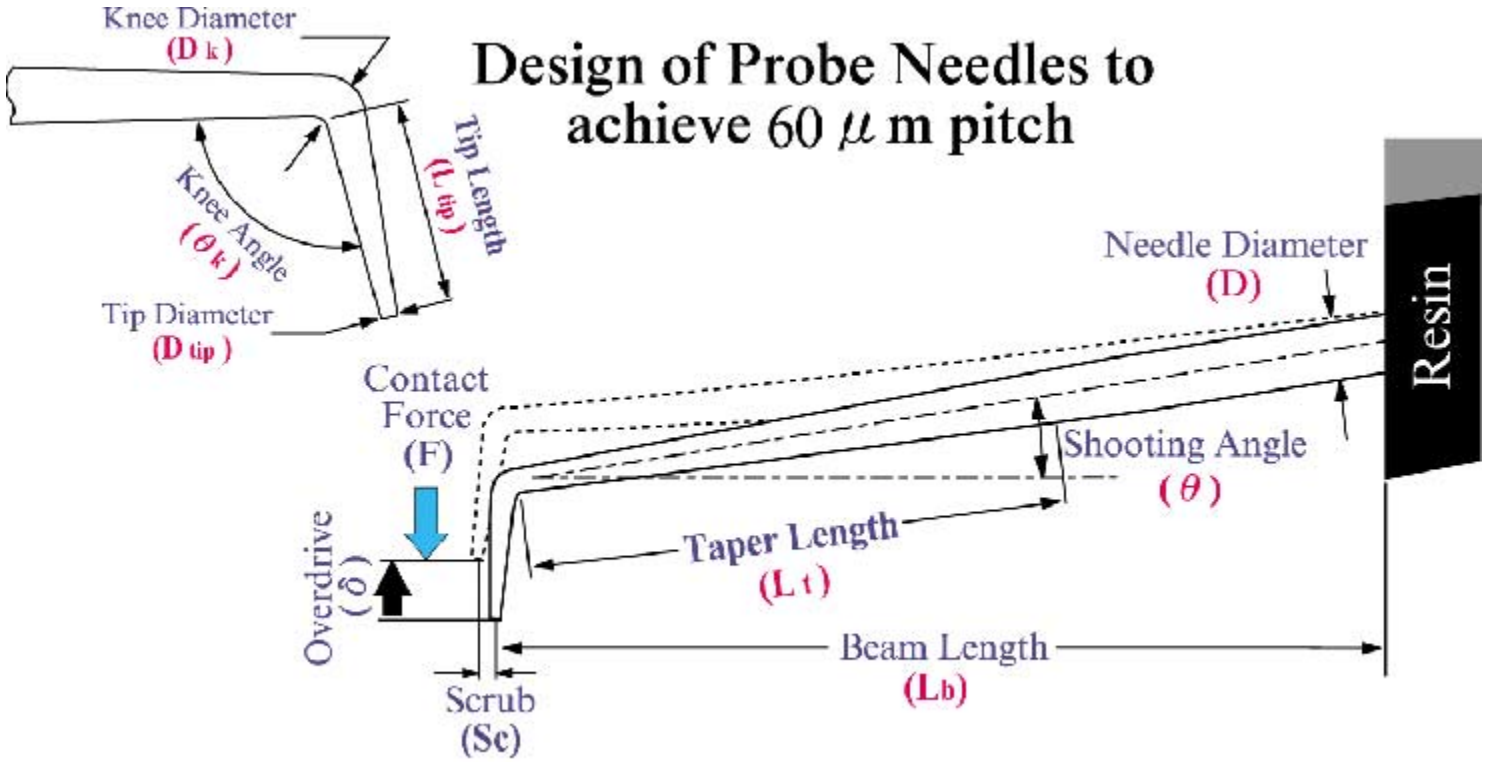
Probe Specification Comparison



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Probe Specification Comparison

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Multi-Square vs Diagonal Epoxy-Ring
60μm pitch 585pins SoC

	Multi-Square					
	D	Theta	Ltip	Lb	Dk	Lt
Layer-1	130um	4	300um	2200um	45um	1650um
Layer-2	130um	4.5	450um	2200um	55um	1540um
Layer-3	130um	5	600um	2200um	60um	1420um
Layer-4						
	Diagonal Epoxy-Ring					
Layer-1	100um	5	170um	2000um	30um	1200um
Layer-2	100um	7	230um	2000um	33um	1200um
Layer-3	100um	10	290um	2000um	37um	1200um
Layer-4	100um	12	350um	2000um	40um	1200um

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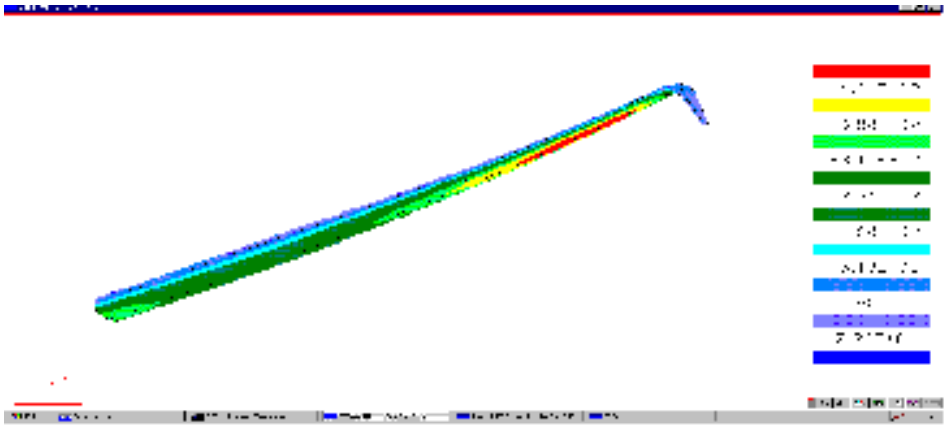
FEM analysis



	OD	Force	Scrub
Layer-1	50um	3.85g	9um
Layer-2	50um	4.71g	11um
Layer-3	50um	5.26g	14um

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Reliability Test

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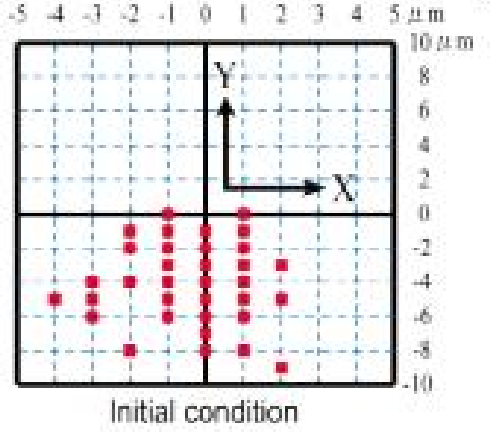
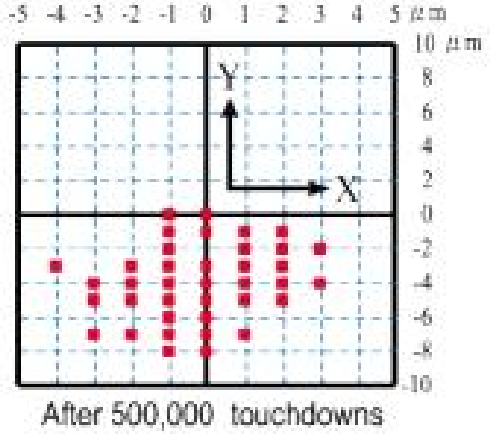
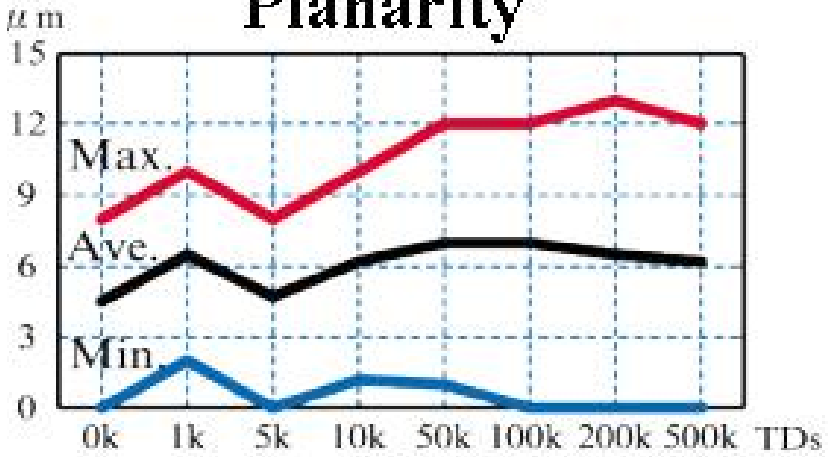
Positional Accuracy

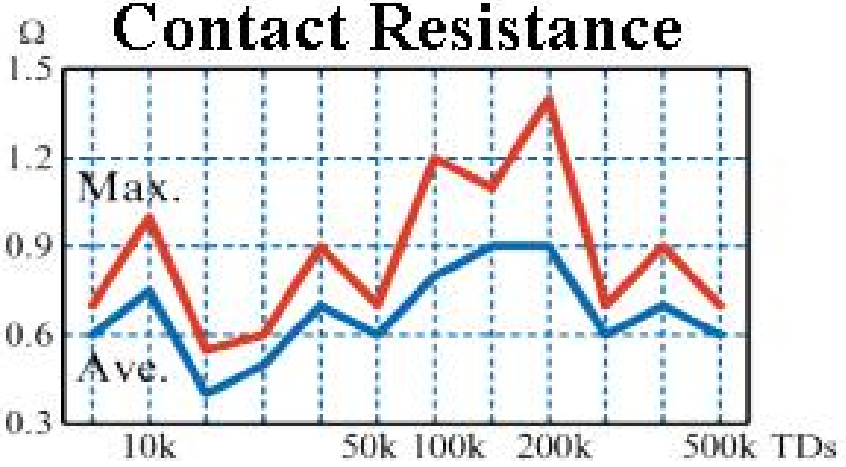




Planarity



Contact Resistance



Reliability is equivalent to conventional epoxy-cantilever

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Improved Scrub Margin

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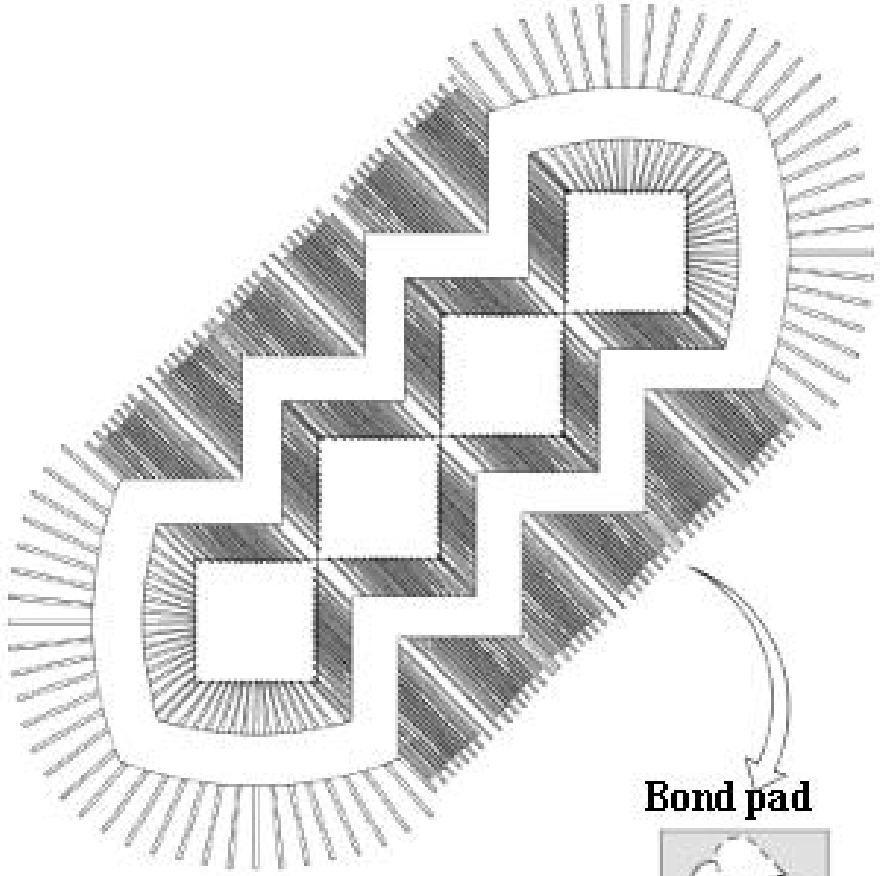
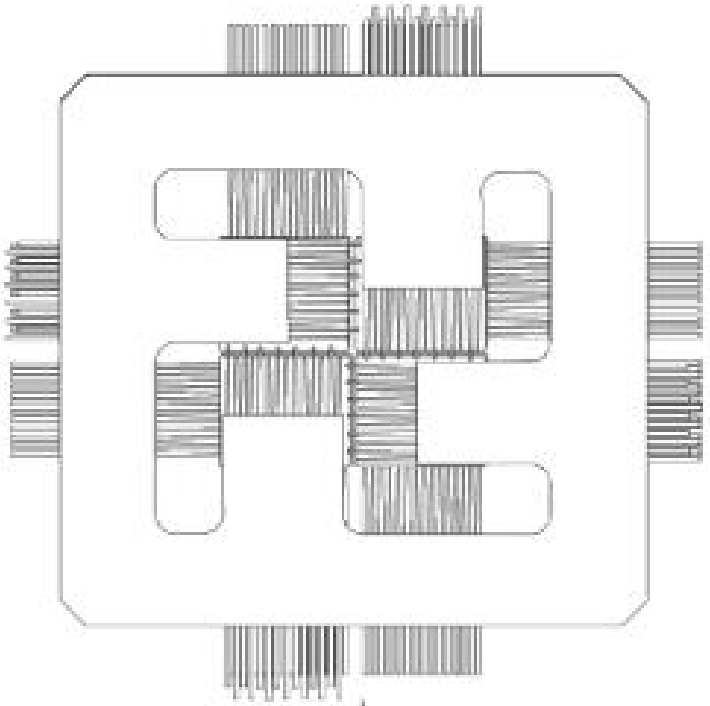
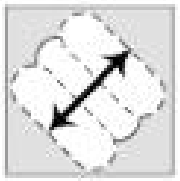
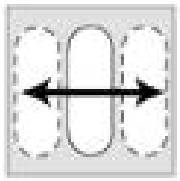
Conventional 4DUT



Multi-Square







Scrub margin

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Summary

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- ✓ **Multi-Square probe technology enables 1x2, 4, 8 and 2x2 DUT probing patterns for ICs with pads on all four sides.**
- ✓ **The efficient probe patterns supported reduce the number of touchdowns required per wafer, increasing ATE throughput.**
- ✓ **Perpendicular needle approach angles allow fine pitch probing and optimized scrub margin.**
- ✓ **The technology is compatible with conventional epoxy-cantilever production systems and therefore competitive for cost and schedule.**
- ✓ **The technology is based on proven cantilever designs and provides the same reliability and performance as conventional epoxy-cantilever technology.**

ECT