RF Signal Integrity Characterisation of Probe Cards

K. Helmreich, A. Lechner

Advantest Test Engineering Solutions GmbH

June 2001

ADVANTEST

Outline

1 Motivation: At-Speed Probing
2 How to Quantify 'Speed' ?
3 Measurement Items and Methods
4 Results
5 Summary

ADVANTEST

Motivation: At-Speed Probing

In the past ...

probe technologies limited wafer level test speed

Now ...

new probe technologies promise at-speed capabilities

Question:

How fast can we go ?

ADVANTEST

How to Quantify 'Speed' ?

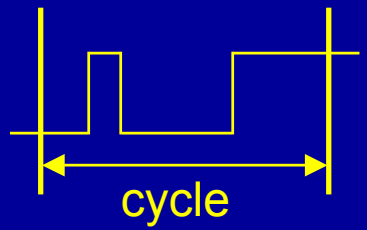
Common Misunderstandings

- intermix **test vector rate**, **test data rate** and **bandwidth**, all expressed in units of **MHz**
- use terms as **transition time**, **rise time**, **fall time** without clear threshold definition (e.g. 20% to 80%)
- don't differentiate **signal transition time** and **equivalent** or **intrinsic transition time** of **interconnects**
- don't distinguish between **probe card** and **probe assembly**, i.e. PC and PC interface to tester

ADVANTEST

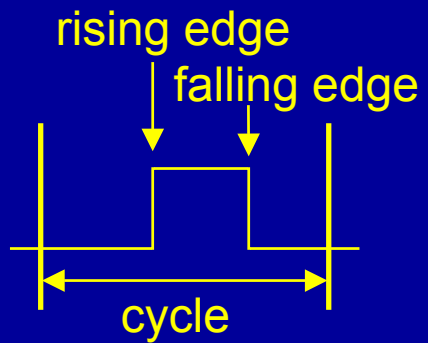
The 'Speed' Confusion - What is a MHz ?

1. **Test Vector Rate R_v**



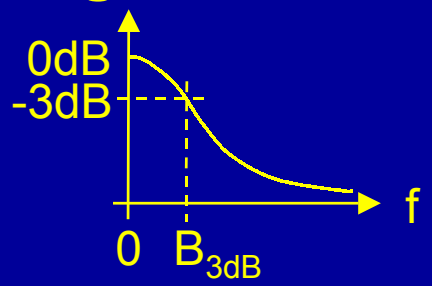
number of test cycles per second,
e.g. 400 Mcps,
usually referred to as 400 MHz

2. **Test Data Rate R_D**



number of bits transferred per second:
a bit of data is transferred with
- rising edge (SDR), e.g. 400 Mbit/s
- both edges (DDR), e.g. 800 Mbit/s

3. **Signal Bandwidth $B_{3dB,signal}$**



3dB-width of the frequency band of sine components constituting the signal, for test signals from DC to e.g. 600 MHz

ADVANTEST

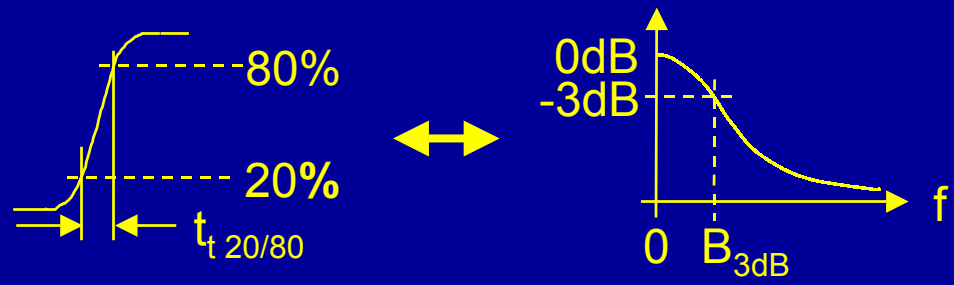
'Speed' Relationships: Signal and Intrinsic Transition Times

Assumptions:

1. Test signals show 'Gaussian' edges
   (i.e. time integral of Gaussian pulses)
2. PC assembly shows Gaussian filter characteristic: $a(dB) \sim -f^2$

→ $B_{3dB,\mathbf{sig}} = 0.22 / t_{t\ 20/80,\mathbf{sig}}$

→ $t_{t\ 20/80,\mathbf{int}} = 0.22 / B_{3dB,\mathbf{int}}$



signal passing PC assembly:

$t^2_{t\ sig,\ out} = t^2_{t\ sig,\ in} + t^2_{t,\ int}$

tolerated transition time prolongation ≈ 5%:

$t_{t\ 20/80,int} < 0.32\ t_{t\ 20/80,sig,\ in}$

approximate maximum test vector rate:

$R_{V,\ max} \approx 1 / (5\ t_{t\ 20/80,sig})$

ADVANTEST

Model and Reality

Real Test Signals ...

may not show exactly Gaussian edges

Real PC Assemblies ...

may not show Gaussian filter characteristic

Fortunately ...

above equations are fairly accurate for a variety of edge shapes and monotonous low pass filter responses

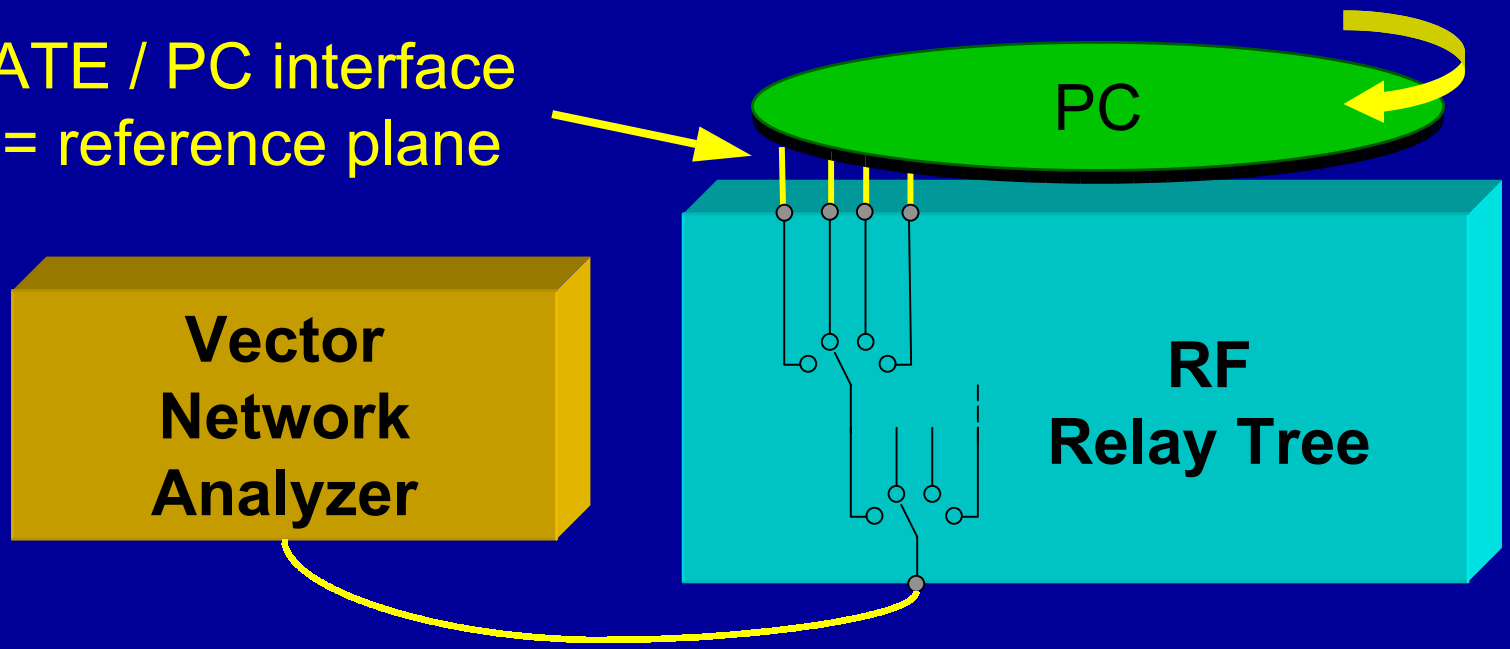
Requirements to At-Speed Probe Assemblies

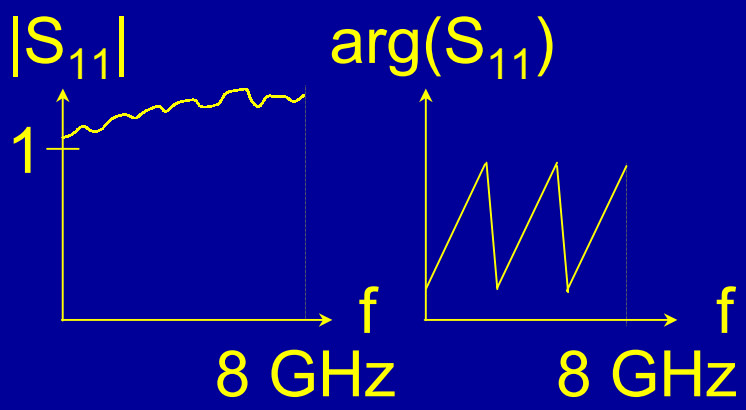
- **uniform propagation delay over channels**
- **sufficiently low intrinsic transition time on all channels**
- appropriate power / ground structures
- sufficiently low crosstalk between channels

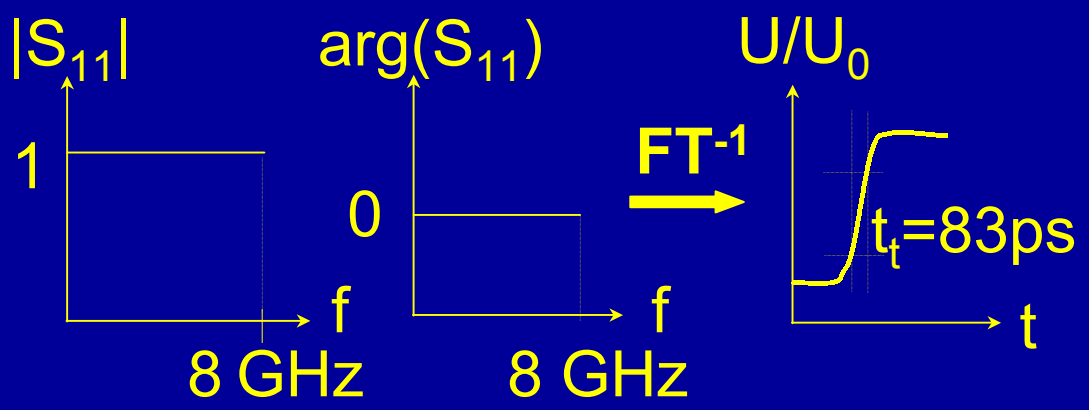
ADVANTEST

Measurement Method: Frequency Domain Reflectometry

ATE / PC interface
= reference plane







ADVANTEST

Test Fixture Characterisation System - TeFiCS®

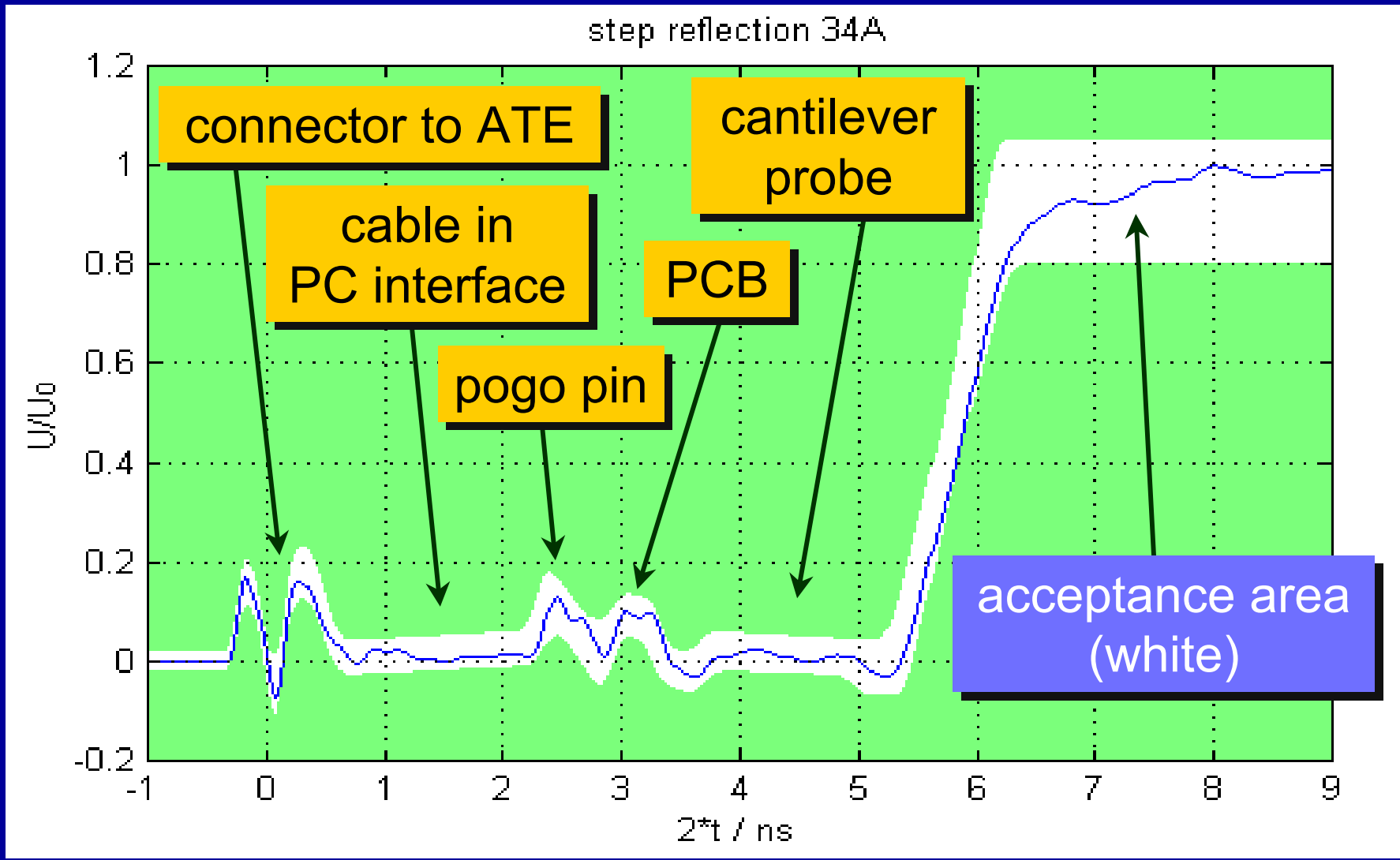
ADVANTEST

TeFiCS® Probe Card Test Unit

ADVANTEST

Results: PC Assembly

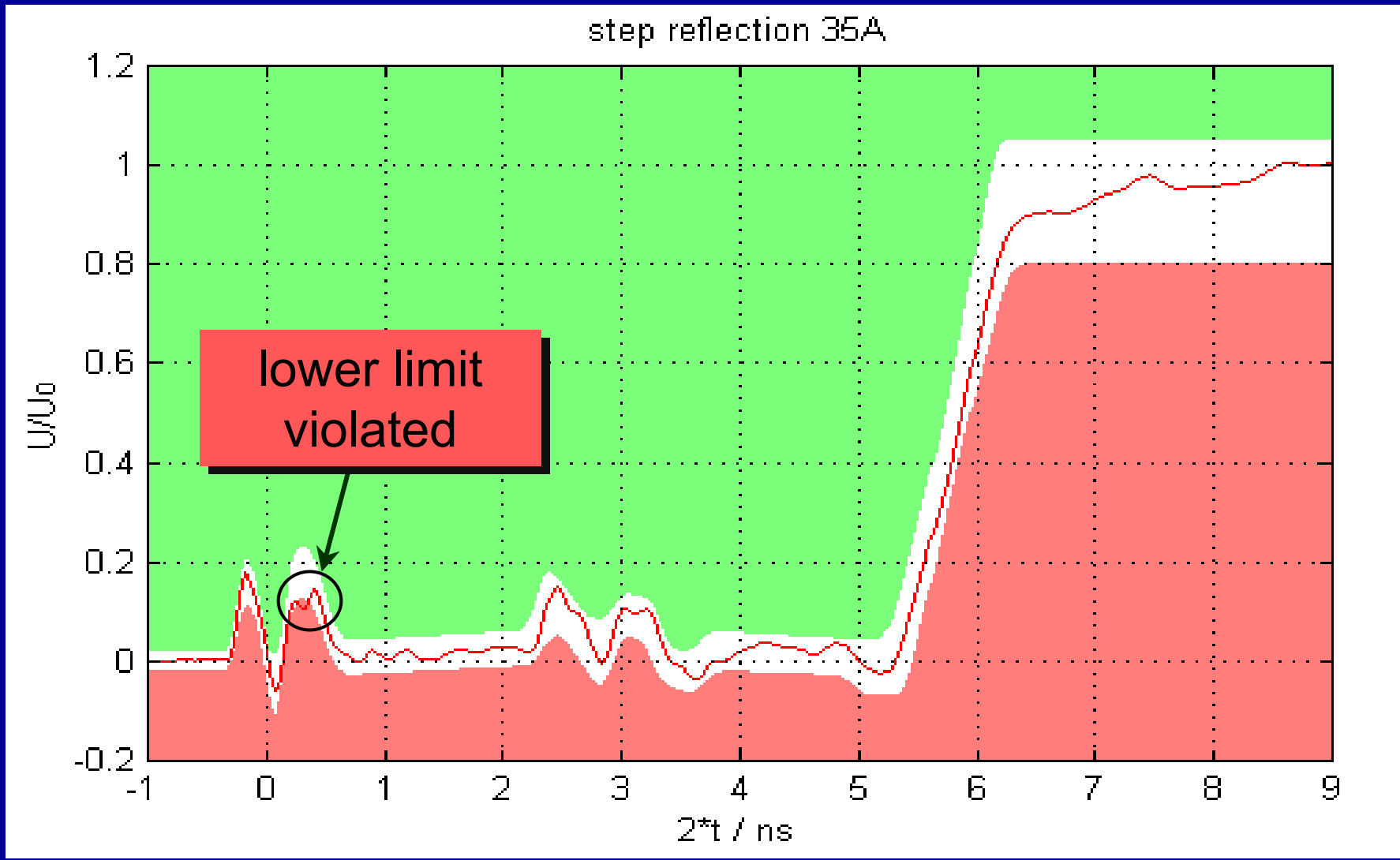
Step Response



ADVANTEST

Results: PC Assembly

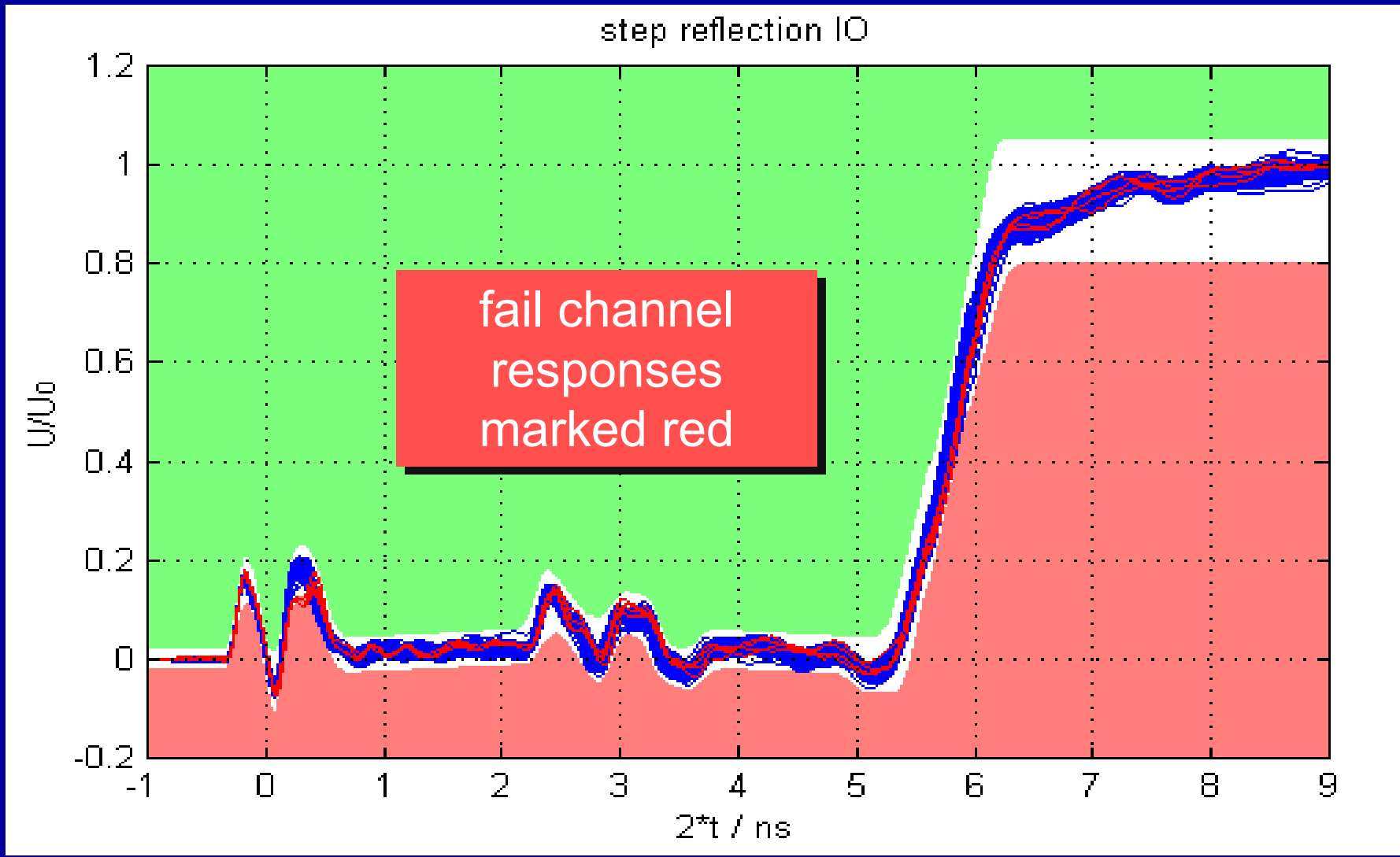
Pass / Fail Decision



ADVANTEST

Results: PC Assembly

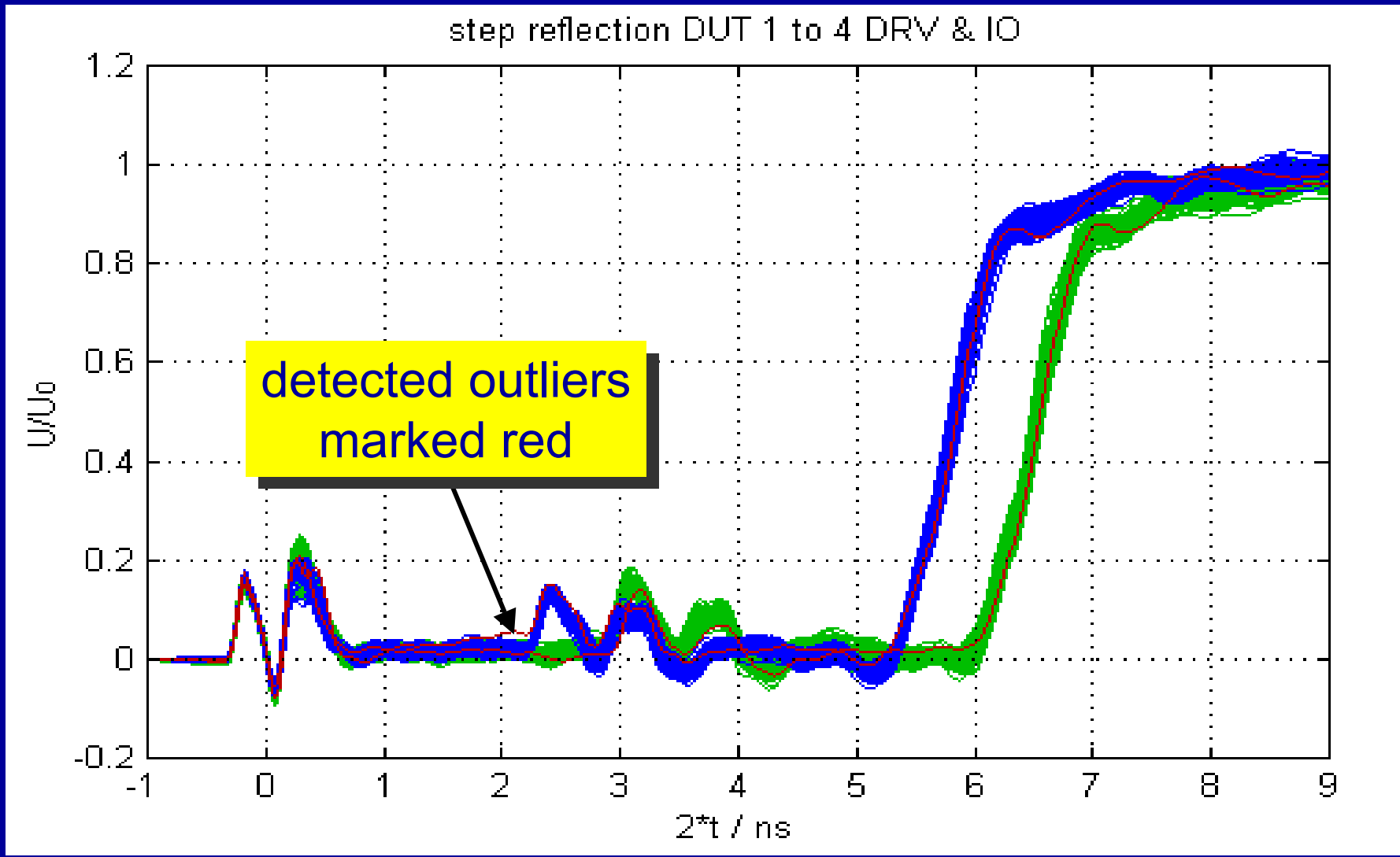
Analysing Step Responses



ADVANTEST

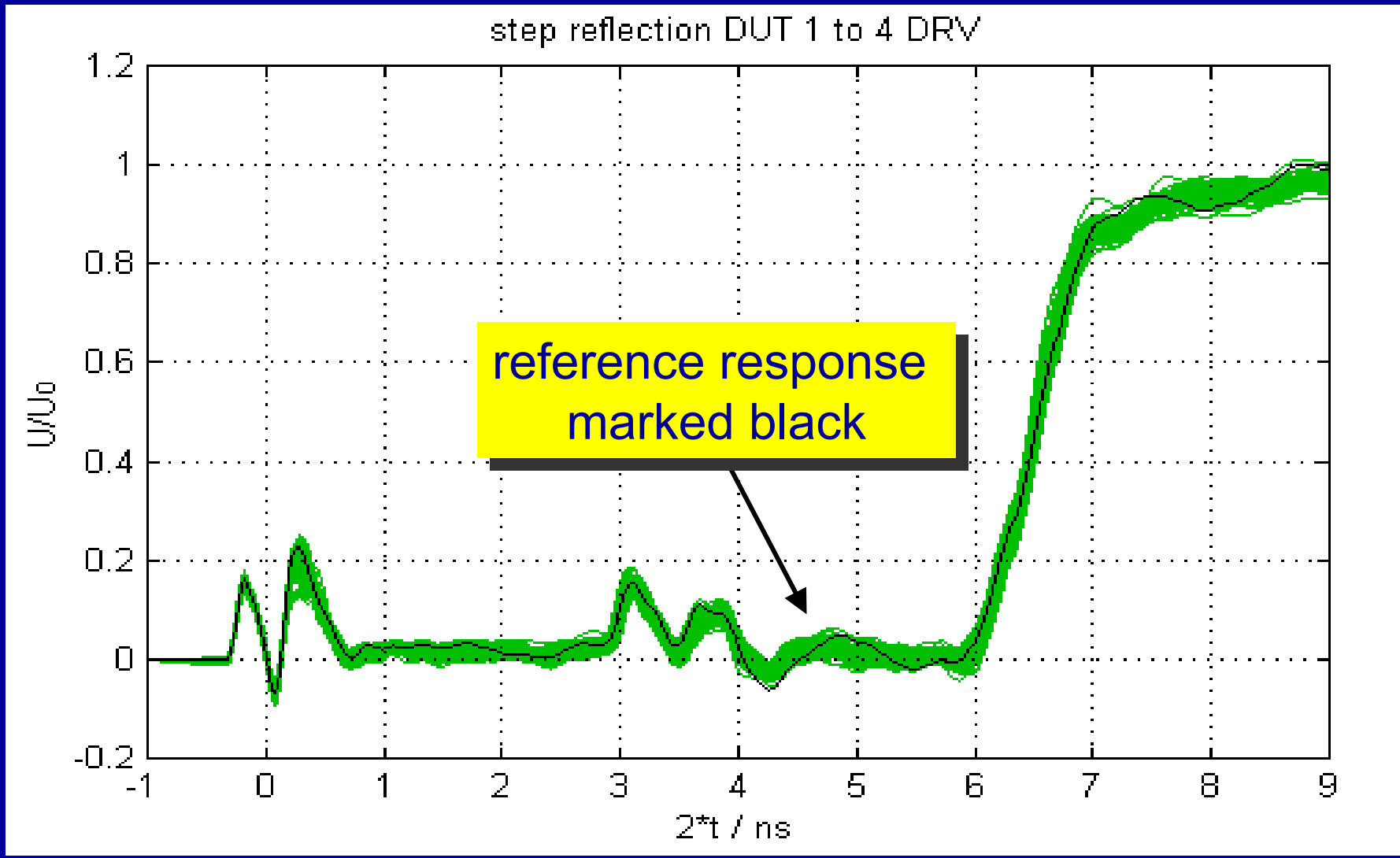
Results: PC Assembly

Comparing Channel Classes



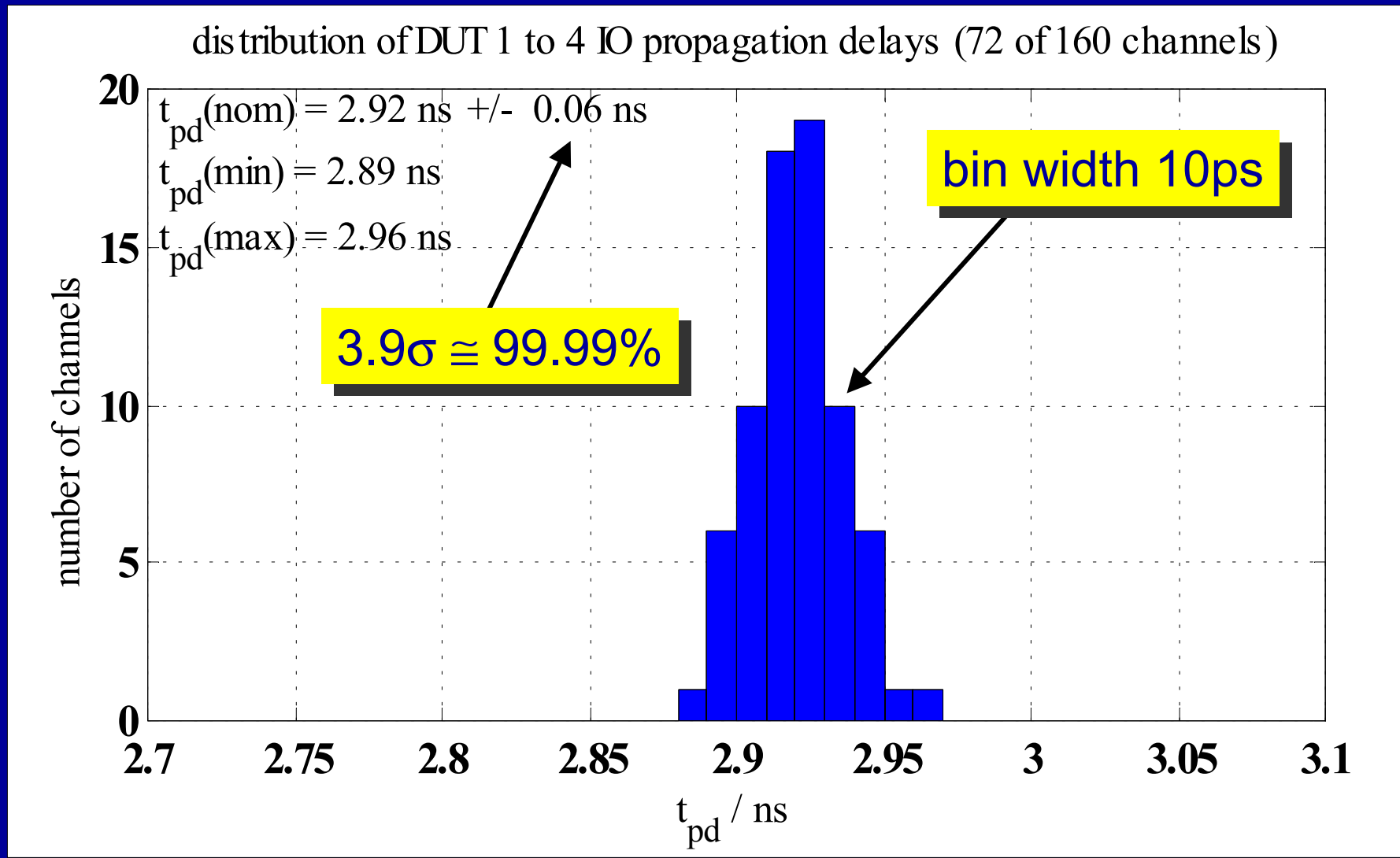
ADVANTEST

Results: PC Assembly Comparing to Reference Response



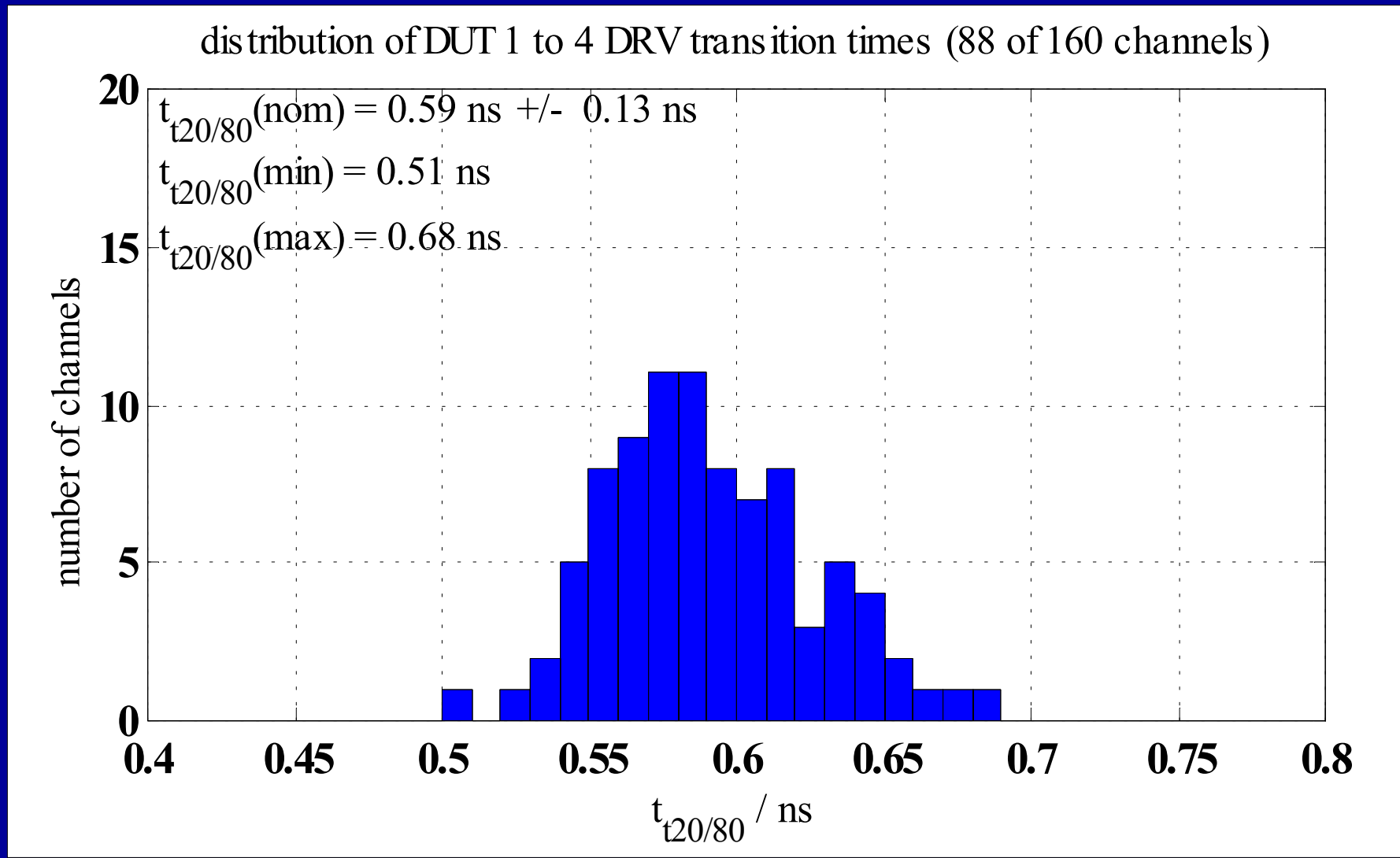
ADVANTEST

Results: PC Assembly — Propagation Delay Histogram



ADVANTEST

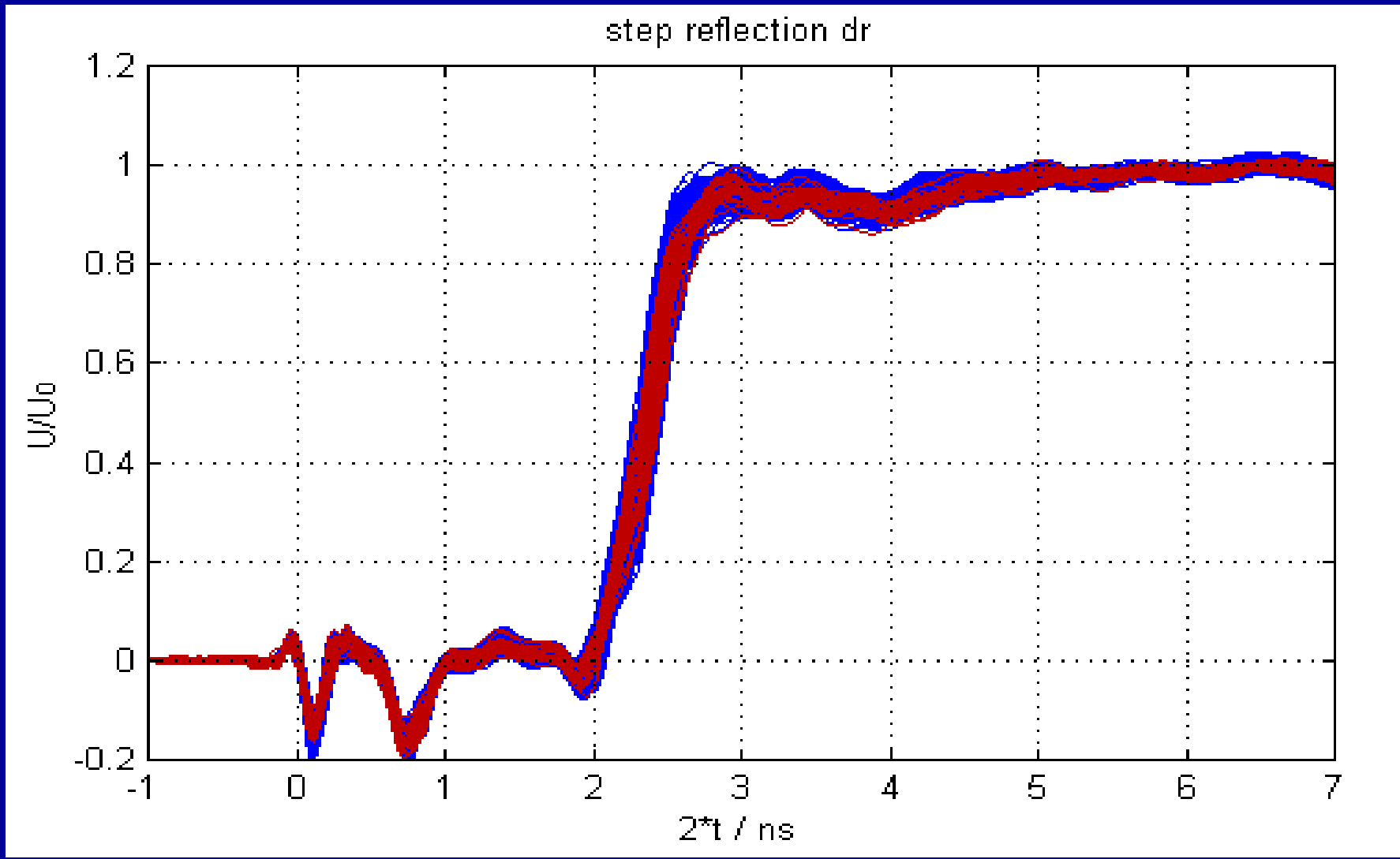
Results: PC Assembly Intrinsic Transition Time Histogram



ADVANTEST

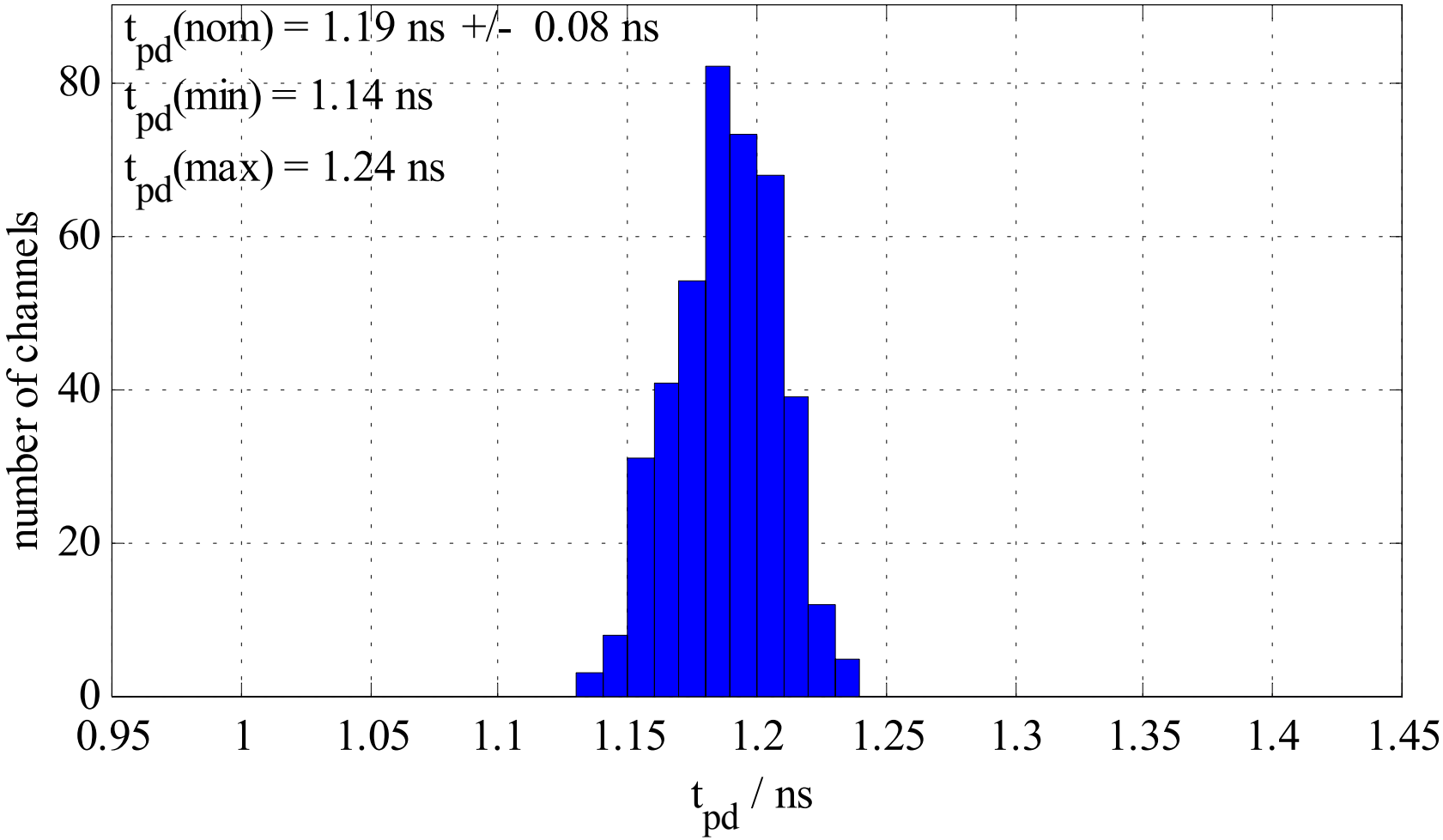
Results: Cantilever PC

Step Response



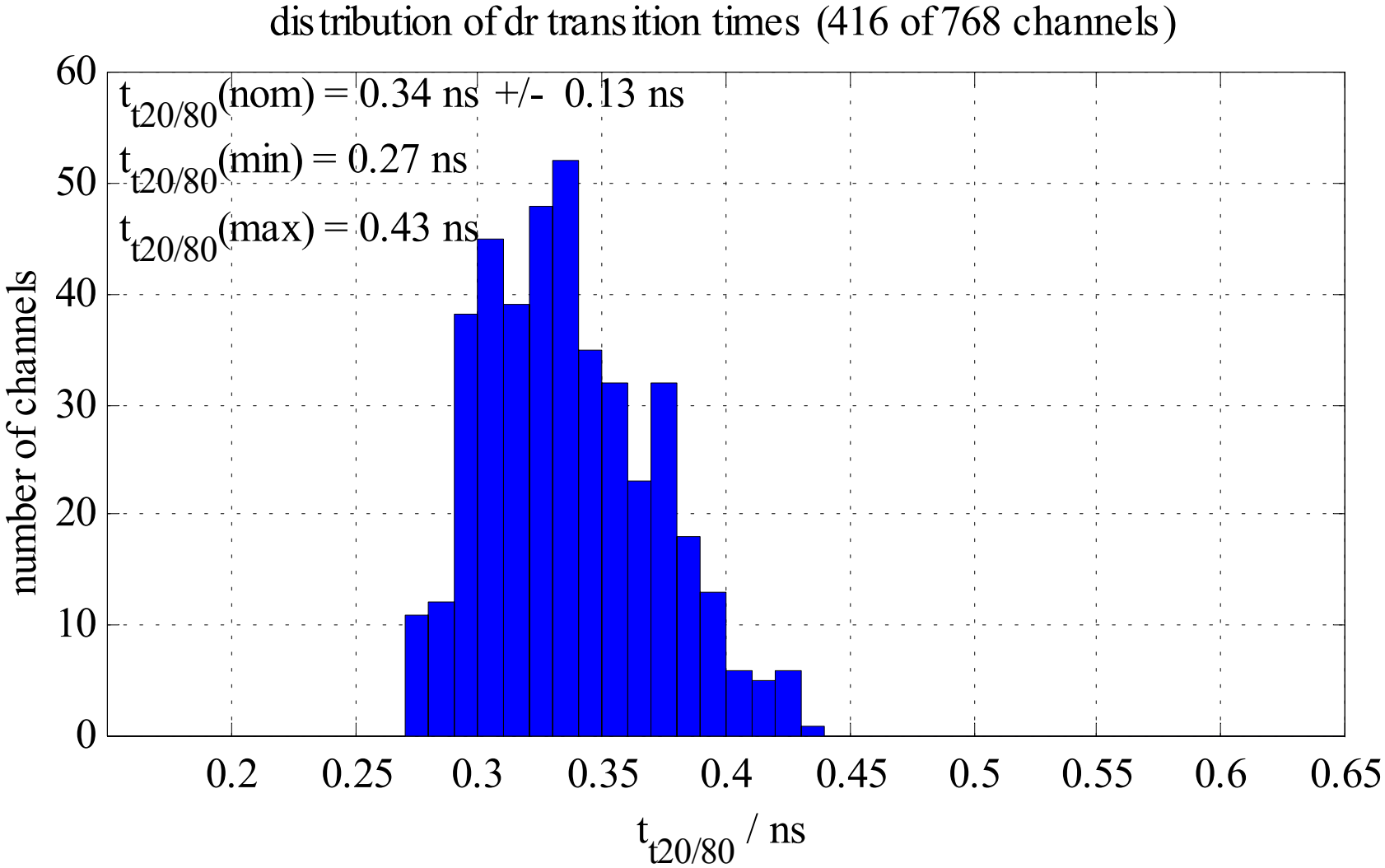
ADVANTEST

Results: Cantilever PC Propagation Delay Histogram



ADVANTEST

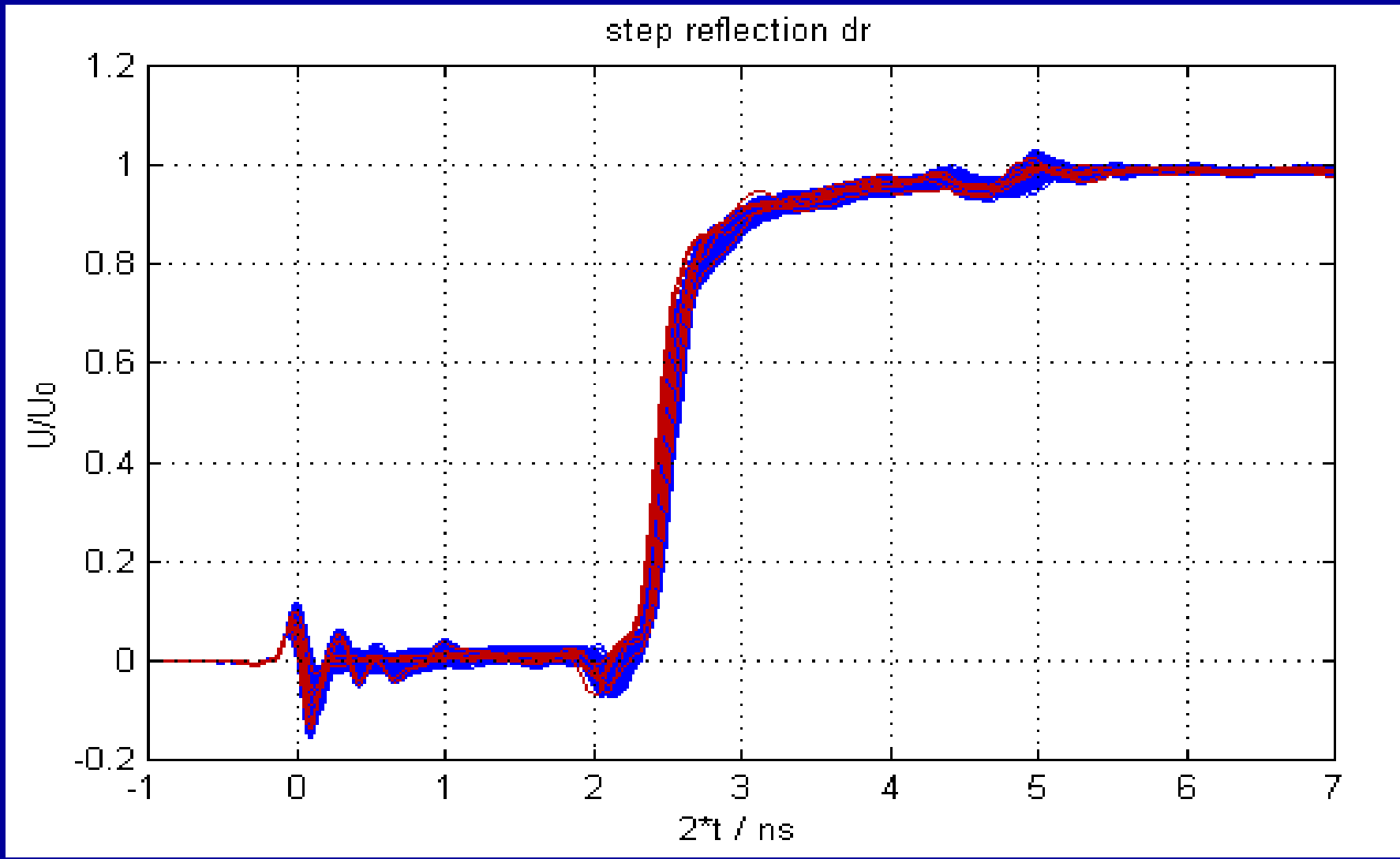
Results: Cantilever PC Intrinsic Transition Time Histogram



ADVANTEST

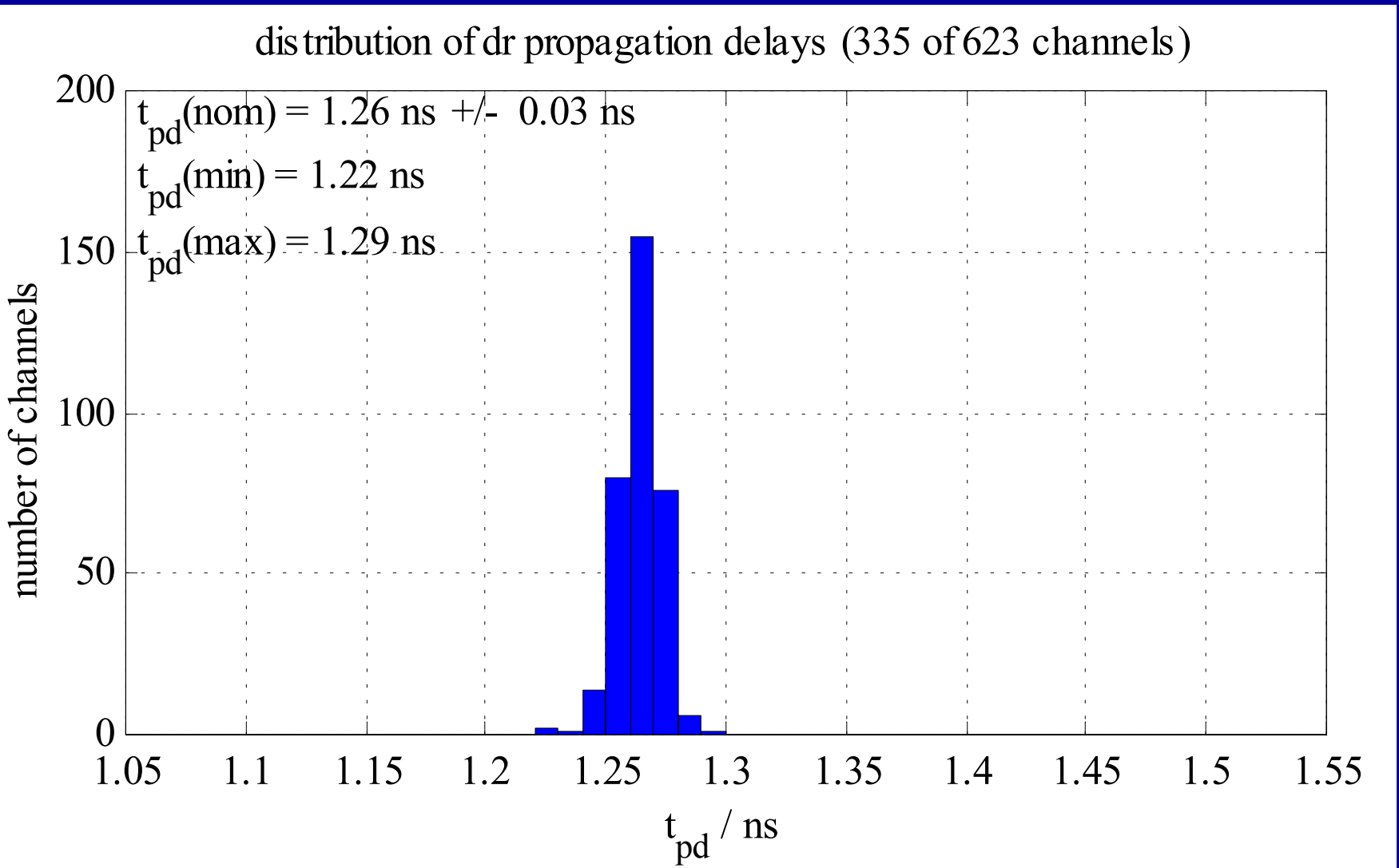
Results: Vertical PC

Step Response



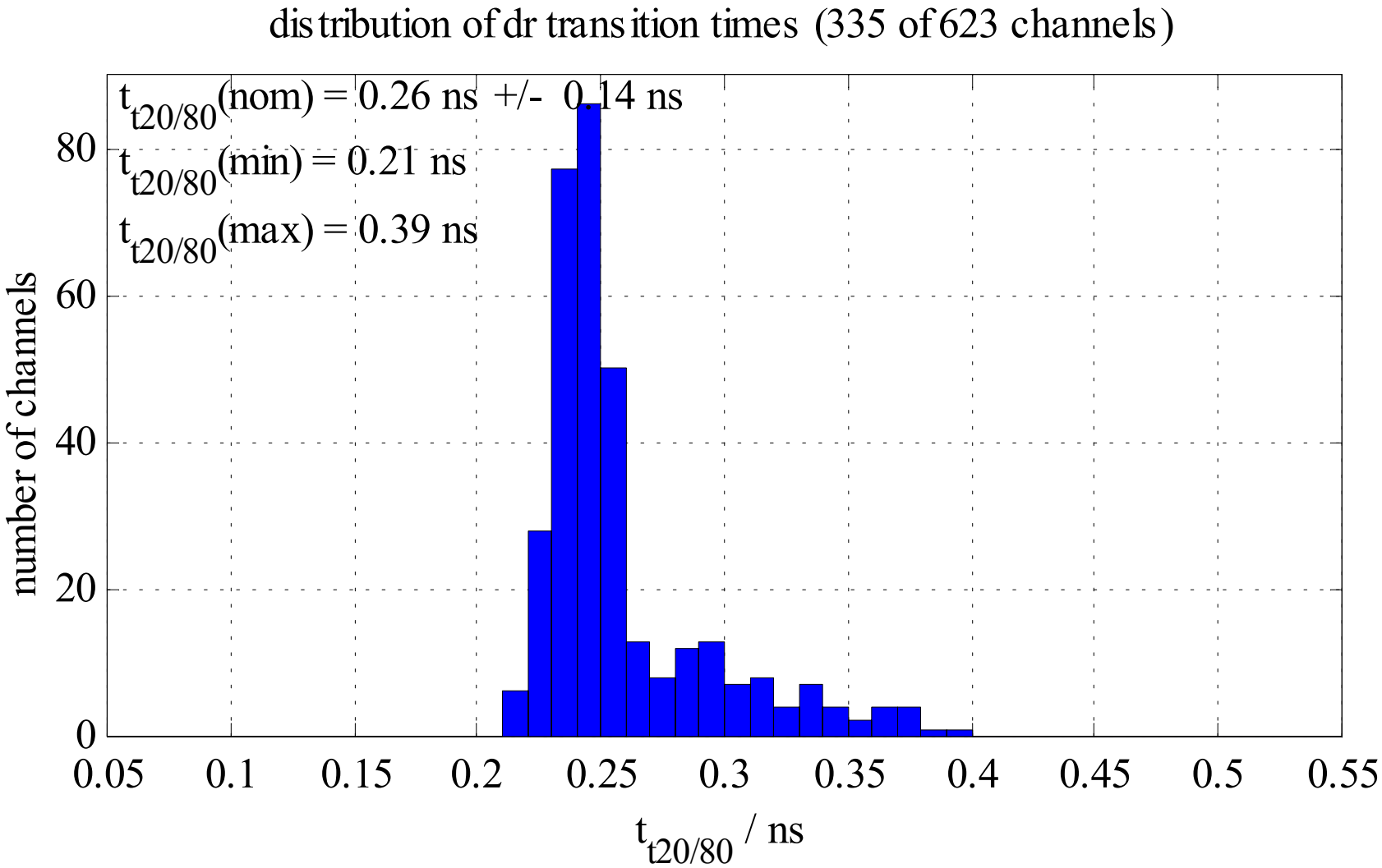
ADVANTEST

Results: Vertical PC Propagation Delay Histogram



ADVANTEST

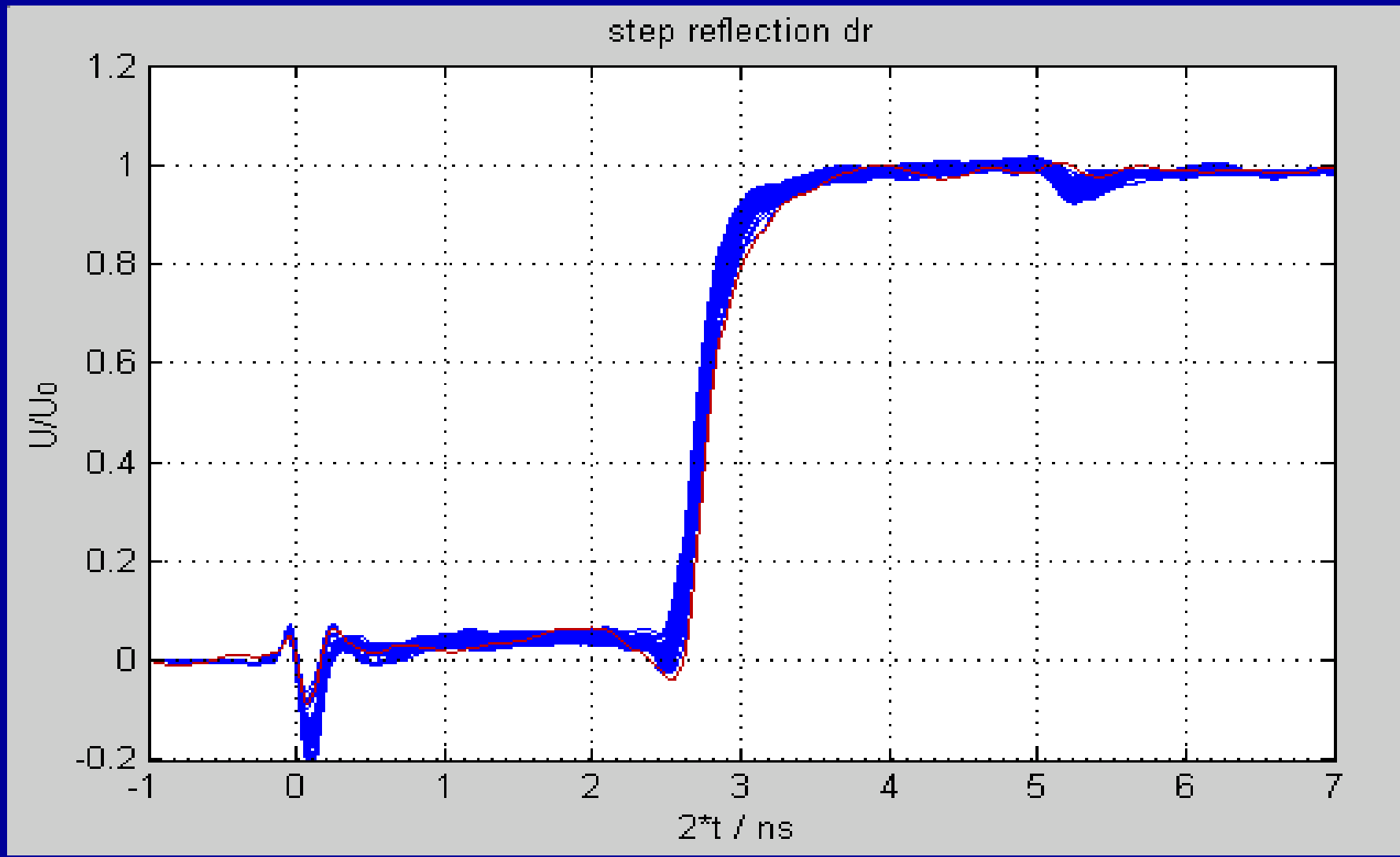
Results: Vertical PC Intrinsic Transition Time Histogram



ADVANTEST

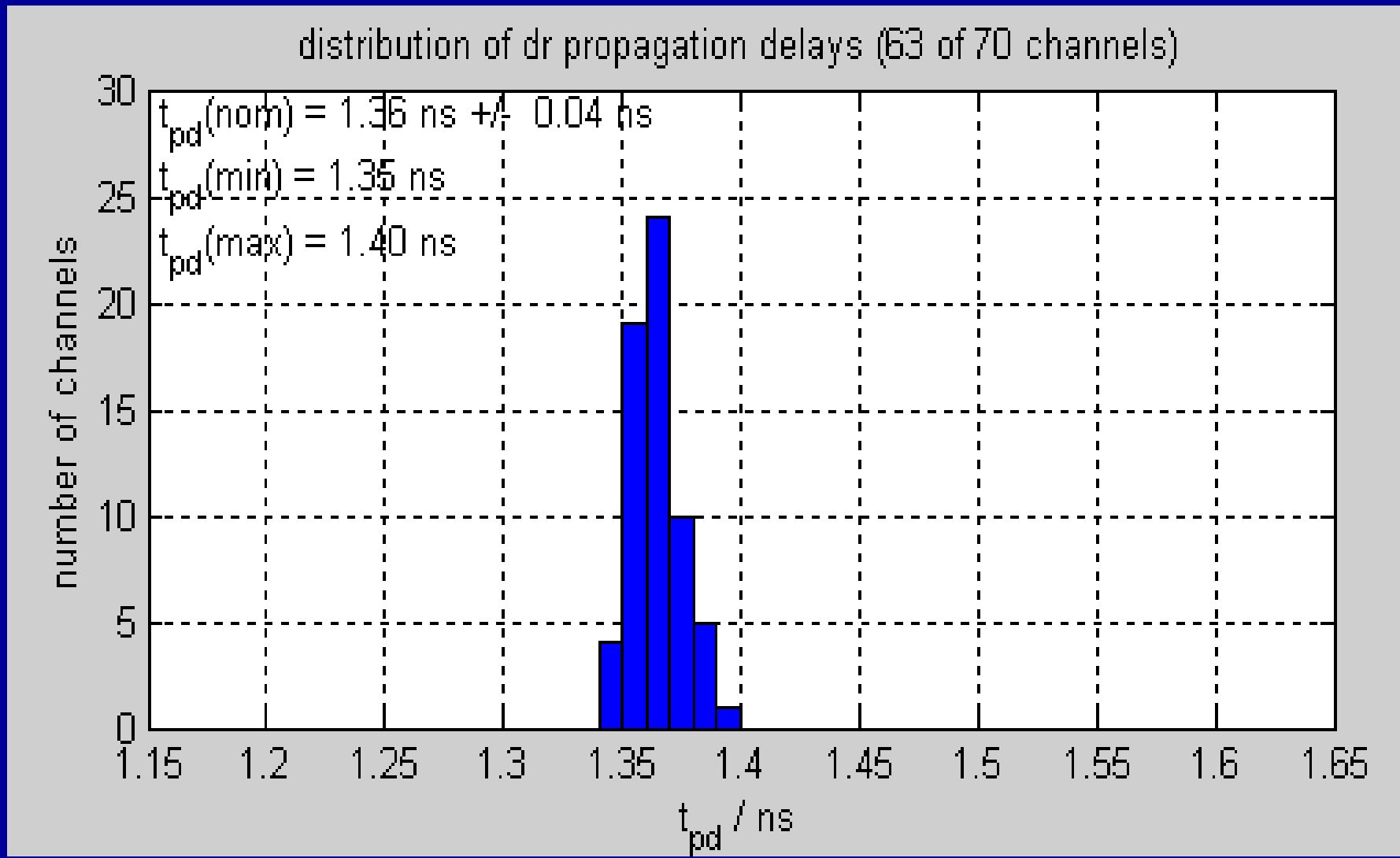
Results: Buckling Beam PC

Step Response



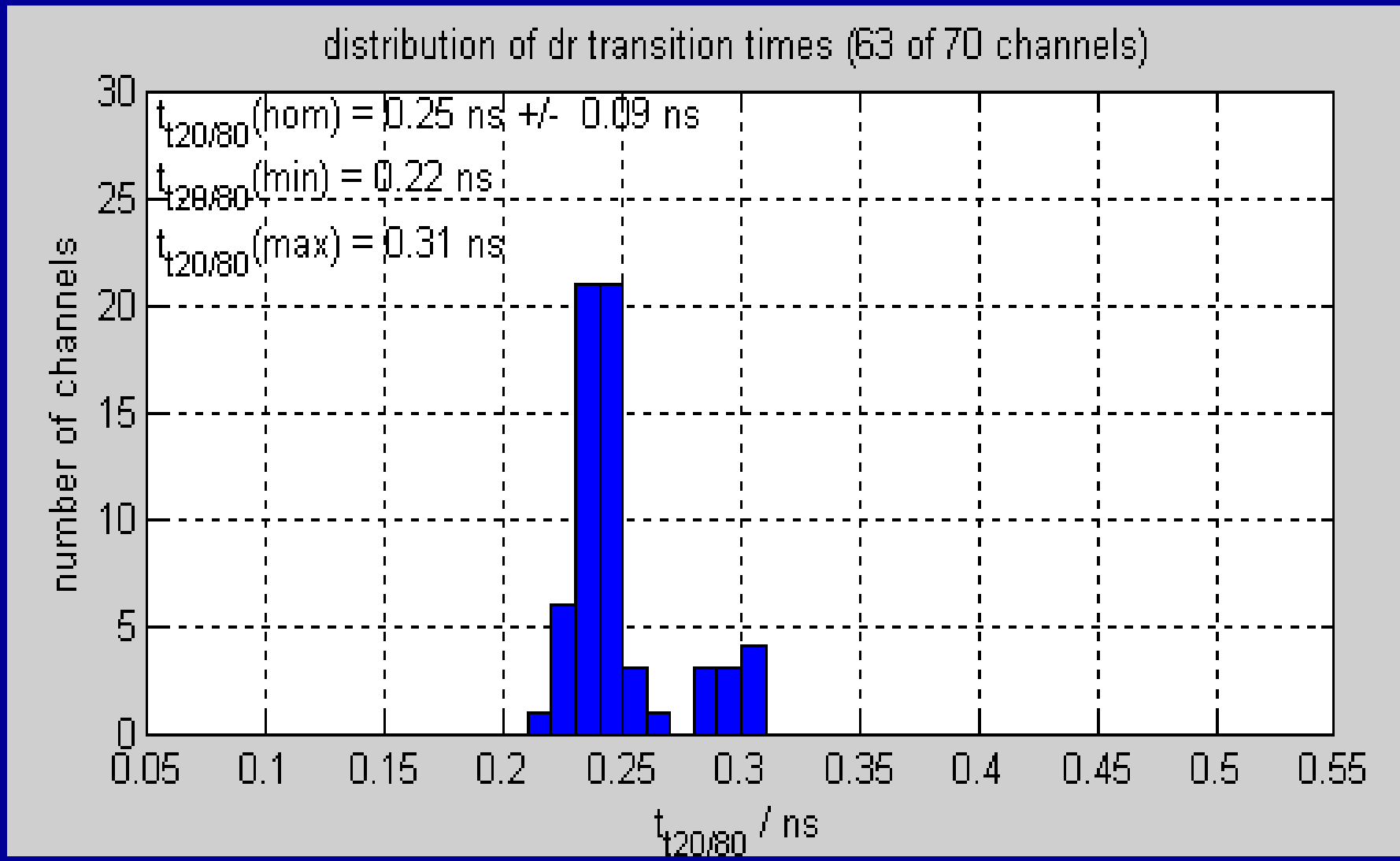
ADVANTEST

Results: Buckling Beam PC Propagation Delay Histogram



ADVANTEST

Results: Buckling Beam PC Intr. Transition Time Histogram



ADVANTEST

Summary

- **TeFiCS®** measures
  - propagation delays and
  - intrinsic transition times

  on **all** signal channels of probe cards or probe assemblies
- Time accuracy better than 10ps
- Amplitude accuracy better than 1%
- Comparison against **user-defined limits** per channel class
- Measurement time **3s per channel**
- Test report generation (responses, histograms, statistics)
- Crosstalk and power / ground stability are not addressed

ADVANTEST

Conclusion

TeFiCS® ...

- enables RF probe card / probe assembly characterisation and automated test of relevant properties from all channels
- helps monitor, compare and improve PC quality with respect to signal integrity and channel-to-channel variance
- allows qualifying and certifying PCs and PC assemblies prior to delivery to customer
- is the first system world-wide for this purpose

ADVANTEST