International SEMATECH Wafer Probe Benchmarking Project

WAFER PROBE ROADMAP

Guidance For Wafer Probe R&D Resources

2002 Edition

Fred Taber, IBM Microelectronics
Probe Project Chair

Gavin Gibson, Infineon

2002 Southwest Test Workshop

Announcing

Publication of the 2002 Edition of the Wafer Probe Roadmap

Compiled by the International SEMATECH Wafer Probe Benchmarking Project

Available at:
http://www.sematech.org/public/docubase/abstracts/wrapper15.htm

Outline

Introduction

Approach

Product Driven Requirements

Wafer Probe Technology Requirements

Wafer Probe Operations Requirements

Difficult Challenges

Wrap-up

Introduction: SEMATECH

- International SEMATECH Mission
  - Members will gain manufacturing advantage through cooperative work on **SE**miconductor **MA**nufacturing **TECH**nology
- Members (12)

Advanced Micro Devices
Agere Systems
Hewlett-Packard
Hyundai
Infineon
Intel
IBM
Motorola
Philips
STMicroelectronics
Texas Instruments
TSMC

Introduction: Probe Project

- Organized 2Q2000
  - Target and Drive Wafer Probe Improvements
    - Operations
    - Probe Card Technology
    - Probe Card Performance
  - Open To All 12 International SEMATECH Member Companies
    - Custom Funded: Dues

Introduction: Probe Project

- Custom Funded Projects
  - SEMATECH: Legal, Technical & Administrative Support
  - Members: Technical Data & Information, Know-how & Direction

Introduction: Probe Project

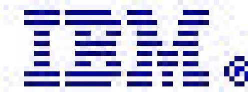
- Benefit
  - Project Members: Value
    - World Class Operations, Methods & Practices
    - Survey Results
  - SEMATECH Members: Awareness
    - Annual Reports
    - Focus Group Output
  - Industry: Guidance
    - Roadmaps, Guidelines & Standards

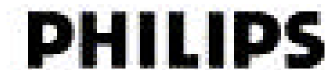
Introduction: Probe Project

- Approaches (On a Pre-Competitive Basis)
  - Benchmark Metrics
  - Best-in-Class Identification
  - Best Practice Sharing
  - Site Visits
  - Networking
  - **Validation of Industry Roadmap Directions**
  - **Consensus Requirements to Suppliers**
  - Sub-Teams/Focus Groups: Specific Topics

Introduction: Probe Project

- Participants





Approach: Industry Engagement

- Determine Desired Roadmap Content
  - 1Q01 Probe Industry Representatives Provide Feedback on 1996 Roadmap
    - Align Member Needs With Supplier Solutions
    - Create Data Input Template
  - Open Meeting at 2001 SWTW
    - Over 50 Attendees
    - Review/Refine Roadmap Template
      - Shaped Final Format & Parameters

Approach: Roadmap Data

- Sources
  - Probe Project Member Companies
    - Each Member Entered Data into the Template
      - Reflects Member's Probing Requirements
      - Across 5 Product Families
        - DRAM, uProcessor, ASIC's, RF & Mixed Signal
  - International Technology Roadmap for Semiconductors (ITRS) - 2001 Update
    - For Selected Template Parameters

Approach: Roadmap Data

- Rollup
  - Facilitated By International SEMATECH
  - Algorithm Captures Production/Mainstream
    - Suggested Guideline: Assume Leading Edge 12-18 Months Earlier
    - Each Parameter From 2002 Through 2005
    - ITRS Reflects 1st Year of Production

Approach: Roadmap Organization

- Chapters
  - Product Driven Requirements
  - Wafer Probe Technology Requirements
  - Wafer Probe Operations Requirements
- Appendix
  - Difficult Challenges

and a

Glossary of Terms

Product Driven Requirements

- Specifications

2001 SEMATECH Wafer Probe Roadmap

	PARAMETER	DESCRIPTION	APPLICATION	YEAR 2001 (Ref)	2002	2003	2004	2005
Specifications	Probe Points (max. #)	Signal / Prw & Gnd eg 150 / 18	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Probe Pad Opening (min. um)	Bond Pad Size Length x Width eg 130 X 90	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Probe Pitch (min. um)	a) Single Row b) Staggered Row / Rows c) Perimeter d) Array eg a85, b65/3, d200	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Bump Size (min. um)	Width:Diameter/Height eg 120/120	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					

Product Driven Requirements

- Interconnect Metallurgy

2001 SEMATECH Wafer Probe Roadmap

	PARAMETER	DESCRIPTION	APPLICATION	YEAR 2001 (Ref)	2002	2003	2004	2005
Interconnect Metallurgy	Pad Thickness (um)	a) =< 1.2 b) =< 1.0 c) =< 0.8 d) =< 0.6 e) Other (Define)	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Pad Metallury	a) Al/Si/Cu b) Cu c) Au d) 0ther (Define)	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Bump Metallurgy	a) Pb/Sn b) Sn/Pb c) Au d) Other (Define) (P)lated or (E)vaporated eg ap, be, ce, de	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Active Structure Under Pad	eg Y / N	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Under Bump Metalurgy (UBM)	a) Pb/Sn b) Sn/Pb c) Au d) Other(Define) eg a	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					

Product Driven Requirements

- Electrical Performance

2001 SEMATECH Wafer Probe Roadmap

	PARAMETER	DESCRIPTION	APPLICATION	YEAR 2001 (Ref)	2002	2003	2004	2005
Electrical Performance	Device Operating Voltages	Operating Voltages (min / max) eg 1.8v / 5v	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	AC Characteristics	Bandwidth (test operating frequency) eg 300	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
		Reflections (max.)	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					

Product Driven Requirements

- Suggested Source: 2001 Edition of ITRS

  http://public.itrs.net/Files/2001ITRS/Home.htm

  - Chapters: Executive Summary, Test & Test Equipment, Assembly & Packaging
    - Pad/Bump Pitch
    - I/O's - Signal & Power
    - Metallurgical Characteristics
    - Device Operating Voltages
    - A.C. Elect. Performance (No Reflections Data Avail.)
  - Under Consideration: Wafer Probe Roadmap Within Future ITRS Updates

Wafer Probe Technology Requirements

- Interconnect Deformation

2001 SEMATECH Wafer Probe Roadmap

	PARAMETER	DESCRIPTION	APPLICATION	YEAR 2001 (Ref)	2002	2003	2004	2005
Interconnect Deformation	Probe Scrub Area	a) Maximum Area in μm^2 b) Maximum % of pad opening eg a50, b100	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Probe Scrub Depth	a) Maximum depth in µm b) Maximum % of pad thickness eg a1, b?	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Bump Diameter/width (max delta)	a) +/- ? µm b) +/- % of diameter	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Bump Height (max delta)	a) +/- ? µm b) +/- % of height	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Reprobe (max.)	# Touchdowns limit (Bump/Pad) eg 4/6	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					

Wafer Probe Technology Requirements

- Multi-DUT

2001 SEMATECH Wafer Probe Roadmap								
	PARAMETER	DESCRIPTION	APPLICATION	YEAR 2001 (Ref)	2002	2003	2004	2005
Multi Dut	Volume (%)	% volume suite of parts that require multi dut	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	XY Area	a] X Dimension (mm) b] Y Dimension (mm) eg 6/8	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Probe Points	Signal:Pwr:Gnd / Touch Pin Count / Touch eg 800	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					

Wafer Probe Technology Requirements

- Interconnect Deformation
  - Pad/Bump Sizes Reducing / Scrub %: Area Stable, Depth Decreasing
    - Approaching Practical Limits of Current Probe Technologies?
- Multi-DUT
  - Percentage Growing
    - Up to Full Wafer For Memory
    - Other Families ~2x in 2005 vs. 2002
    - Probed Area & # of Probe Points Increasing

Wafer Probe Technology Requirements

- Electrical Performance

2001 SEMATECH Wafer Probe Roadmap

	PARAMETER	DESCRIPTION	APPLICATION	YEAR				
				2001 (Ref)	2002	2003	2004	2005
Electrical Performance	Current (max.)	Probe Tip (ma) eg 10	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
		DC Leakage	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	Resistance	Contact (Ohm) eg 1	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
		Series eg 2	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					

Wafer Probe Technology Requirements

- Current (Max.)
  - Probe Tip: Stable Across Product Types
  - Leakage: Stable Across Product Types
- Resistance (Max.)
  - Contact: Stable Across Product Types (<1 Ohm)
  - Series: Stable (<2 Ohms to <4 Ohms Depending on Product Type)

Wafer Probe Technology Requirements

- Thermal

2001 SEMATECH Wafer Probe Roadmap								
PARAMETER		DESCRIPTION	APPLICATION	YEAR 2001 (Ref)	2002	2003	2004	2005
Thermal	Thermal Characteristics	Chuck Set Point (min/max) C eg 125/-10	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
		Soak Times (Minutes) eg 5	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					

Wafer Probe Technology Requirements

- Thermal Performance
  - Chuck Set Point
    - Minimum Typically Reducing
      - ASIC's & Mixed Signal Stable
      - Worst Case: Memory to -40C
    - Maximum Rising
      - Worst Case: Memory to 140C
  - Soak Time
    - Typically Stable Across Product Types
      - Microprocessor Reducing

Wafer Probe Operations Requirements

- Operations

2001 SEMATECH Wafer Probe Roadmap

	PARAMETER	DESCRIPTION	APPLICATION	YEAR 2001 (Ref)	2002	2003	2004	2005
Operations	Order Leadtime (Days)	Leadtime (1st design) Single Dut/ Multi Dut eg 14/21	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
		Leadtime (Reorder) Single Dut / Multi Dut eg 7/14	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
	# Touchdowns per card type before cleaning	OFFLINE a) Cantilever b) Vertical c) Membrane d) Other(Define) eg. a300, c0	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					
		ONLINE a) Cantilever b) Vertical c) Membrane d) Other(Define) eg. a300, c0	Memory					
			ASICS					
			Microprocessor					
			RF					
			Mixed Signal					

Wafer Probe Operations Requirements

- Unit Cost & Cost of Ownership
  - Not Covered
  - Need for Consistent Industry-wide Models
- Leadtime
  - Single DUT & Multi-DUT
    - 1st Order Time Shortening; Reorder Mostly Stable

Wafer Probe Operations Requirements

- Touchdowns Before Cleaning
  - Cantilever
    - Online - Mostly Stable
    - Offline - Memory & Mixed Signal Increasing Significantly; Others Mostly Stable
  - Vertical
    - Online - Most Product Types, Slight Increase
    - Offline - All Product Types, Significant Increase

Difficult Challenges

- Within Test & Test Equipment Chapter of 2001 ITRS (Reproduced in Probe Roadmap)
  - High Frequency Probing
  - Reduced Geometry
  - Multi-DUT
  - Probing at Temperature
  - Product: Metallurgies & Sensitivity to Probing
  - Probe Cleaning
  - Cost & Delivery
  - Probe Metrology

Wrap-Up

- New Wafer Probe Roadmap
- Industry Engagement is Key
  - Align Users and Suppliers
- Annual Update is Planned
- Feedback Encouraged
  - Questions, Comments, Suggestions, Errata……etc.
    - Collection Focal Point: International SEMATECH

Acknowledgements

- Thanks to:
  - The Probe Industry participants. Their guidance and insight into developing the scope of the Roadmap was invaluable
  - Jim Ammenheuser of SEMATECH for his dedicated contributions to the planning, organization and compilation of the Roadmap
  - The Member company principals. The Roadmap project would not have been possible without their devotion and resolve to see it through.