Best Practice Metrology Protocol

Presented to:

SOUTHWEST TEST WORKSHOP 2002

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Goals of Presentation

1. Provide best known practices for "metrology methodology"
2. Detail troubleshooting techniques
3. Discuss common mistakes
4. Provide guidelines on when and what to test

Basic Terminology

1. **Probe Card (PC)** – Assembly consisting of circuit board through test head
2. **Tester** – Metrology tool
3. **Pogo Pins** – Spring contacts connecting tester to the probe card circuit board
4. **Pogo Pin Pad** – Pad on PCB that contacts pogo pin
5. **Motherboard** – Tester bed containing pogo pins – simulates different platforms
6. **PCB** – Printed Circuit Board of the PC
7. **Contact resistance** – a/k/a C_{RES}
8. **ODL** – Overdrive leakage

Step 1: First Things First

Know:

1. Production test requirements of the probe card
2. Equipment specifications *vs* testing requirements
3. Applicable test techniques
4. Physical and electrical characteristics inherent in probe card technology – current carrying capacity, deflection force, etc.

Step 2: Know The PC Specifications

1. Leakage
2. Planarity
3. Path Resistance
4. Alignment
5. Overdrive leakage
6. Wire check - XY probe location to pogo pin pad
7. Component – layout, value, type

Step 3: Determine Test Equipment

1. Appropriate test equipment
2. Mother board – platform specific
3. Meters – off-line testing
4. Power supplies – required to drive components

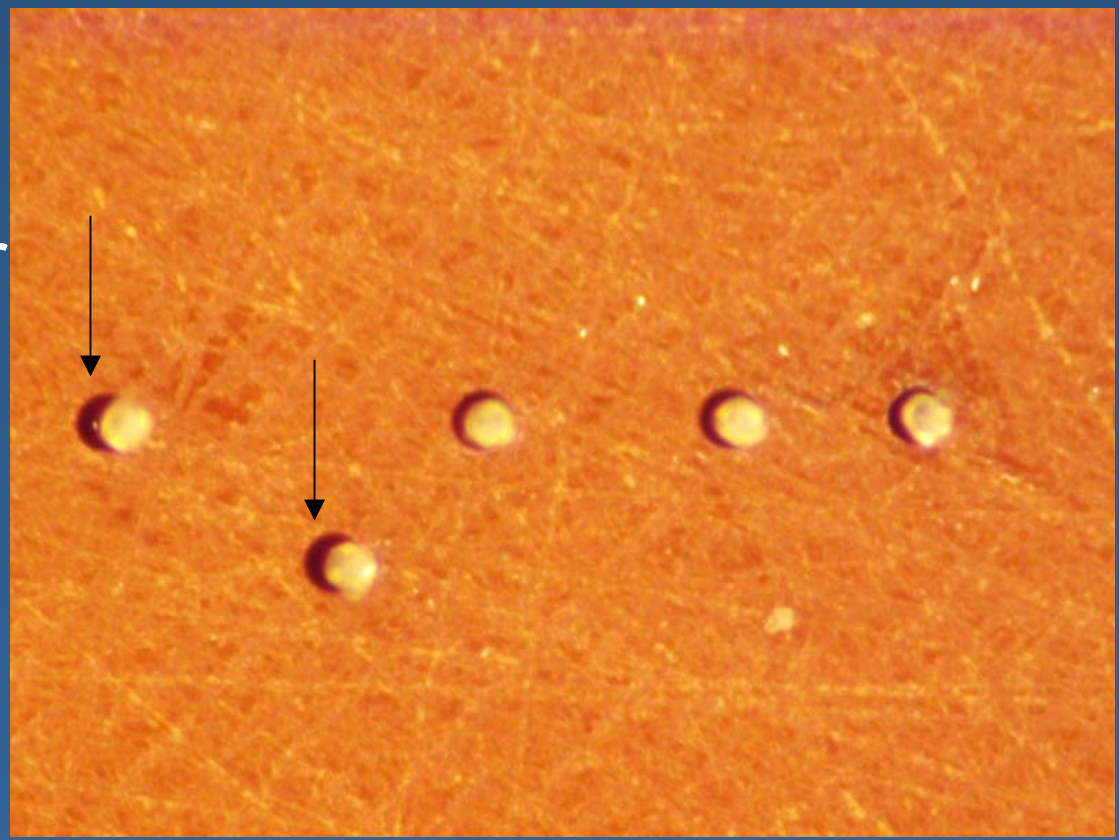
Step 4: Verify Test File

1. Verify XY coordinate information to associated pogo pin pad (edge)
2. Verify component layout
3. Verify set-up test specifications
   a. Overdrive
   b. Limits – physical and electrical
   c. Dwell time

Step 5: Visual Inspection

Look for General Defects

1. Bent probes
2. Debris
3. Hand & finger prints
4. Missing components, hardware



Step 6: Start Testing!

Order of testing for "first article" probe card

1. Leakage – quickest, easiest test
2. Bulk Planarity & Path Resistance – most closely matches actual production testing
3. Overdrive Leakage
4. Alignment
5. Full Planarity & Path Resistance – bussed probes test individually
6. Wire Check
7. Components

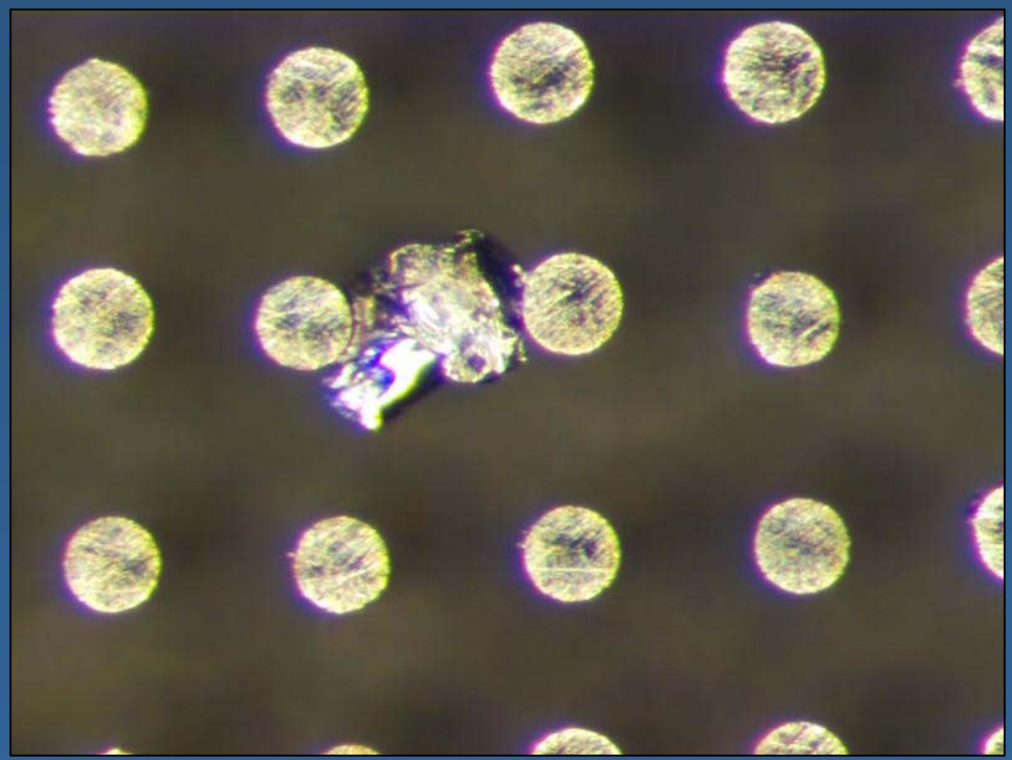
Troubleshooting - Basics

1. KISS – Keep it simple smarty – look for most obvious reasons for failure – i.e. bent probe, cleanliness
2. Troubleshoot on tester whenever possible - start with activities that allow testing to flow with minimal interruption
3. Different failures follow different progressions

Troubleshooting PC After Leakage Test Failure

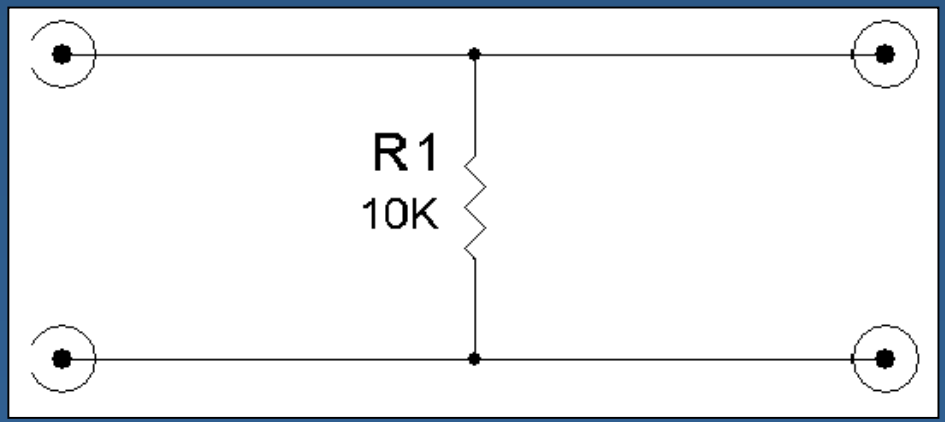
Note: Test most effected by external factors

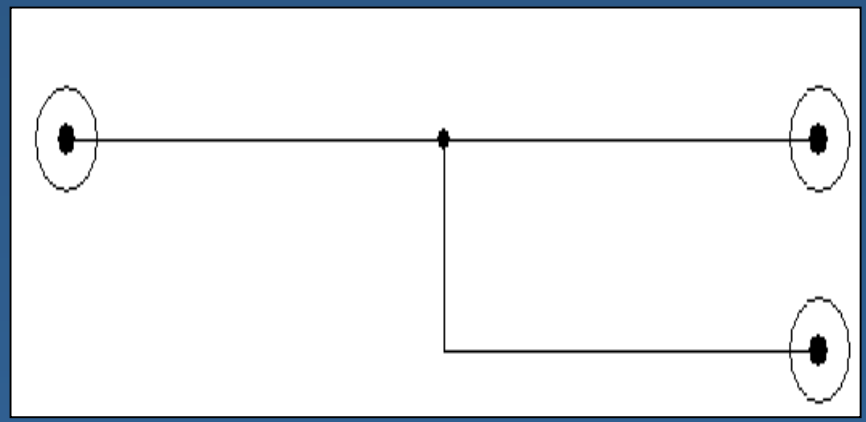
1. Revisit cleanliness issue especially debris and hand and fingerprints



… After Leakage Test Failure (con't.)

2. Check components
   a. Locate defective components
   b. Identify apparent failure due to component layout – i.e. resistor between two traces

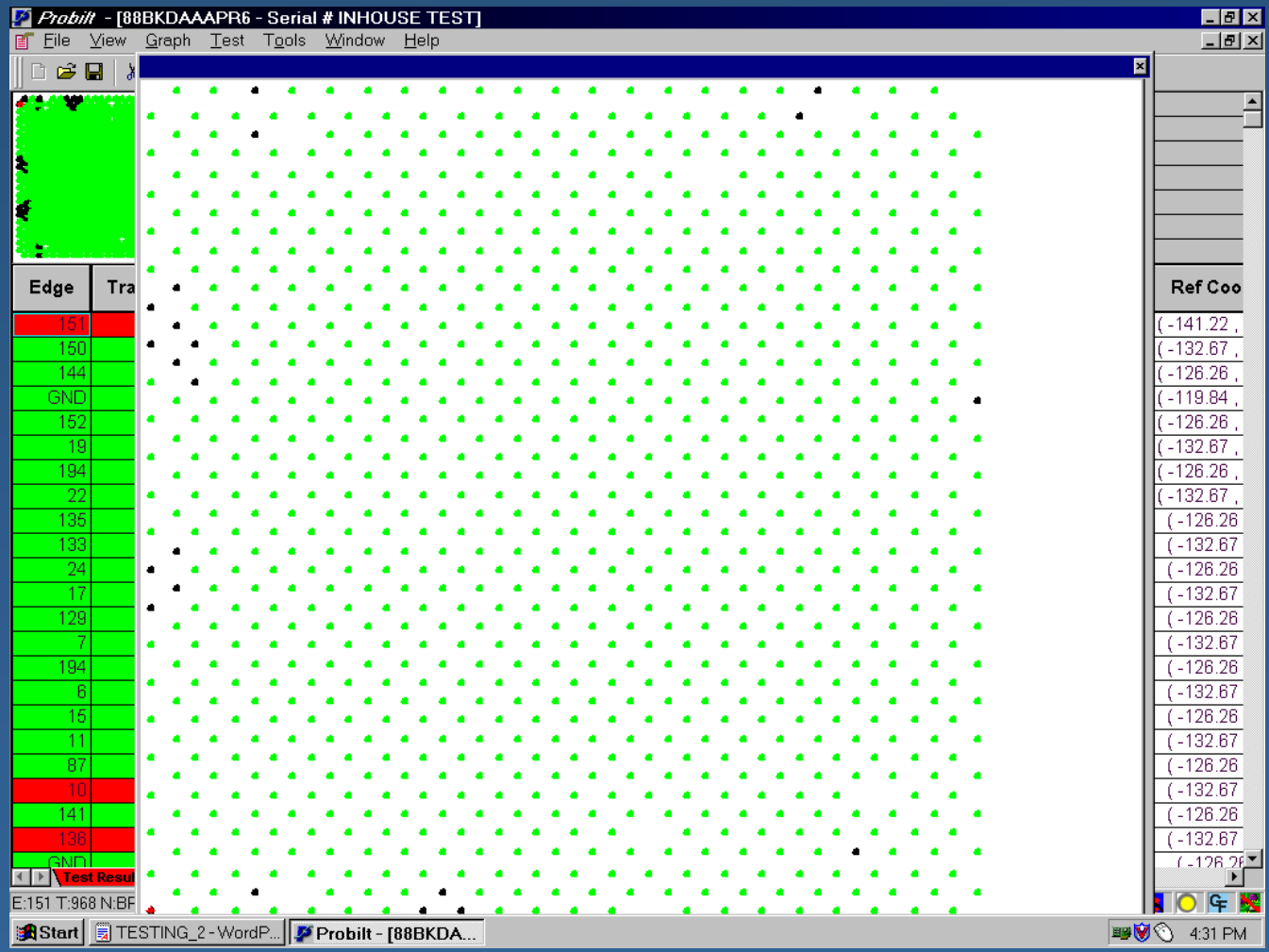




3. Verify test equipment – test probe card off line

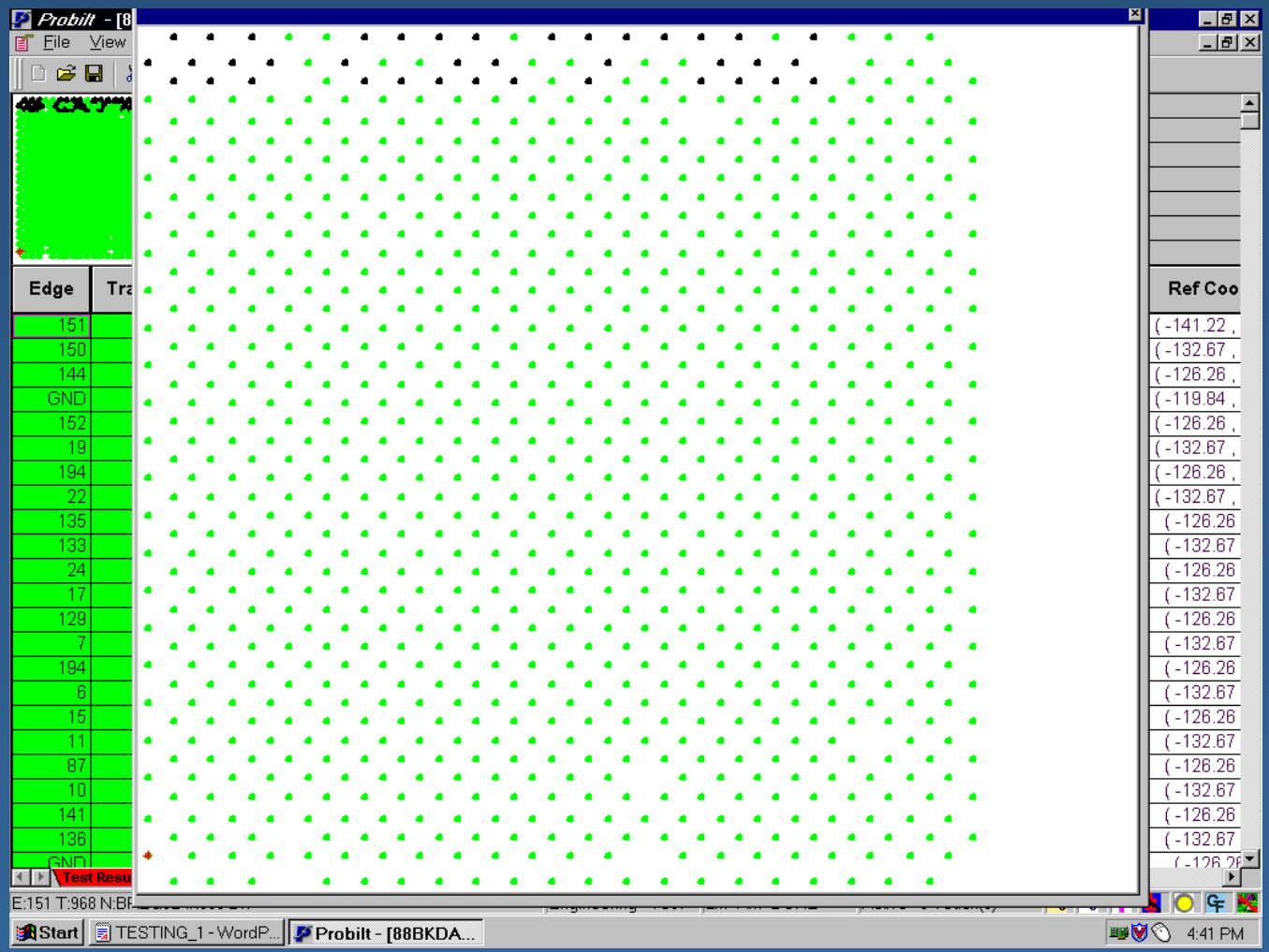
… After Bulk Planarity & Path Resistance Test Failure

Check array display first. Dispersed planarity failure – often PC issue not equipment issue.



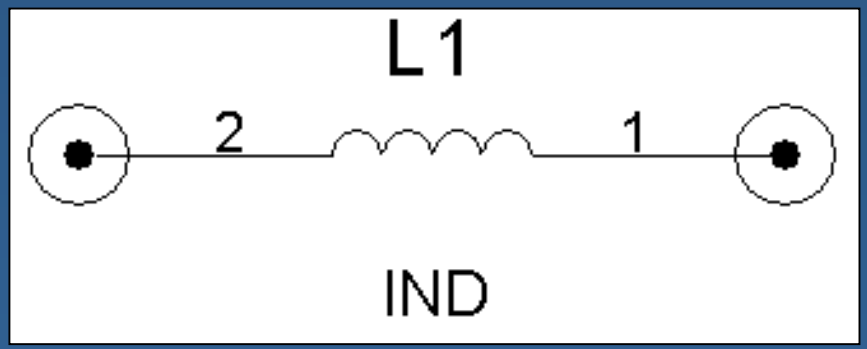
… After Bulk Planarity & Path Resistance Test Failure

Grouped planarity failure – *check* test equipment calibration.

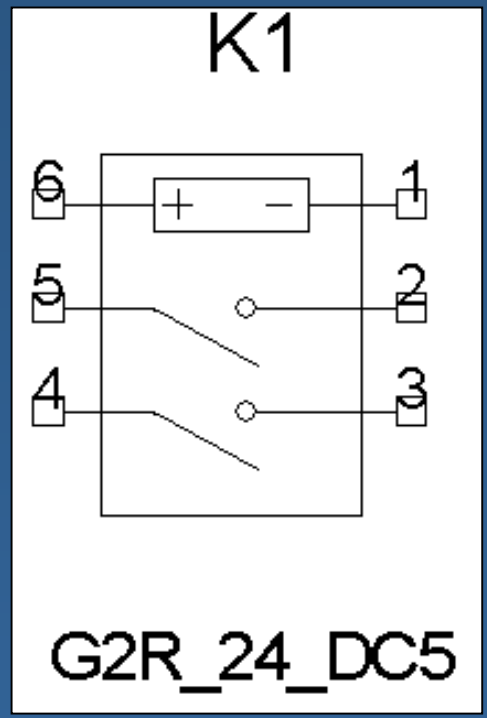


… After Bulk Planarity & Path Resistance Test Failure (con't.)

1. Verify test file for correct specifications
2. Revisit cleanliness issues – bent probes, debris, lint, etc.
3. Component related



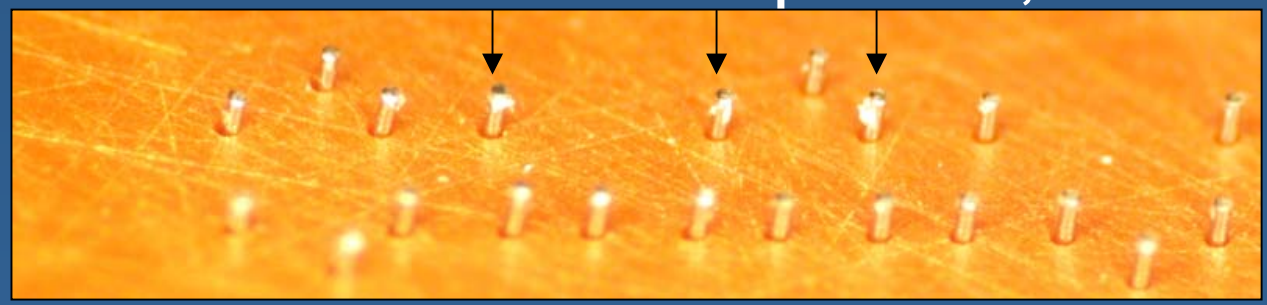
4. Verify test equipment



… After Alignment Test Failure

Note: Alignment refers to probe tip location in relationship to pad. This is not a theta measurement.

1. Verify XY co-ordinates
2. Revisit cleanliness issues – bent probes, debris, lint



3. Verify test equipment

… After Overdrive Leakage Test Failure

Note: 95% of ODL failures due to product failure NOT test protocol - exact opposite of other tests.

1. Verify test file for correct specifications
2. Inspect for bent probes and debris
3. Verify test equipment

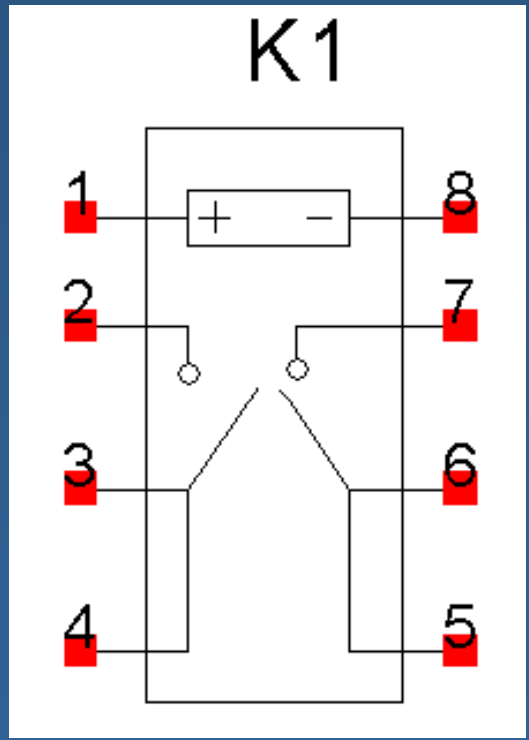
… After Full Planarity & Path Resistance Test Failure

Note: These failures will generally be bussed probes that have been individually tested.

1. Verify test file for correct specifications
2. Revisit cleanliness issues
3. Verify test equipment

… After Wire Check Test Failure

1. Verify orientation of array - *CRITICAL*
2. Verify pogo pin pad designation to XY location
3. Inspect for bent probes and debris
4. Component operation
5. Verify equipment

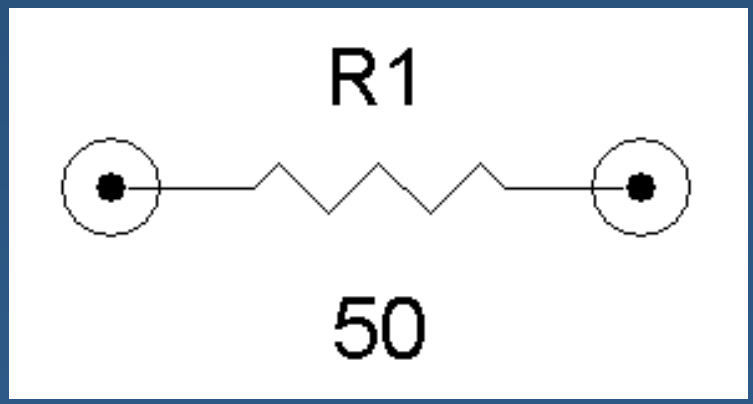


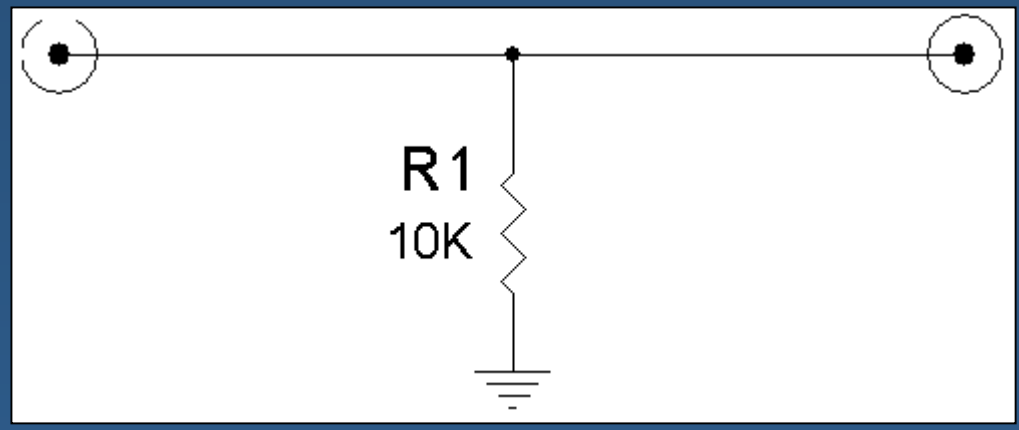
… After Component Test Failure

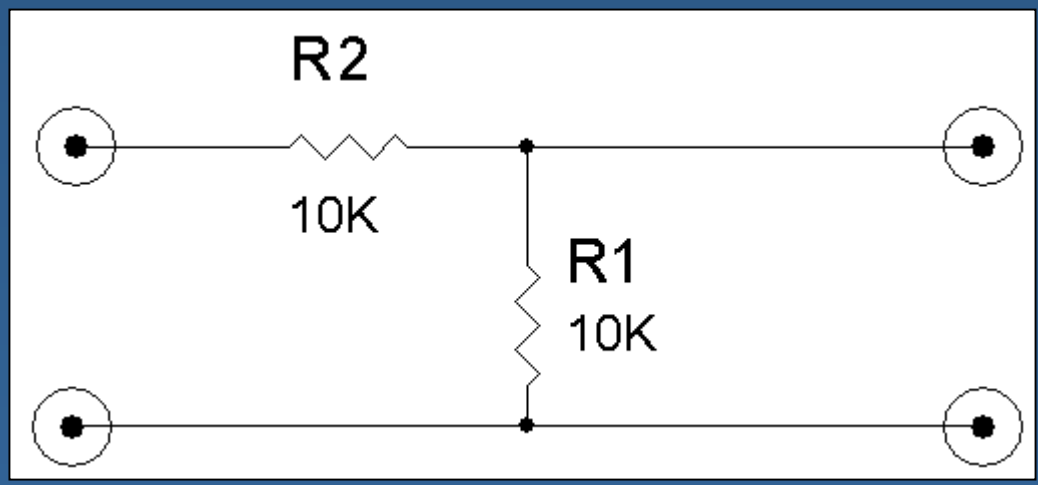
Note: Components can cause different failures (apparent and real) during different tests.

1. Verify test file for correct specifications
   a. Component value correct
   b. Component layout correct
   c. Component type correct
2. Verify test equipment

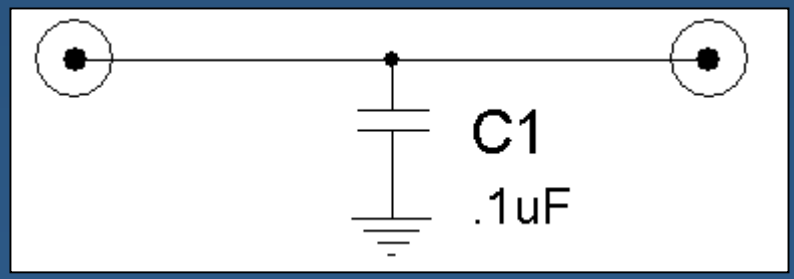
... more on Component Test Failures

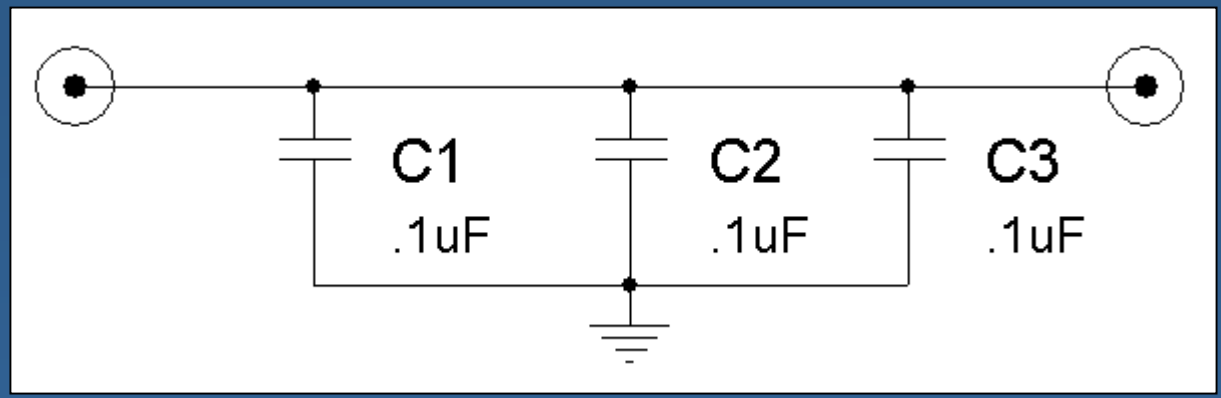






... more on Component Test Failures





Tricks of the Trade

1. Verify connection between probe card and tester
2. Use fizz test to prove out opens
3. Try to verify and resolve failure before removing probe card from tester – i.e. debris
4. Flag certain passing criteria as “failure”– quick way to pinpoint crucial component verification.

FIZZ Test

Most Common Mistakes

1. Poor handling
2. Incorrect documentation
   - Different nomenclature between vendor and probe card customer
3. Misinterpretation of test results
4. Equipment set-up
5. Orientation of the array

Misinterpretation of Test Results

Edge	Trace	Pad Name	Pad #	Die #	Align Error	Planarity	Cres	Wire Check
0	975	HBD17	975	1	N/R	-0.1	4.61	N/R
1	861	HBD14	861	1	N/R	-0.26	5.47	N/R
2	886	DINVB1	886	1	N/R	-0.2	4.66	N/R
3	887	HBD28	887	1	N/R	-0.41	5.07	N/R

Edge	Trace	Pad Name	Pad #	Die #	Align Error	Planarity	Cres	Wire Check
0	975	HBD17	975	1	0.72	-0.1	4.61	3
1	861	HBD14	861	1	0.37	-0.26	5.47	2
2	886	DINVB1	886	1	0.22	-0.2	4.66	1
3	887	HBD28	887	1	0.29	-0.41	5.07	0

Misinterpretation of Test Results

Edge	Trace	Pad Name	Pad #	Die #	Align Error	Planarity	Cres	Wire Check
0	975	HBD17	975	1	0.46	N/F	O/R	3
1	861	HBD14	861	1	0.29	N/F	O/R	2
2	886	DINVB1	886	1	0.23	N/F	O/R	1
3	887	HBD28	887	1	0.19	N/F	O/R	0

Edge	Trace	Pad Name	Pad #	Die #	Align Error	Planarity	Cres	Wire Check
0	887	HBD17	887	1	0.13	-0.06	4.62	0
1	886	HBD14	886	1	0.38	-0.24	5.34	1
2	861	DINVB1	861	1	0.3	-0.19	4.66	2
3	975	HBD887	975	1	0.29	-0.41	5.13	3

Calibration

Note: Test results are only as good as calibration of equipment

1. Adhere to equipment manufacturer's calibration schedule
2. Run daily calibration of motherboard test platform to tester
3. Make OEM "calibration" procedure part of technician training

When and What to Test

Card Type	Leakage	Bulk Planarity & Path Resistance	Overdrive Leakage	Alignment	Full planarity & path resistance	Wire Check	Components
First Articles	X	X	X	X	X	X	X
Re-Orders		X					
Repaired Cards		X					
High Volume		X	X				
Intermittent Usage		X					

Conclusions

1. Good in-house metrology can keep probe cards in production and on-line
2. Preparation is the key to metrology that works for you – not against you
3. Interpretation of data is as important as the data itself
4. It's the simple stuff that kills you