Intel® Sort-Interface-Unit (SIU) Design Methods for Reducing Burn Rates on Tight-Pitch C4 Logic Arrays

Kip Stevenson and Pooya Tadayon

Intel Corporation

Sort Test Technology Development

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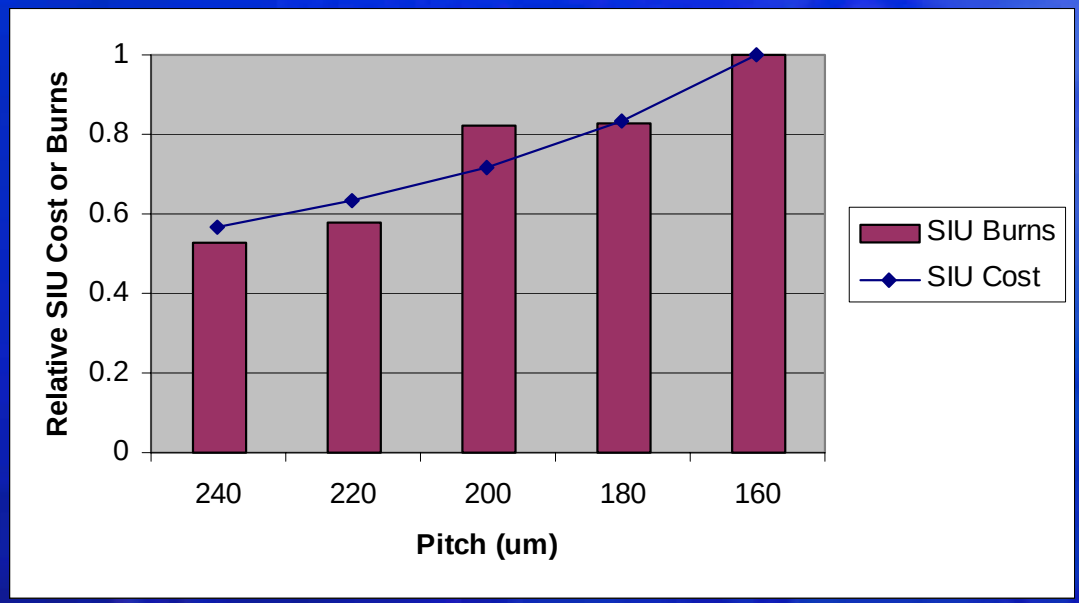
Problem Statement

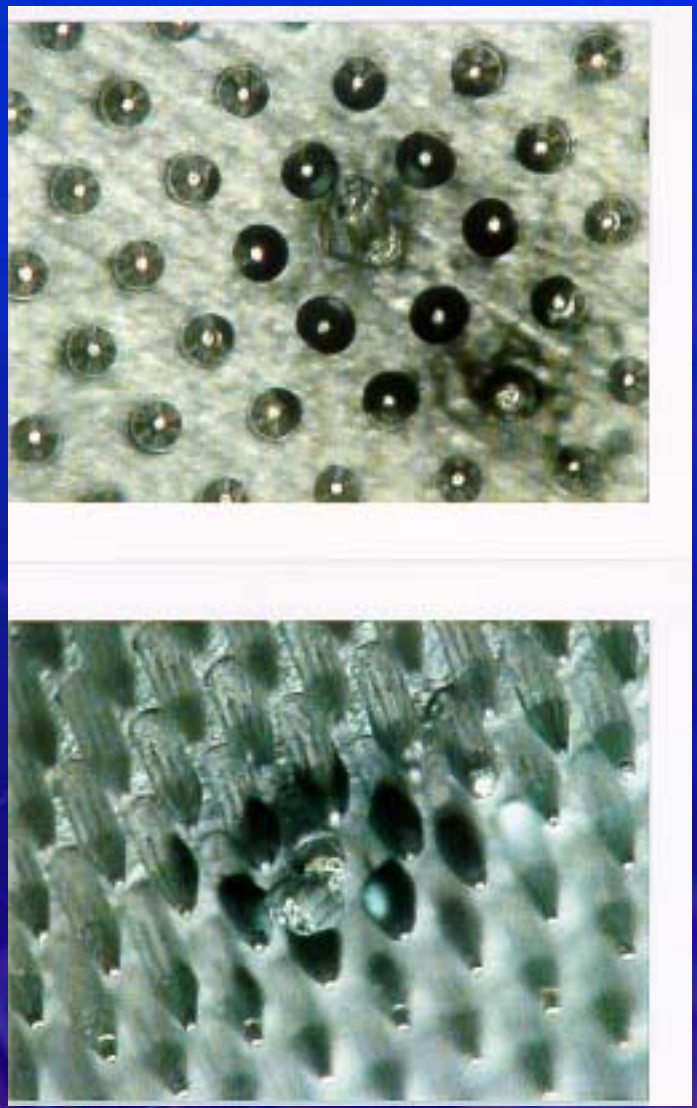
- **Logic Test Challenge: Reduce or maintain test cost in the face of aggressive technological scaling for increased power and reduced array bump pitch.**
  - **Increased Power Density**
  - **Increased Probe Density**
  - **Increased Failure Modes**
    - **Probe burning**
    - **Probe-to-Probe shorting**
    - **Die defects**

SIU Cost and Burn Trends

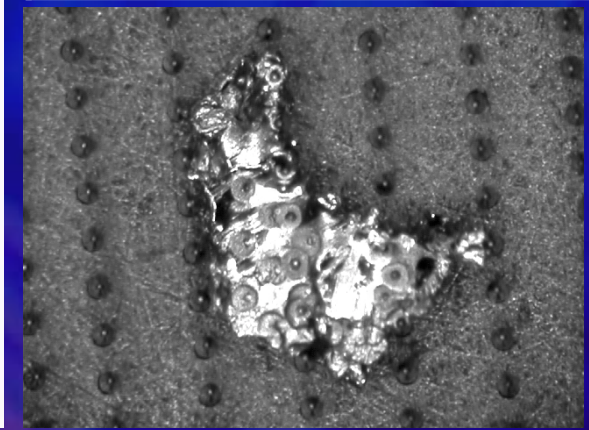


- Burn Rate translates into Higher Cost of Ownership due to:
  - Increased early lifetime SIU failures
  - Larger SIU inventories on reserve
  - Reduced Test Capacity due to slower TPT
  - Increased potential for DUT damage

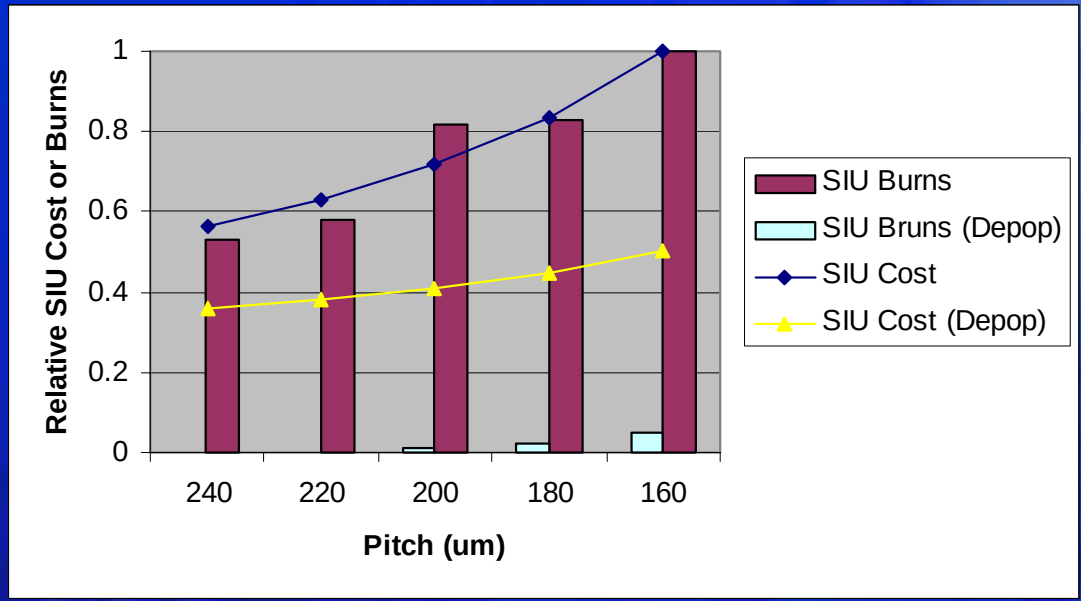
SIU Burns - Examples



Burn Type	No. Probes affected	Process Impact
I: Massive Burn	> 3	Catastrophic burn, Probing Stopped, SIU repair difficult / impossible
II: Bridging	2-3	Large size, Probing Stopped, SIU repair / cleaning needed
III: Bump Pick-up	1	Material stuck on probe, Probing may / may not need to be stopped, SIU easy to repair



SIU Burn Rate Reduction Proposal



- Power/Ground Probe Depopulation has tremendous potential to maintain cost while reducing burn rate:
  - Models predicts ~ 10x Lower Burn Rate
  - SIU unit cost decreased
  - Smaller SIU inventory needed

Intel® Depopulation Design Rules

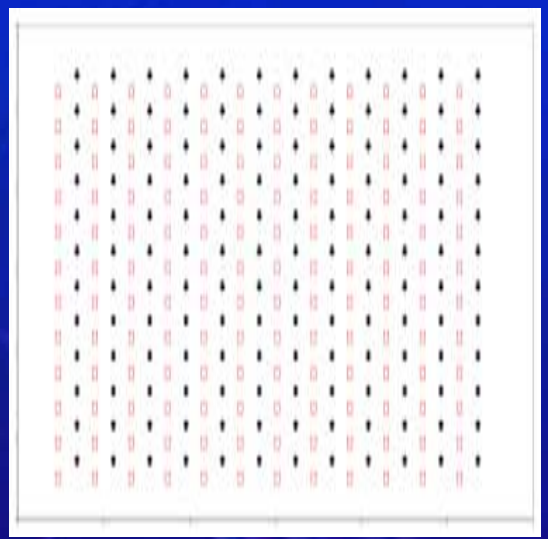
- Use selective depopulation of Pwr/Gnd array to increase the spacing between probes.
  - Pros:
    - Reduce likelihood probe-to-probe bridging
    - Reduce impact of bump defects
  - Cons:
    - Increased current / probe
    - Test performance impact
- Depopulation aims to strike a balance between burn rate reduction and performance impact

Intel® Depopulation Scheme

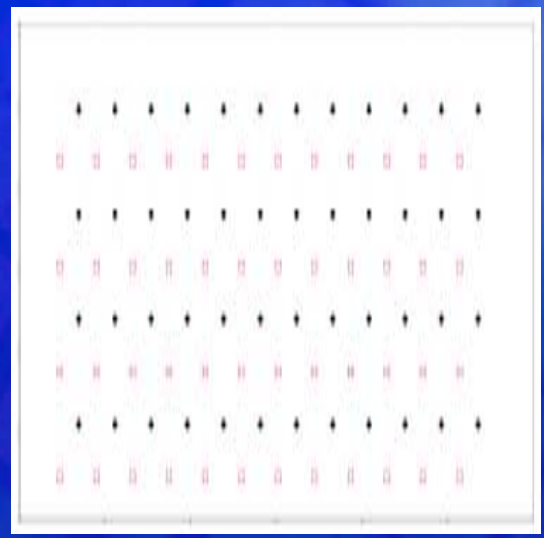
- Min Spacing
  - Adjacent pwr/gnds within a minimum radius (R_min) should not be probed.
- Uniformly Depopulate Pwr/Gnd
  - lower but balanced mechanical force
- 1:X “Odd” Depop Rules
  - 1:3, 1:5, 2:5, 3:5, … Row or Column
  - 1:3, 1:5, … with in Row or Column w/ offset
  - Sequential 1:X Combinations

Depopulation Examples

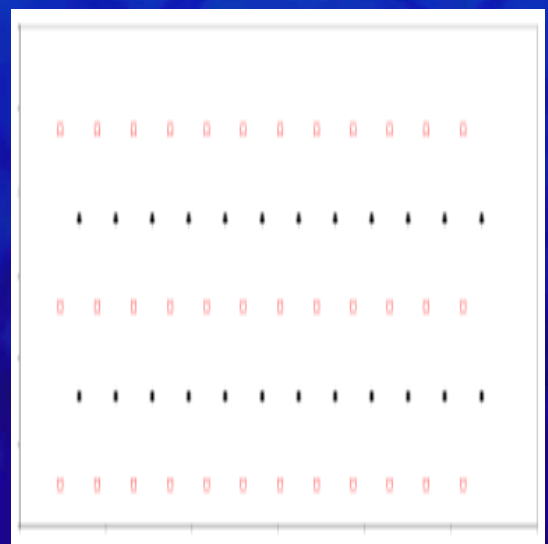
1:X Row (or Column)



1:3



1:5

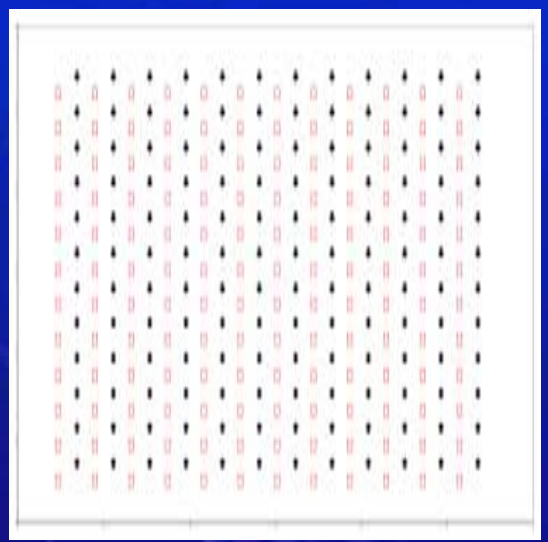


Code:

- Power
- Ground

Depopulation Examples

1:X within Row w offset



1:3

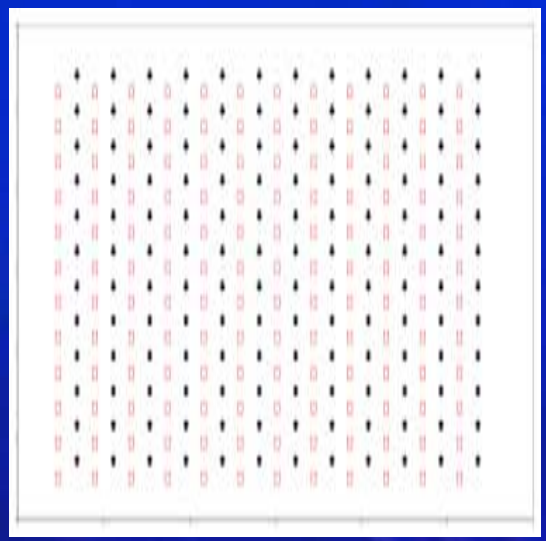
1:5

Code:

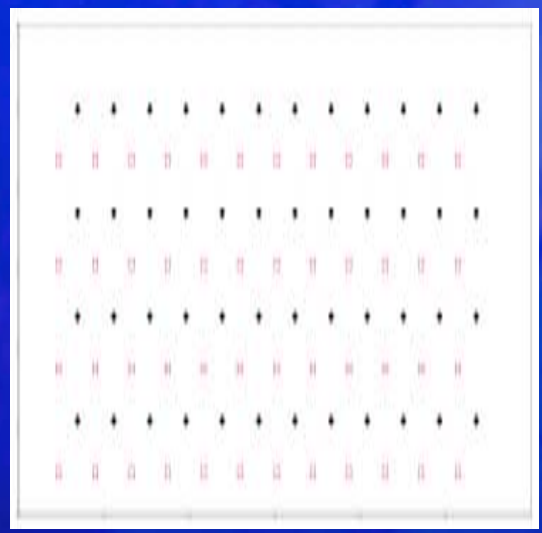
- Power
- Ground

Depopulation Examples

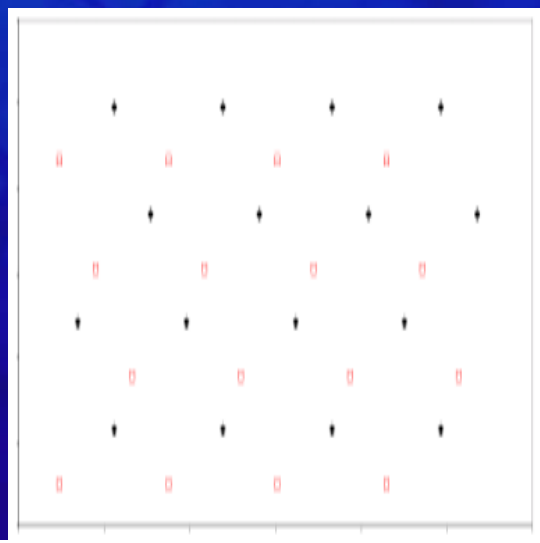
1:X Sequential Combination



1:3
Row



1:3
w/
offset



Code:

- Power
- Ground

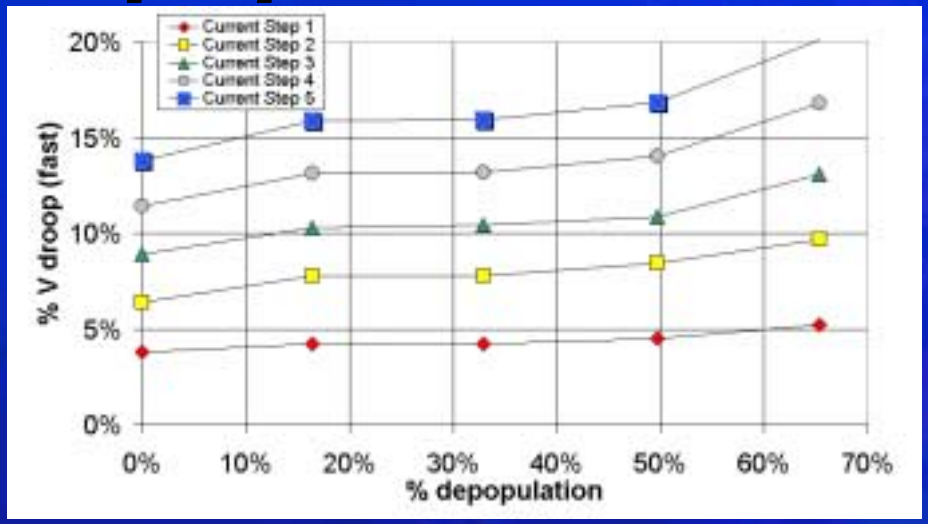
Concerns / Considerations

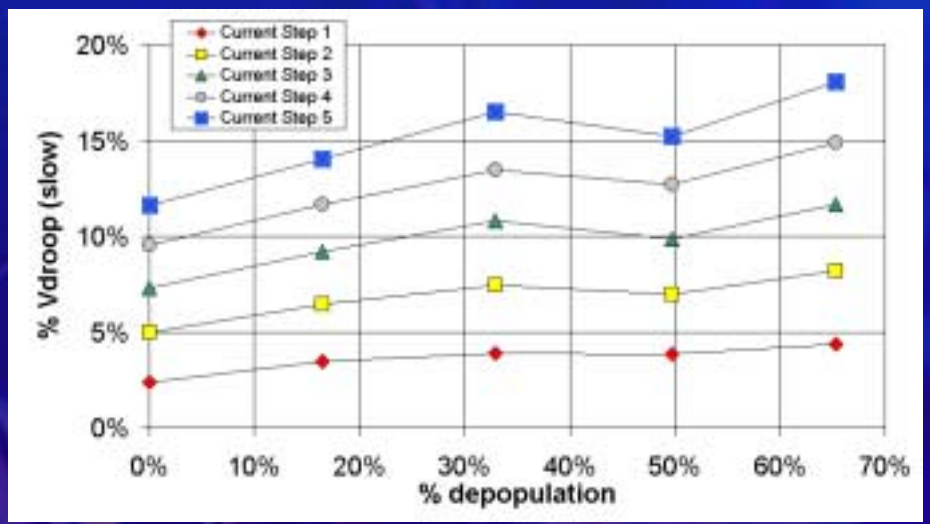
- Probing Force
  - Use uniform depop to prevent regions of high mechanical / electrical stress.
- Current / Probe
  - Max Current Probe Rating requires Minimum Number of Probes: (N_min = X* Max_I + m)
- Power Delivery
  - Vcc Droop = F(N, I_step, …)
- Test Performance
  - Test Yield, Test Time, Device Parametrics

Power Delivery / Performance Impact

- "Product A" -- Vdroop vs. Depopulation
  - Measured Vdroop / Test Yield for successively depop'd SIU.
    - Removed ~ 16% probes / stage
- "Product B" -- Pilot
  - Head-to-Head Sort Comparison for POR (uniform) vs. 1:3 Depop Designs
- "Product C" -- Pilot
  - Head-to-Head Sort Comparison for POR (non-uniform) vs. 1:3 Depop Designs

Intel® "Product A" – Vdroop vs. Depop





Vdroop Increases w/ Current Step + Depopulation

No statistically significant differences in Test Yield, Test Time, Device Parametrics

Depopulation up to ~50% still acceptably within Design Goals for Performance

Intel® "Product B" / "Product C" – Pilot Results

- Depop SIU performed equal to / better than POR SIU for Yield, Test Time, Leakage, Burn Rate
- Depop SIU had Max Frequency differences but no additional Frequency variation or noise
  - Front-End to Back-End Unit Correlation Unaffected

Product	Yield	LKG	Fmax change	Vmin	Test Time	Burn Rate
"Product B"	NC	NC	- 3.4%	NC	NC	POR=3 Depop=0
"Product C"	NC	NC	+ 4 %	NC	NC	Type I, II lower

Summary

- Increasing trend in SIU Burn Rate due to increased power and reduced bump pitch poses tremendous test challenge.
- Selective Depopulation enables significant burn rate reduction at reduced cost w/ some potential impact to test performance.
  - Power Delivery / Burn Rate tradeoffs must be balanced.
- Uniform Depopulation can be achieved w/ simple 1:X rules.
- Intel® results demonstrate significant burn rate reduction w/ limited or no statistically significant reduction in test performance.