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for production probe cards

Production Test of Process Control Monitors (PCMs) with Pyramid Probe Cards

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Goal of Presentation

- Communicate a joint evaluation effort between Texas Instruments, Keithley Instruments and Cascade Microtech investigating the use of Pyramid Probes for probing process monitors with copper pads meeting the shrinking requirements of smaller scribelines.

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Abstract:

Process monitors are used extensively in semiconductor fabs to optimize yields, provide process control feedback, and assure device quality. The scribelines or streets used for PCMs are under the same unrelenting density pressure as IC lithography. Reducing the scribeline by 50 microns on a 5 mm square die, for example, results in a net reduction in area and cost of 2%. This can provide a huge ROI for large wafer fabs. Wafer saw and blade manufacturers are continously reducing saw kerf requirements and PCM pad size is becoming a limiting factor in realizing this competitive advantage. This paper presents DC parametric performance measurements in the femtoamp / femtofarad range for semiconductor test structures with Pyramid Probes. Results will include probing both normal aluminum pads and copper pads. Contact resistance, probe pad damage, multiple probe cycles and probe life time results for both pad materials are also discussed.

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Outline:

- DC Parametric requirements
- Design approach
- Electrical performance
- Contact resistance performance
- Probe mark budget
- Conclusion

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DC Parametric Requirements

- General application is for monitoring test key leakage and capacitance
- Typical production requirements
  - 1-2 pA, 1-2 pF measurements
    - 0.1 pA, 0.1 pF parasitics
- Leading edge engineering requirements
  - 10-50 fA measurements
    - 1-10 fA parasitics
- Probe pads shrinking to meet scribe line shrinks
  - 60-70 um typical today >> 50-40 asap

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Design Approach

- For reference, a typical functional test spec is 10 nA/volt
  - Doesn't require guards (100 megohm)
- Guards required below 1 nA (1 gigohm)
  - milli, micro, nano, pico, femto
  - Typical of parametric test equipment
  - Guard theory: The guard is driven by a separate amplifier to the same voltage as the test pin to reduce current flow to external conductors

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Pyramid Probe Card with Keithley S600 Interface

- Coax force-sense guard
- Twinax routed cables to lower board
- Guarded traces on lower board

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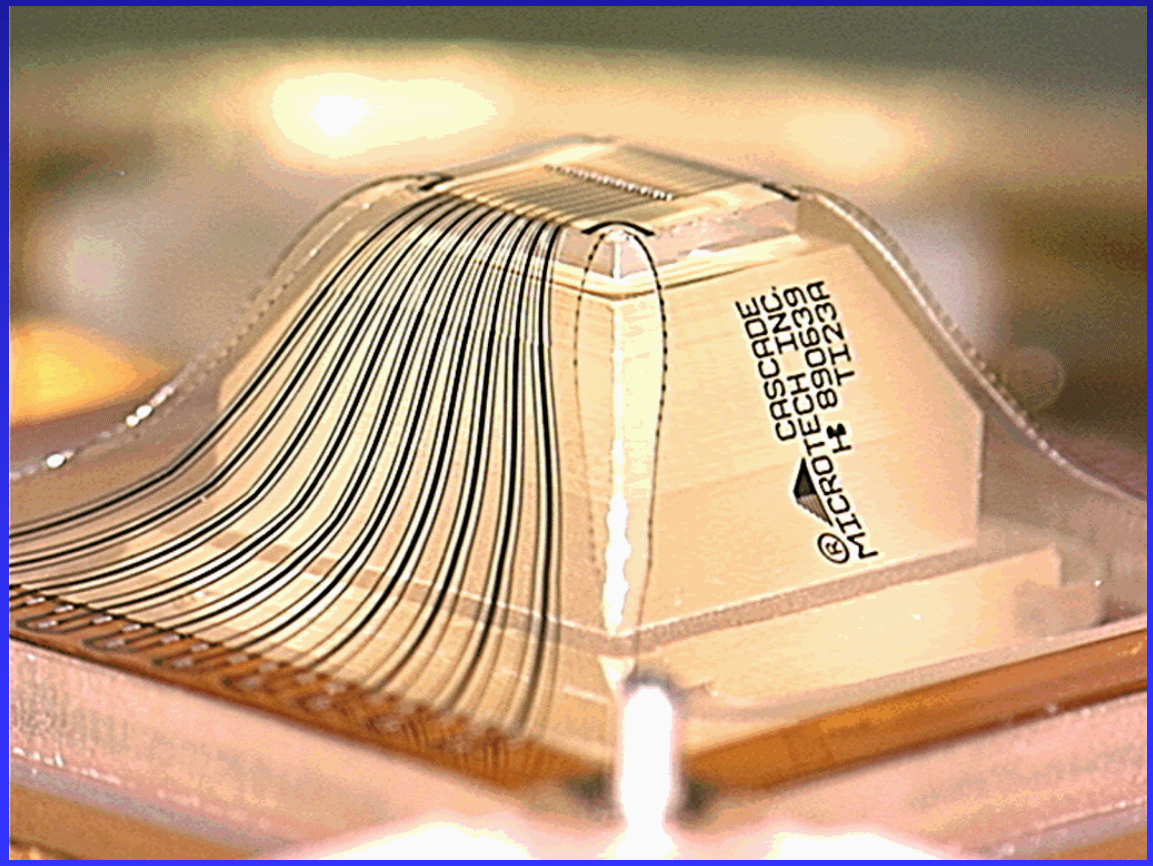
Pyramid Core for Parametric Test

- Guarded circuit board interface
- Guarded traces to probe tips



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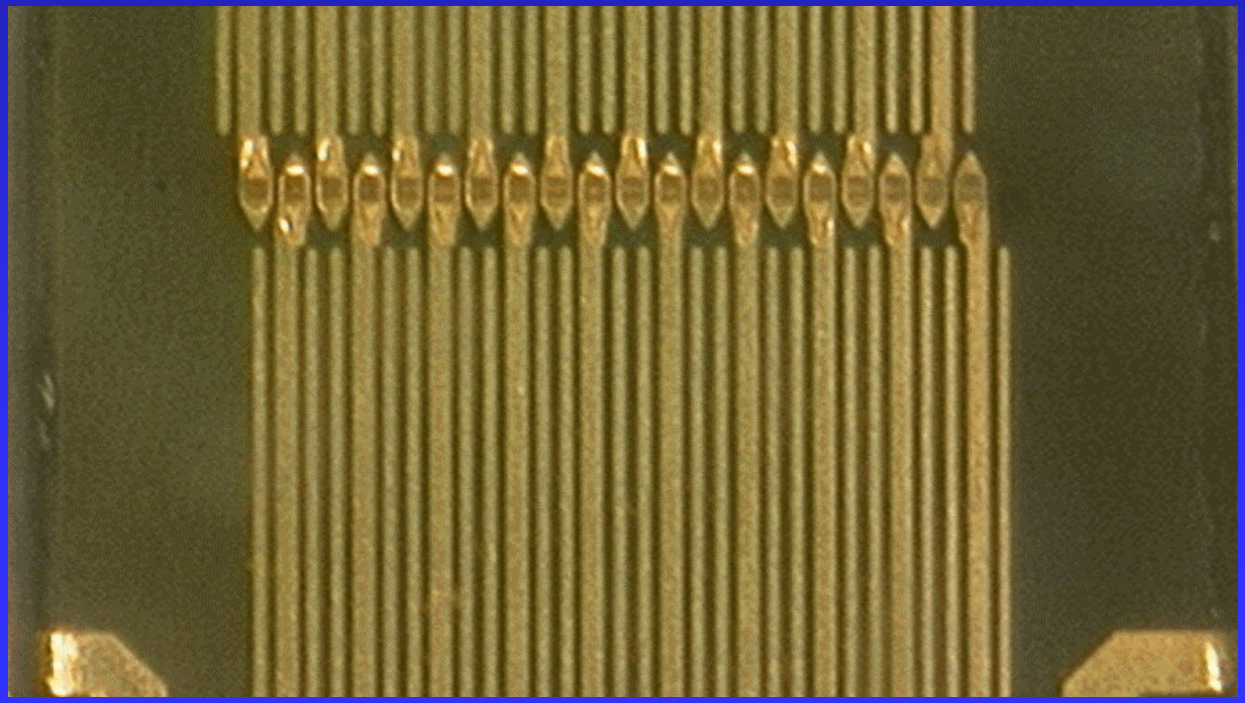
Pyramid Card Looking Down Through Core

- Linear layout typical of scribe line PCMs
- Guarded traces to probe tips (100 um pitch)
- Staggered routing for fine guard pitch



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Link to Keithley Electrical Performance Report

- Please see Bill Knauer's presentation Knauer_SWTW2002.ppt for his original slides in Keithley format

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Electrical Characterization Of Pyramid Probe Card

- Leakage / Settling Time Measurements
- Noise and Offset Measurements
- Capacitance Measurements

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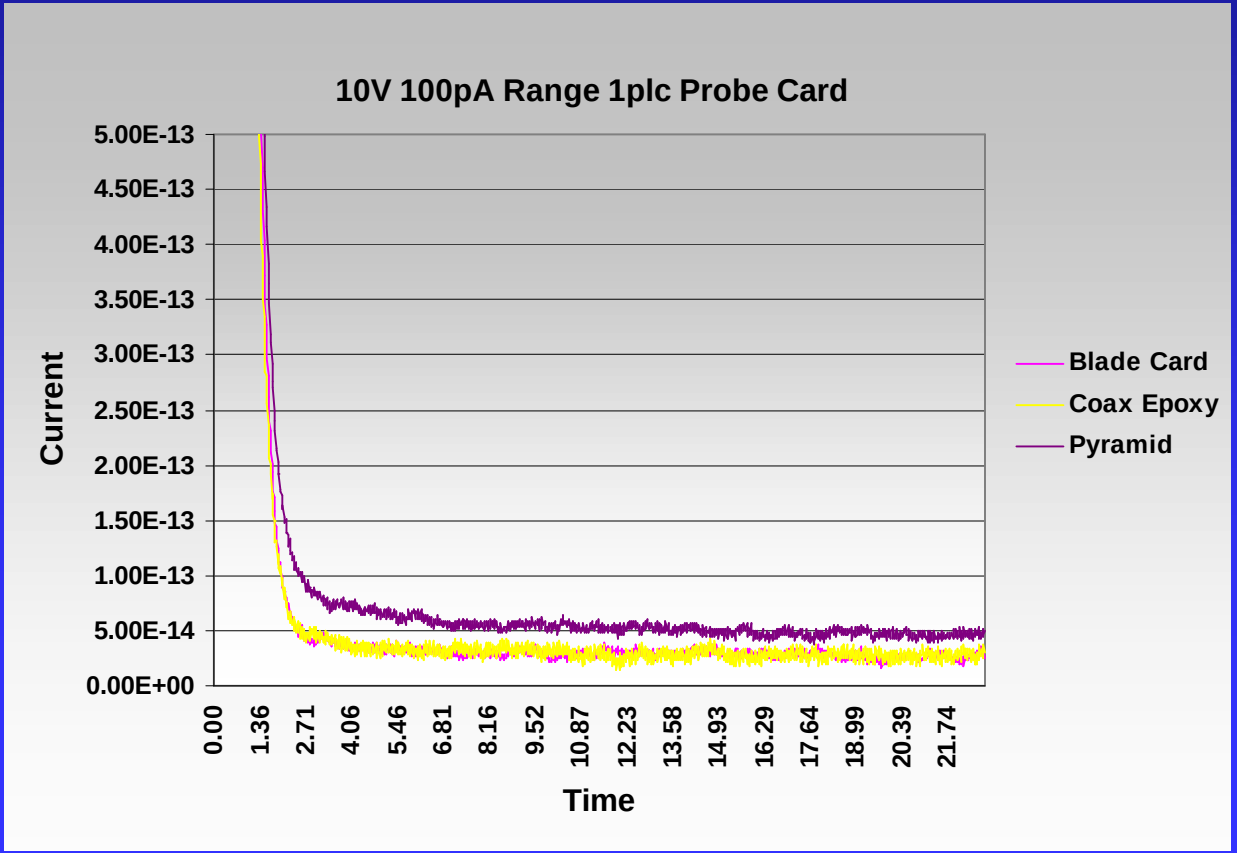
Leakage / Settling Comparison

- Initial settling curve is the same as the blade and coax epoxy cards.
- Longer final settling due to slightly higher leakage and higher dielectric absorption.



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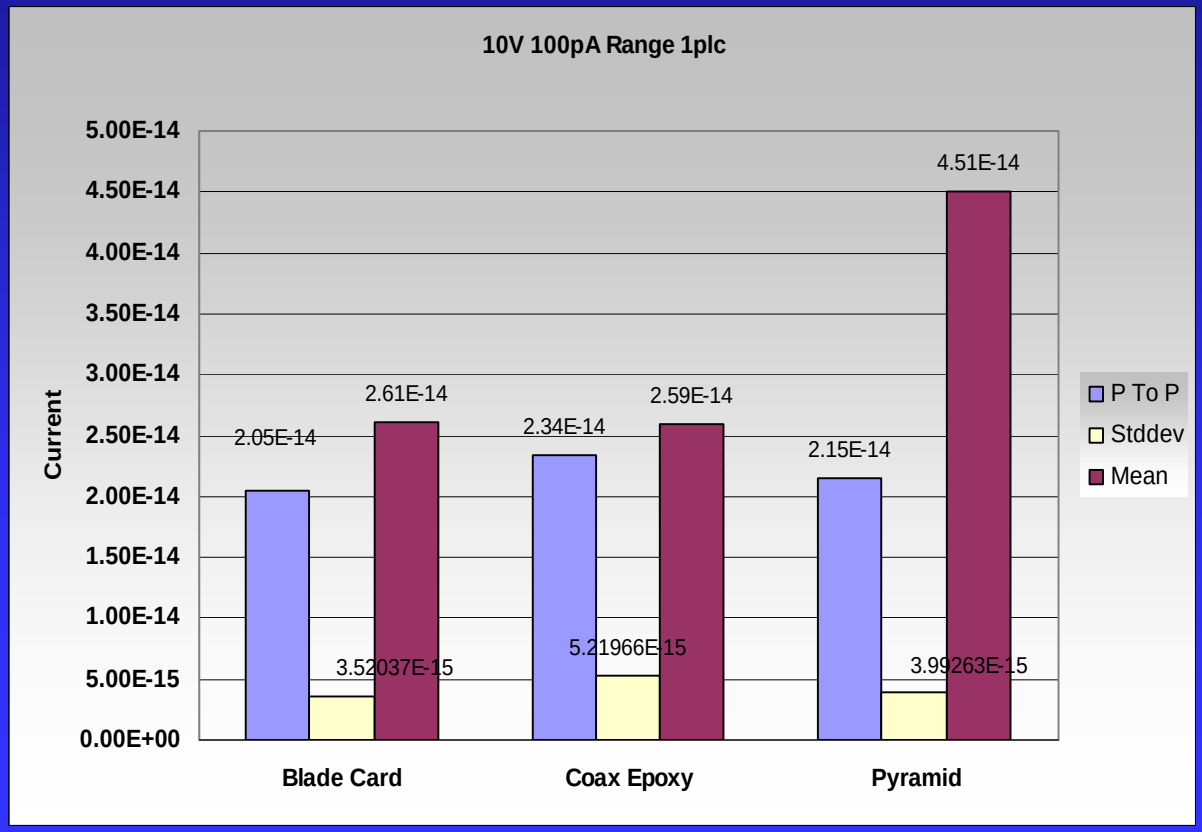
Noise and Offset Comparison

- Peak to peak noise and standard deviation of noise is same as other cards.
- Mean is slightly higher because of leakage.



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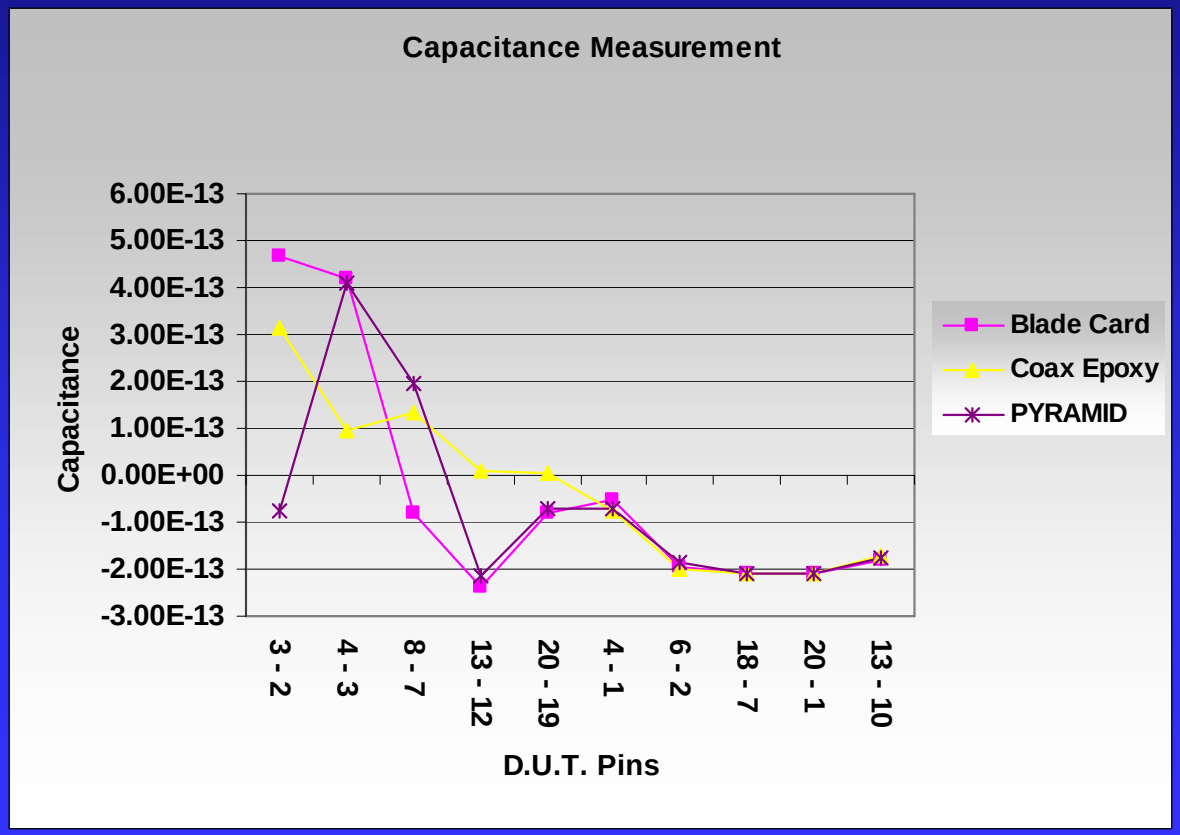
Capacitance Comparison

- Capacitance is the same as other probe cards



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Characterization Conclusions

- Pyramid probe card design shows excellent performance for low current measurements down to 100fA as compared to other low current technologies.
- Increased settling related to dielectric absorption and not capacitance.
- Probes up offset measurements will allow card to perform as well as other low current technologies.

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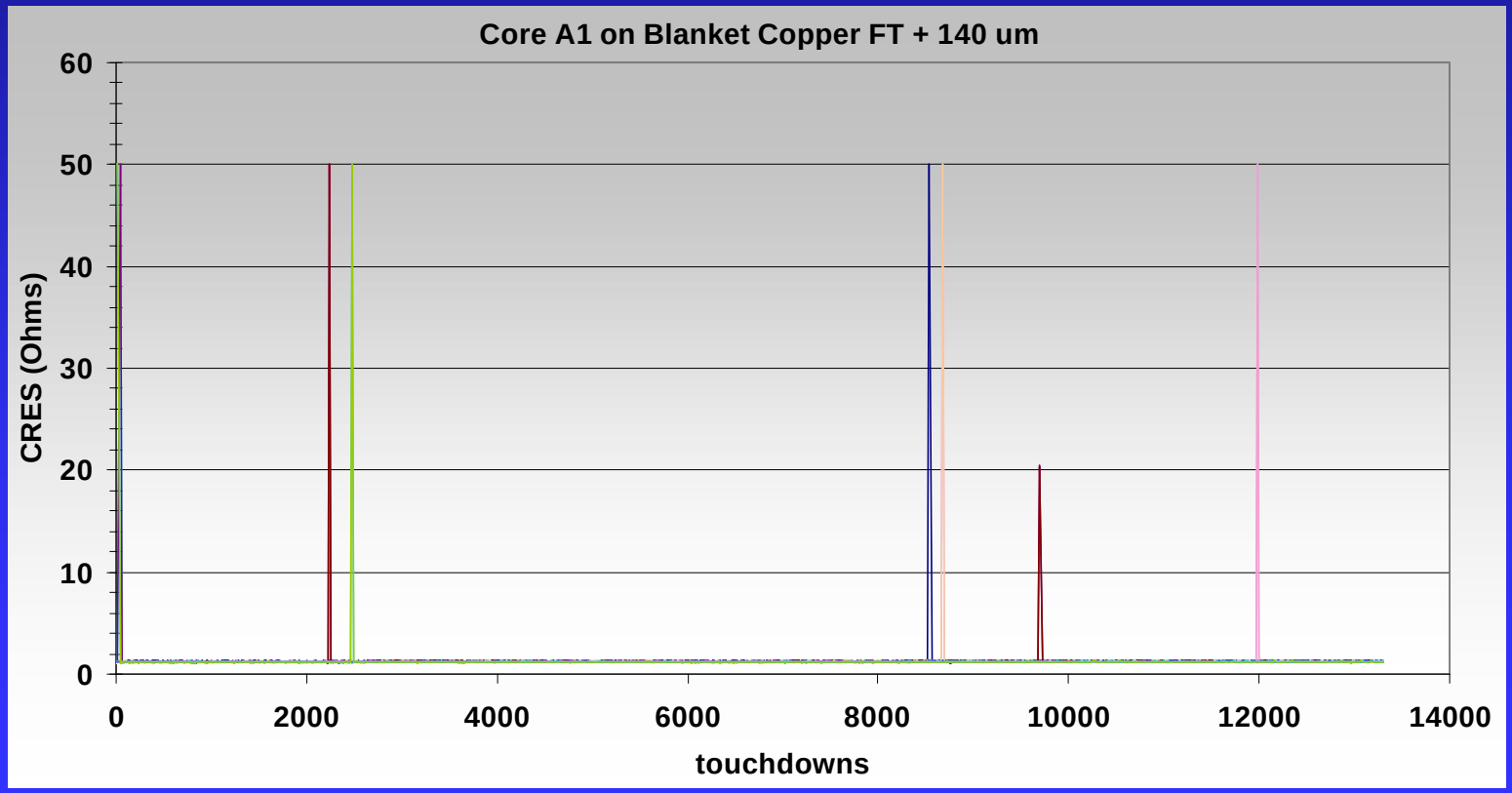
Contact Resistance Test Conditions

- Loop resistance between each of 20 adjacent channels
- 13000 cycles, measure every 20 cycles, no cleaning cycles
- 17 particle hits: class 10K environment (shown as 50 ohms)
- Room temperature



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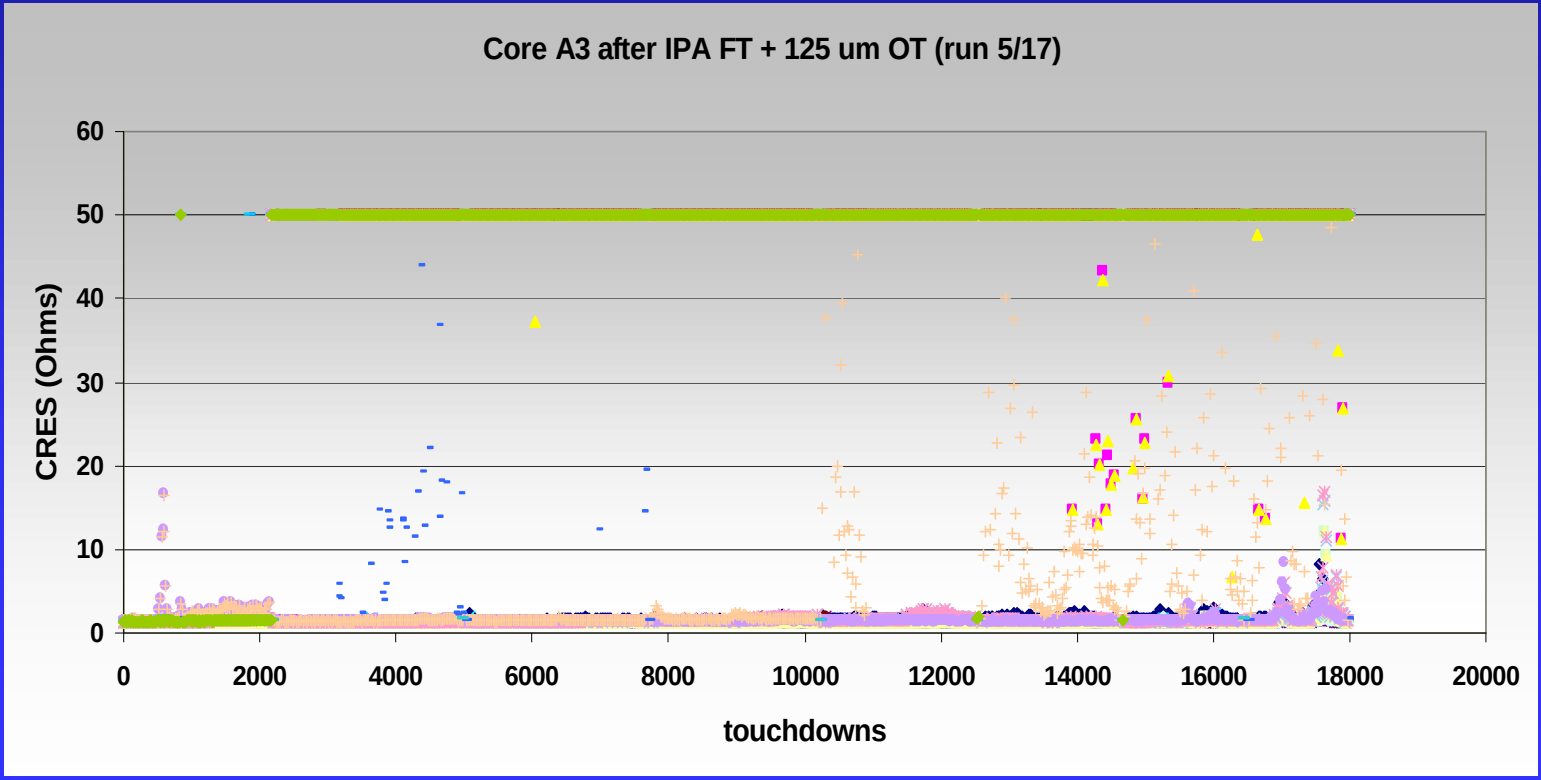
Cres with Low Overtravel on Oxidized Copper Wafer

- Relationship between overtravel, Cres, and copper oxidation time under investigation



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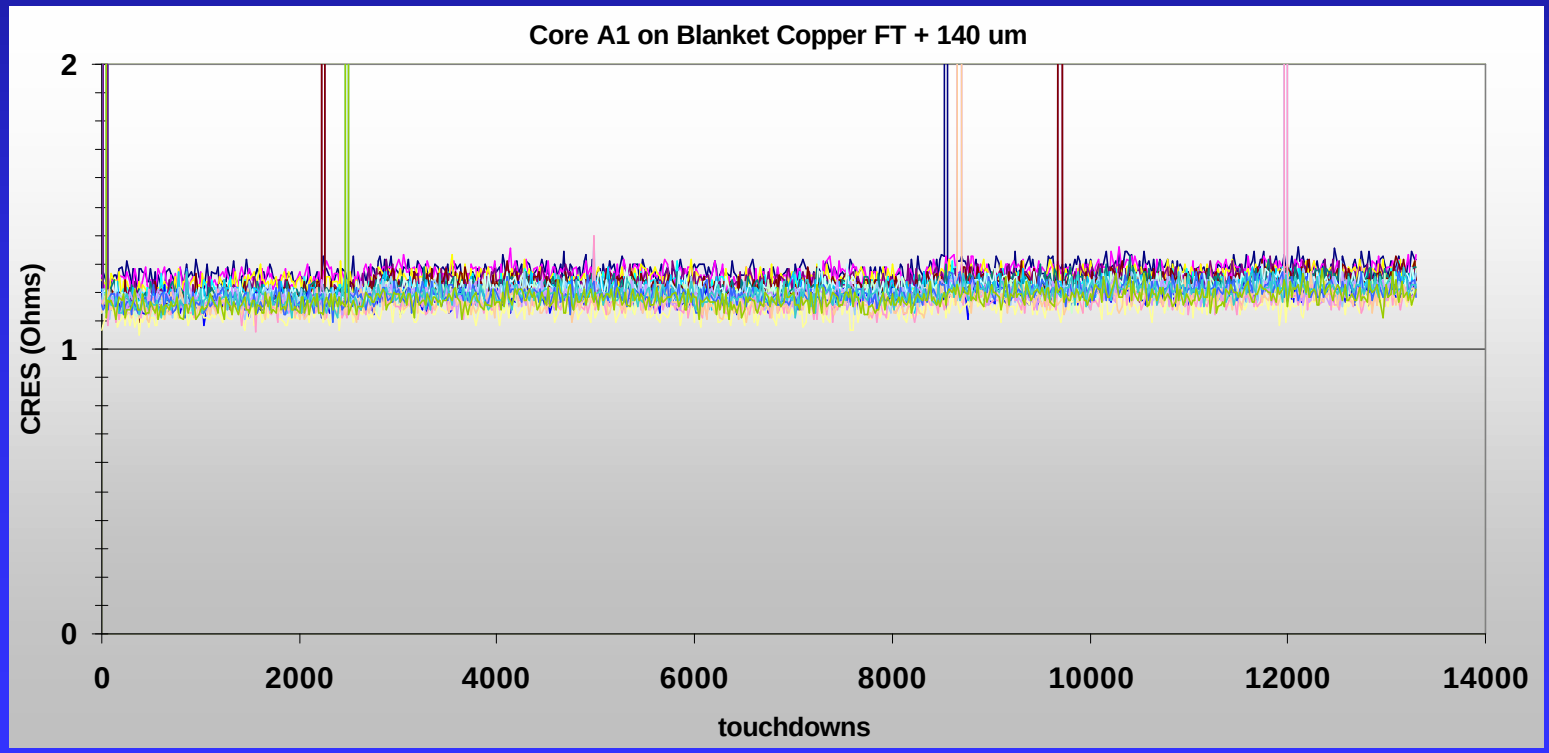
Contact Resistance Performance on clean Copper wafers

- Loop resistance: 1.14 to 1.27 ohms
- Cres average: 0.091 ohms
- Cres std dev: 0.032 ohms



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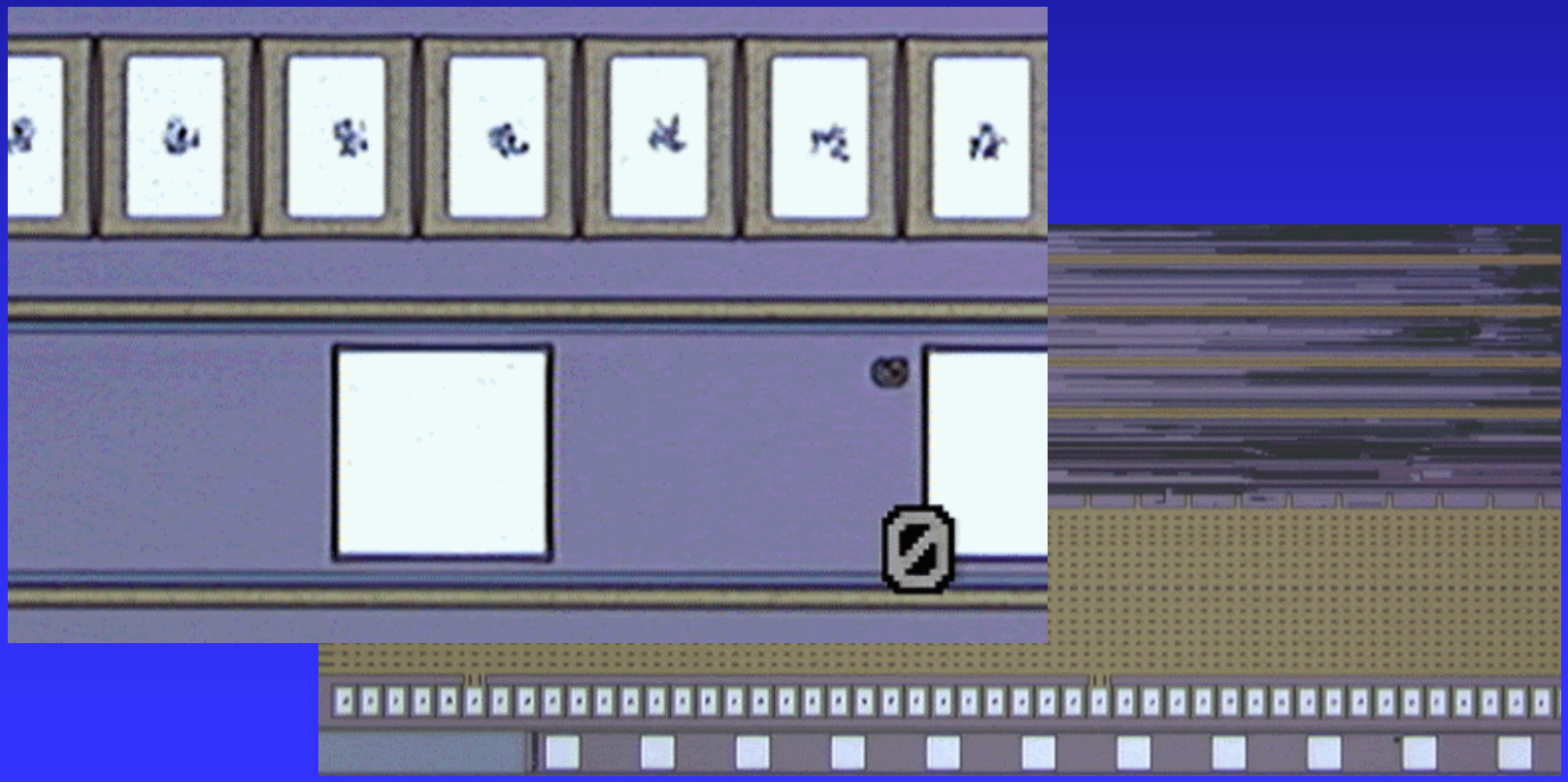
Probe Mark Budget

- Maximum mark size 15 x 20 um
- Positional accuracy +/- 5 um
- Mark budget 25 x 30 um
- Typical marks on 30 x 50 um pads



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Conclusion:

- Pyramid Probe Cards show excellent performance for low current measurements on Aluminum or Copper pads

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KGD Workshop Commercial:

Flip Chip KGD Workshop

June 24-26 Austin, Texas

IMAPS www.imapsflipchip.com

Pyramid Probe high volume solder ball probing results for Known-Good-Die