Speed bumps in Fast probing

> Lalit Kumar
> Janaki Vegiraju
> Bob Fenton
Index

> Introduction
> Bumping Processes - Overview
> Challenges in Bump Wafer Probing
> Proposed Solutions
> Summary and Conclusions
> References
Introduction

> Bumped wafers are becoming more and more common

> Fast probing – probing of very small die with relatively short test times – is a requirement today.
  > Faster testers (also BIST, DFT) – test time ≤ step time in some applications
  > Cost of test pressure
  > Die shrinks

> Both trends combining to generate a new set of prober features
Bumping Processes - Overview

> Evaporated Vs. Electroplated

> Evaporated bump technology has extendibility issues when bump pitch is decreased below 9 mil.

> Electroplated bump pitch is limited more by assembly and reliability considerations than by the formation of the bump.

> We have to probe all of them!
Bumps – a prober’s view
## Ball diameter and pitch design rules (WLP)

<table>
<thead>
<tr>
<th>Diameter</th>
<th>Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.03</td>
<td>0.05</td>
</tr>
<tr>
<td>0.023</td>
<td>0.039</td>
</tr>
<tr>
<td>0.02</td>
<td>0.031</td>
</tr>
<tr>
<td>0.018</td>
<td>0.029</td>
</tr>
<tr>
<td>0.016</td>
<td>0.025</td>
</tr>
<tr>
<td>0.012</td>
<td>0.0197</td>
</tr>
<tr>
<td>0.01</td>
<td>0.0157</td>
</tr>
<tr>
<td>0.008</td>
<td>0.0118</td>
</tr>
<tr>
<td>0.006</td>
<td>0.0078</td>
</tr>
</tbody>
</table>
# FCT Bump design guidelines

## Table 1. Peripheral Solder Bump Design Guidelines.

<table>
<thead>
<tr>
<th>Peripheral Pitch</th>
<th>254 (10mil)</th>
<th>204 (8mil)</th>
<th>152 (6mil)</th>
<th>127 (5mil)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UBM Mask Name</td>
<td>Cap6</td>
<td>Cap4</td>
<td>Cap3.5</td>
<td>Cap3</td>
</tr>
<tr>
<td>UBM Diameter</td>
<td>152</td>
<td>102</td>
<td>90</td>
<td>75</td>
</tr>
<tr>
<td>Max Passivation Opening Diameter</td>
<td>132</td>
<td>82</td>
<td>70</td>
<td>55</td>
</tr>
<tr>
<td>Minimum Final Metal Size</td>
<td>164</td>
<td>114</td>
<td>102</td>
<td>87</td>
</tr>
<tr>
<td>Approved for Sn63/Pb37</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>Approved for Pb90/Sn10</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
</tr>
<tr>
<td>Bump Height Mean</td>
<td>130</td>
<td>100</td>
<td>87</td>
<td>75</td>
</tr>
</tbody>
</table>

All dimensions are microns unless noted.

## Table 2. Solder Bump Array Design Guidelines.

<table>
<thead>
<tr>
<th>Array Pitch</th>
<th>254 (10mil)</th>
<th>227 (9mil)</th>
<th>204 (8mil)</th>
<th>177 (7mil)</th>
<th>160 (6.3mil)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UBM Mask Name</td>
<td>Cap4</td>
<td>Cap3.5</td>
<td>Cap3.2</td>
<td>Cap3.2</td>
<td>Cap3</td>
</tr>
<tr>
<td>UBM Diameter</td>
<td>102</td>
<td>90</td>
<td>80</td>
<td>80</td>
<td>77</td>
</tr>
<tr>
<td>Max Passivation Opening Diameter</td>
<td>82</td>
<td>70</td>
<td>60</td>
<td>57</td>
<td></td>
</tr>
<tr>
<td>Minimum Final Metal Size</td>
<td>114</td>
<td>102</td>
<td>92</td>
<td>92</td>
<td>89</td>
</tr>
<tr>
<td>Approved for Sn63/Pb37</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>Approved for Pb90/Sn10</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
</tr>
<tr>
<td>Bump Height Mean</td>
<td>105</td>
<td>100</td>
<td>90</td>
<td>78</td>
<td>75</td>
</tr>
</tbody>
</table>

All dimensions are microns unless noted.
Bump characteristics summary

> Bumps in wide use are .004” to .025” tall
  > Ball tolerance can be as much as ±20%
  > Balls have a wider location tolerance than bond pads
> Bumped wafers typically have areas that do not contain bumps
> Some wafers have no bump free areas
Useful characterizations for probing

> Flip chips can be from 30% to 50% smaller than perimeter attach counterparts
Challenges in Bump Wafer Probing

> Profile
> Alignment
> Z height detection/probe height measurement
> Automated probe to pad alignment (APTPA)
> High throughput – test cell could be idle during profile and alignment
> Needle cleaning – different needs than bond pads (not covered in this paper)
> “Follow map” probing from inspection equipment (not covered in this paper)
Probe requirements

> Prealignment
  > Must determine center of the wafer relative to chuck center, with bumps as large as .034”.
  > Must find wafer edges for bumped wafers with bump arrays all the way to the edges.
  > Must not “lose” die in the case of very small die and inaccurate edge detection.
Probe requirements

> Profiling/ Z alignment

> The profiler must be able to detect the wafer surface between bumps, or bump arrays as high as .034”.

> Determine the nominal height of the tops of the bumps, which is probing height.
Prober requirements

> APTPA

> Based on the size and tolerance of the balls, the ball targets could vary. For example, a .020” nominal ball diameter could have balls from .014” to .026”. This range is based on various ball manufacturers specifications and tolerances. In practice, a given wafer would likely exhibit more uniformity.
Prober requirements – high throughput

> Alignment (and potentially profiling) time detracts from overall test cell throughput.
> Tester is “down” during alignment – reducing tester utilization
> Must be accurate, but fast!
Proposed Solutions

> Finding the Wafer Edge – critical!
  > Scan from outside of the wafer edge at a safe height (nominal wafer thickness + bump height + tolerance) towards the wafer center until the edge is detected.
## Useful characterizations for probing

<table>
<thead>
<tr>
<th>Category</th>
<th>Description</th>
<th>Profile</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Category 1</strong></td>
<td>Peripheral bumps with clear area, bumps are .005” or smaller</td>
<td>surface between bumps</td>
</tr>
<tr>
<td><strong>Category 2</strong></td>
<td>Peripheral bumps with clear area, bumps are up to .035”</td>
<td>surface between bumps</td>
</tr>
<tr>
<td><strong>Category 3</strong></td>
<td>Die are area array and fully populated. Clear areas exist on wafer edge and OCR</td>
<td>clear areas on the wafer edge or OCR</td>
</tr>
<tr>
<td><strong>Category 4</strong></td>
<td>Wafer is fully populated with bumps. No clear areas exist</td>
<td>bumped area, fit bump by application or offset</td>
</tr>
</tbody>
</table>
Solutions

> Categories 1 through 3
> Find the wafer surface and add the bump height
> Finding the wafer surface height
> Train several bump free sites.
> Find the wafer surface height at those sites.
> Add bump height to the wafer surface height, which becomes probing height.
> Is this a valid approach?
Finding the wafer surface

Thickness .29.5 mils
Solutions

> Category 4

> Profile the aggregate surface

> Determine profiler spot size versus ball area

> Profiler measurement will be an average of these areas

> Add in offset to product file to obtain probing “Z” height
Category 4 data

Bump Height 33.5 mils
Bump Height 40.5 mils
Bump Height 39 mils
Bump Height 39 mils
Summary and conclusions

> Bump probing is becoming more of a requirement
> New prober features are needed to process bumped wafer
References


> Wafer Level Packaging Addresses Chip-to-Module Interconnections; Paul A. Kohl and Kevin Martin; Georgia Institute of Technology, Atlanta; April 2001.

> C4 Makes Way for Electroplated Bumps; David Clegg et. All; Motorola Semiconductor Products Sector, Austin, Texas; March 2001.

> Classical Electrodynamics (Second Edition), J.D. Jackson