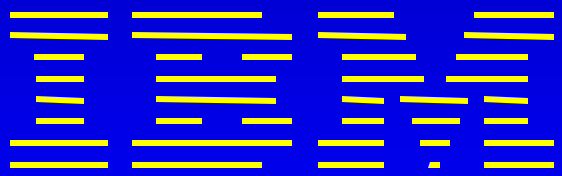
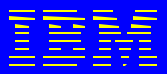
Area Array Cobra Probe Card With 5 GHz. Bandwidth

Raphael Robertazzi

IBM Research

6/12/02





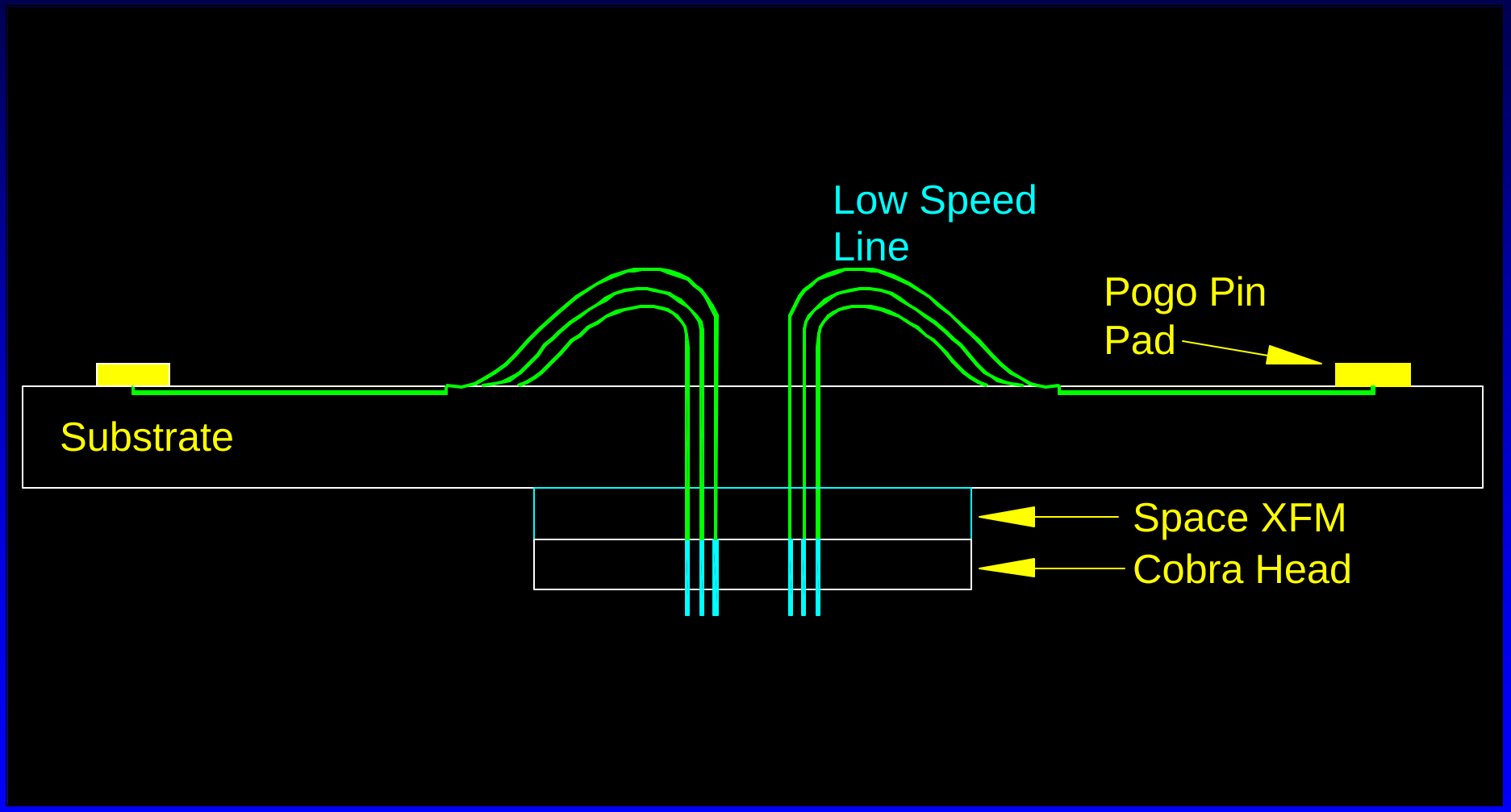
Outline

- Motivation: *Test High Speed Area Array ICs In The Development Stage, At Wafer Level.*
  - Improve The Bandwidth Of Cobra Probe Cards For At Speed (10Gb/s) Test.
  - Performance Equal To Or Better Than Membrane Probes, Extension To Higher Frequencies.
- New Hand Wired Space Transformer Concept / Implementation.
- Experimental Results.
  - Rise Time / Bandwidth Measurements.
  - 10 Gb/s Serializer/Deserializer Wafer Level BERT Test.
- Conclusions.

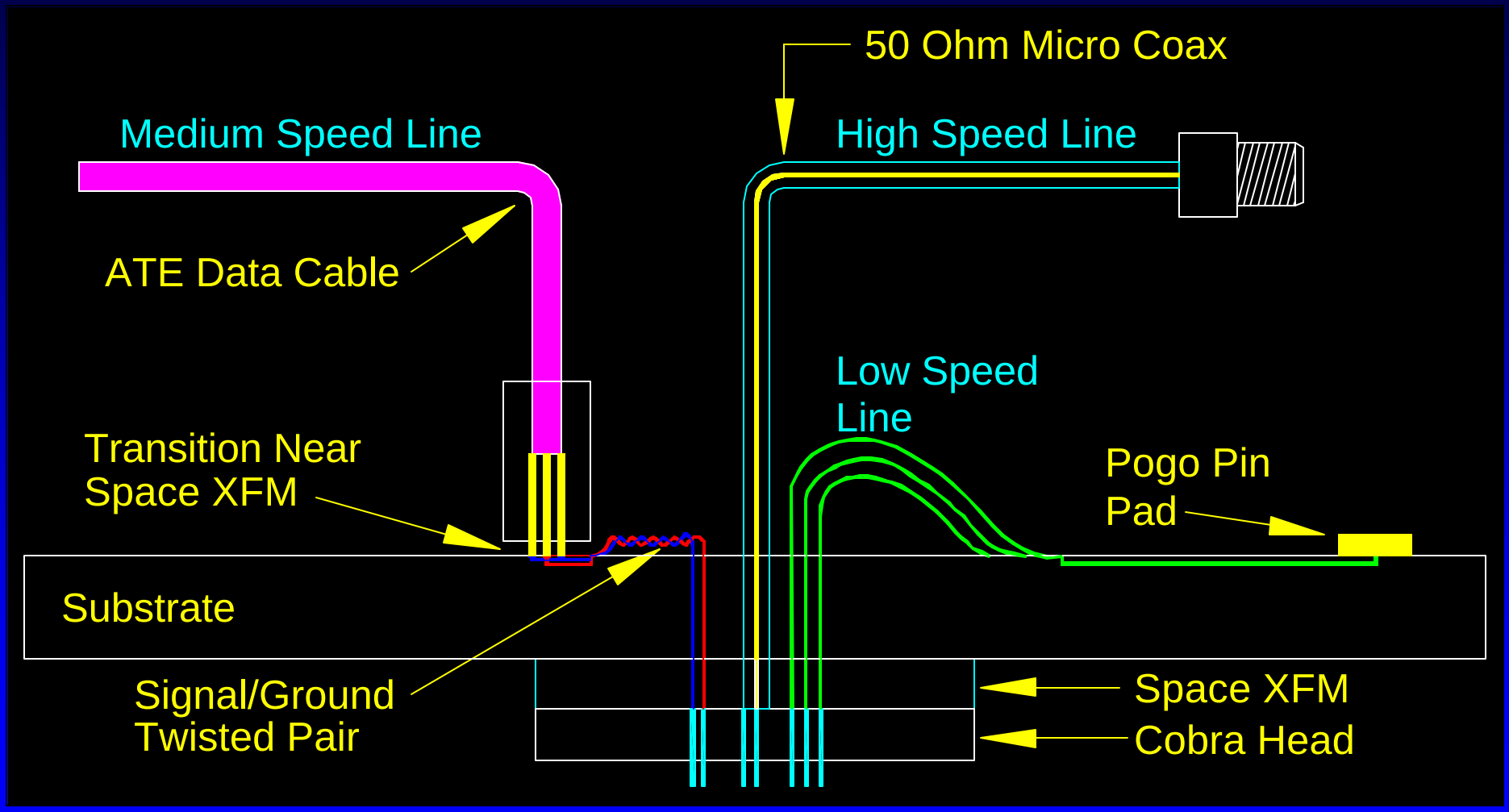
Motivation

- Wafer Level, Developmental Testing Of High Pin Count Communications ICs.
  - Connection To C4 Arrays (Cobra Probe).
  - Large Numbers (~100) Of Medium Speed (0.5-1 Gb/S) Data Lines.
  - Microwave (10 Gb/S) Data Rates On Selected Lines.
  - Complex, Multiple Power Domains.
  - Path To 40 Gb/s Test.

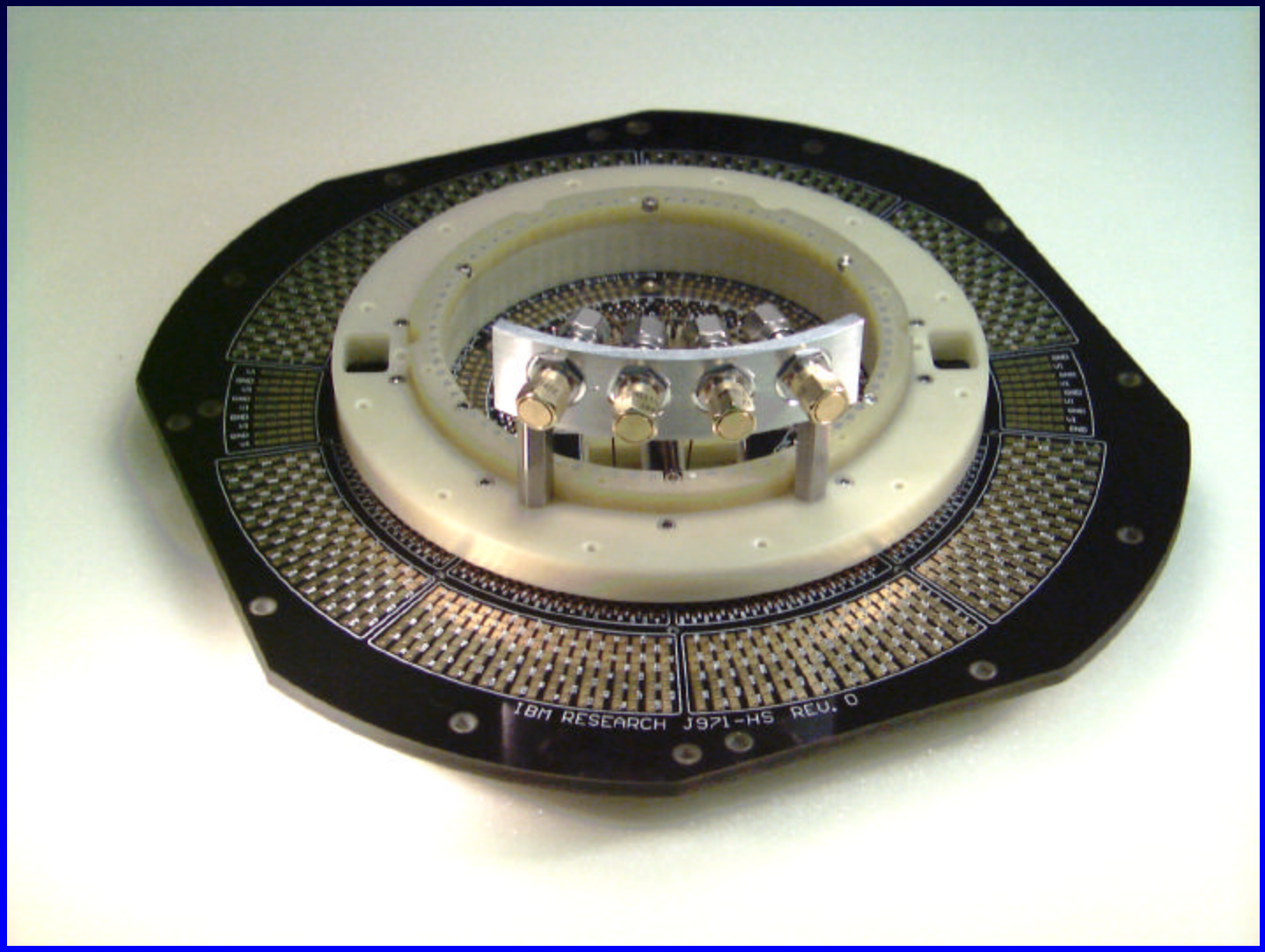
Conventional Cobra Probe Card



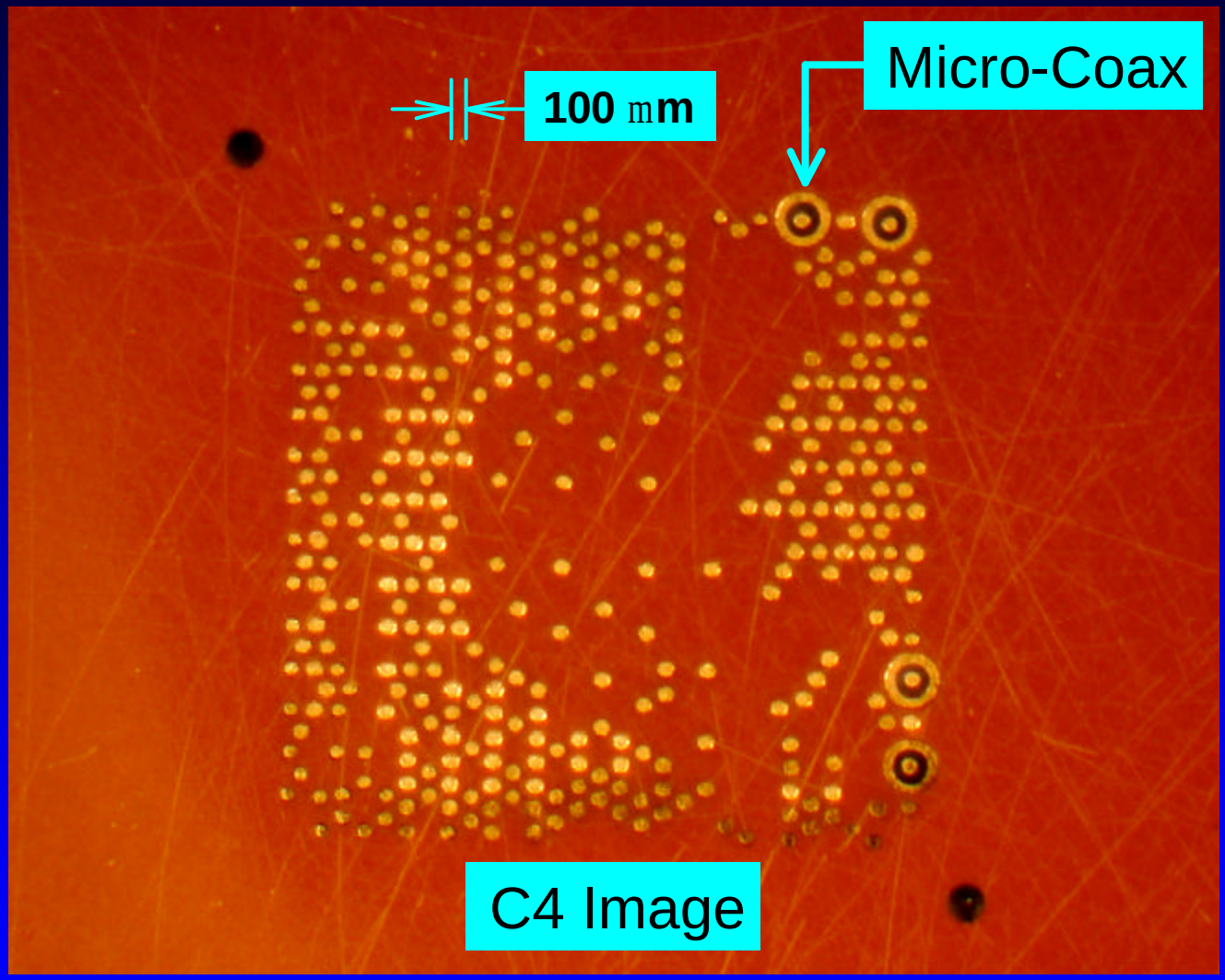
High Performance Cobra Probe Card



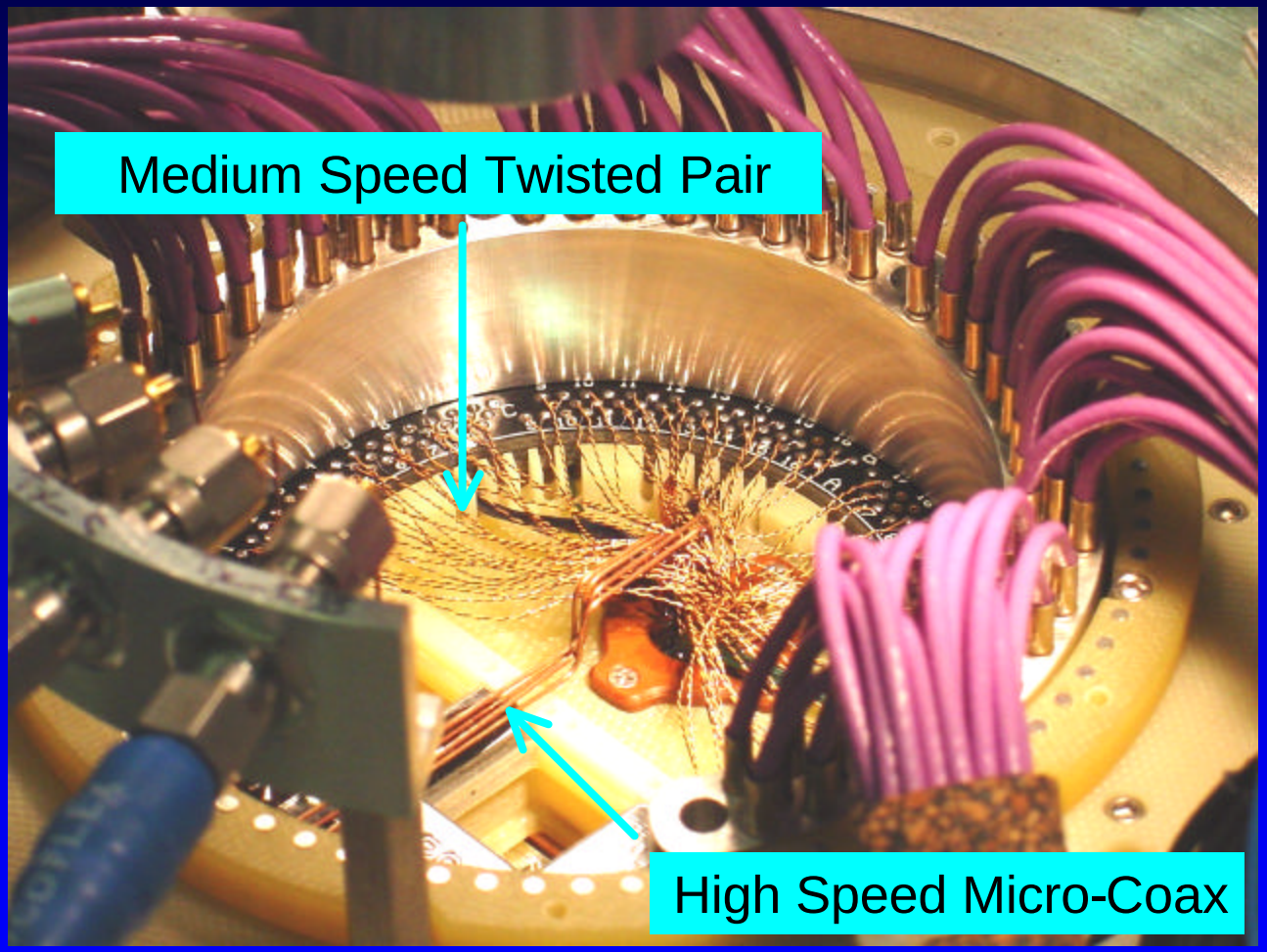
Probe Card Photo



Space Transformer



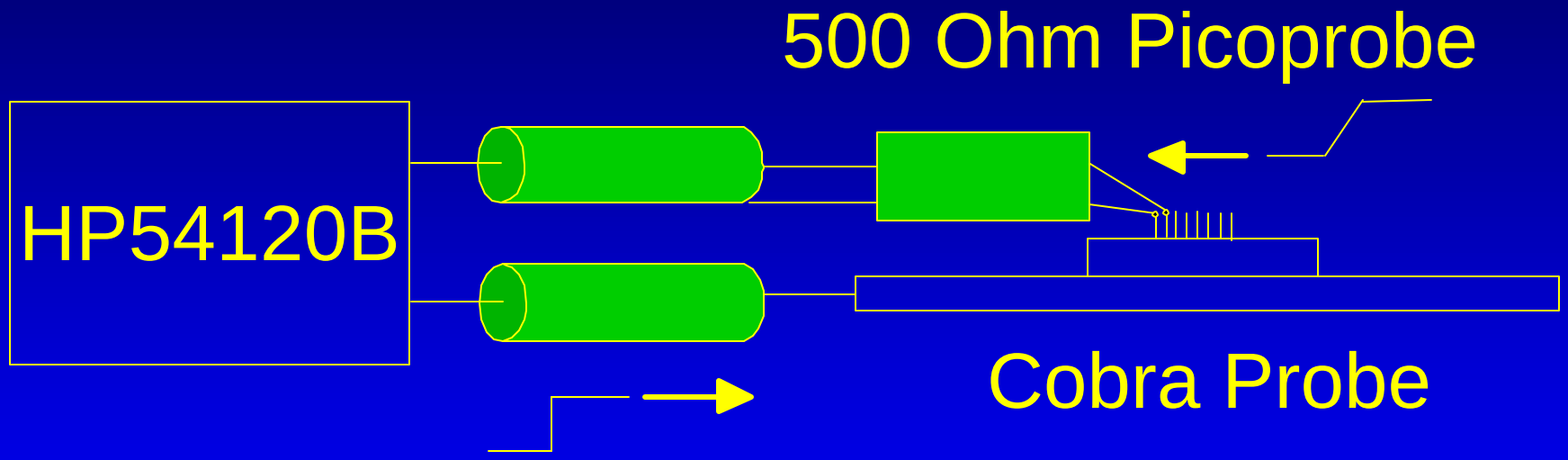
Probe Card On HP83K Test System



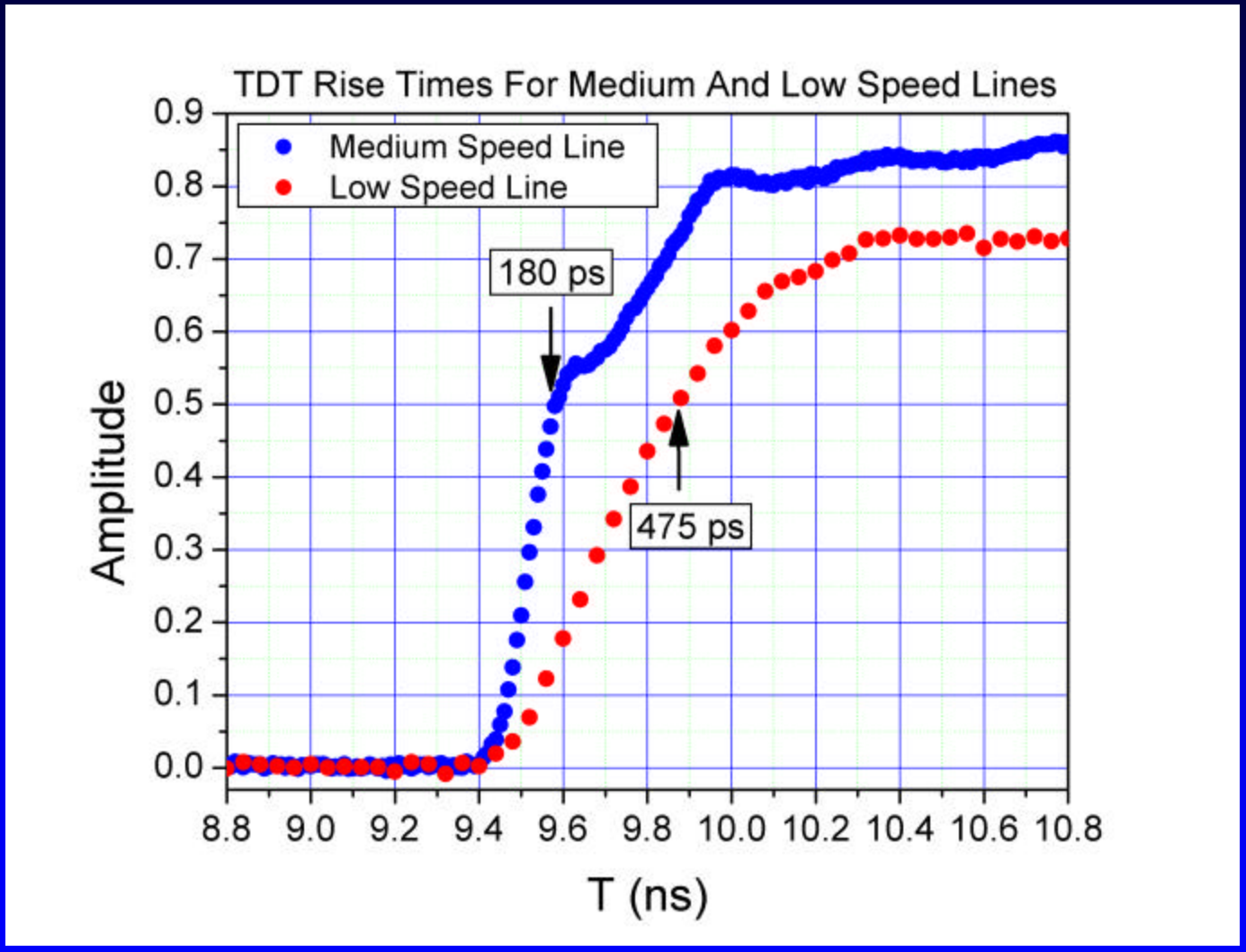
Probe Card Features

- Space Transformer Manufacturable In 4-6 Weeks.
- Addition Of Medium Speed Differential Lines Capable Of 3-4 X Bandwidth Of Standard Space Transformer Lines (92 Ports).
- Addition of High Speed Lines Capable Of 20 X Bandwidth of Standard Space Transformer (4 Ports).
- Other Improvements Relevant to Microprocessor Test And Decreased Probe Card Manufacturing Time.

TDT Characterization



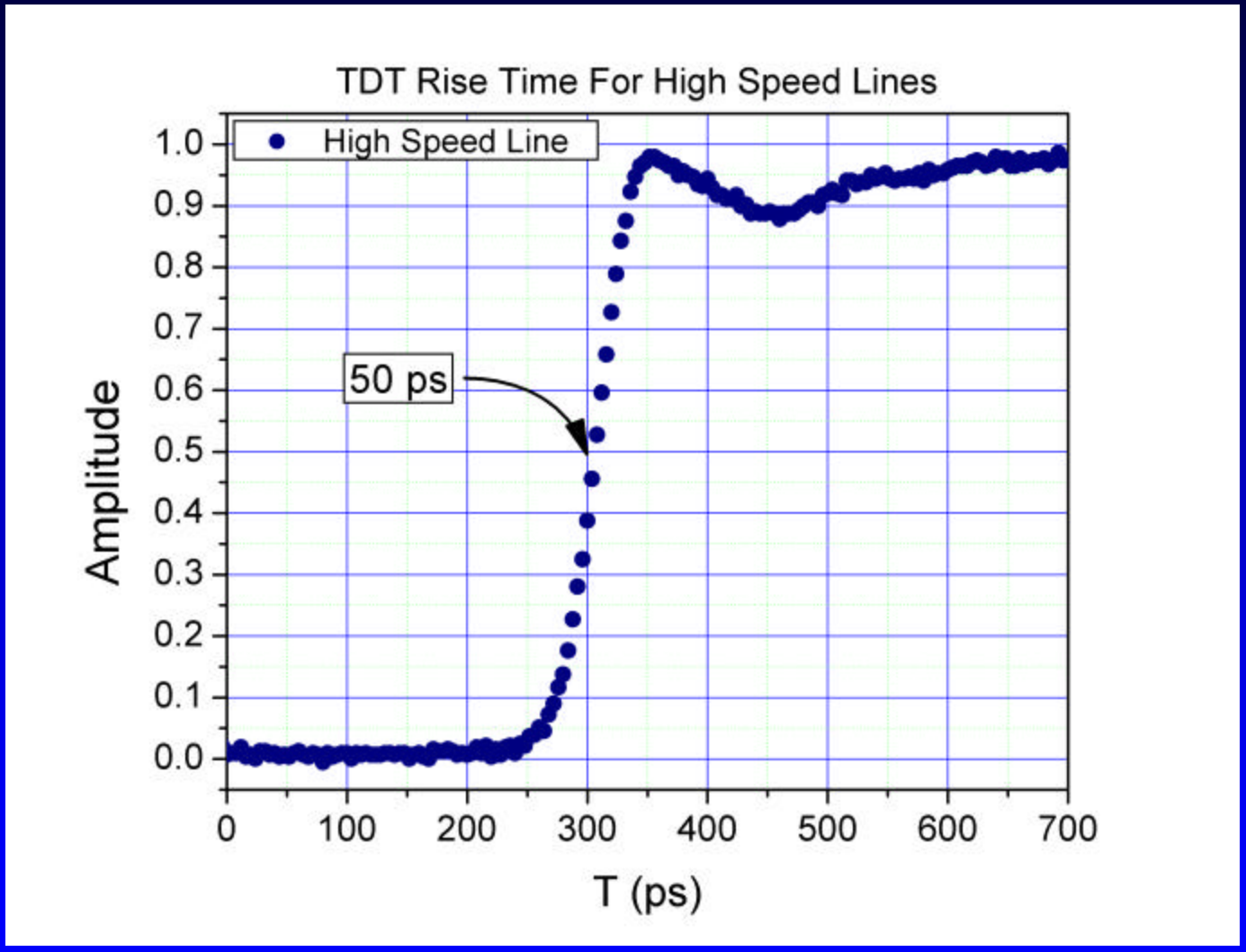
TDT For Medium And Low Speed Lines



Low and Med Speed Line Rise Time Comparison

	$\tau_{20/80}$ (ps)	$\tau_{10/90}$ (ps)
Low	980	2160
Med	355	530

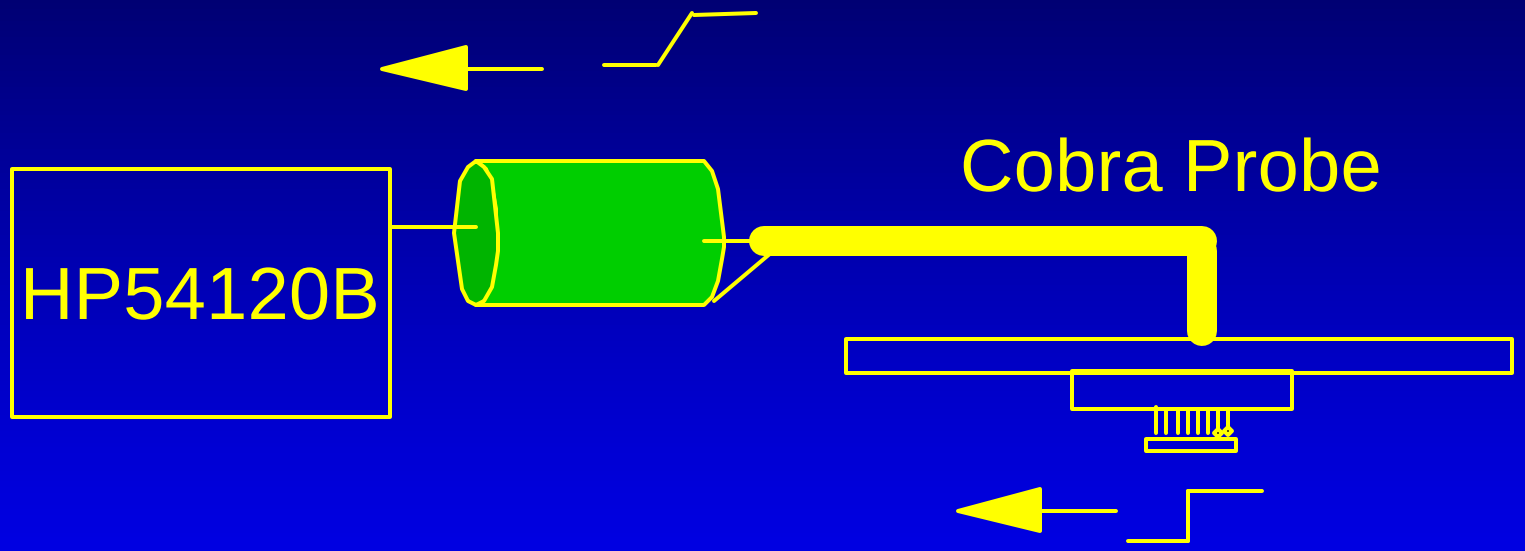
TDT For High Speed Lines



High Speed Line Rise Time

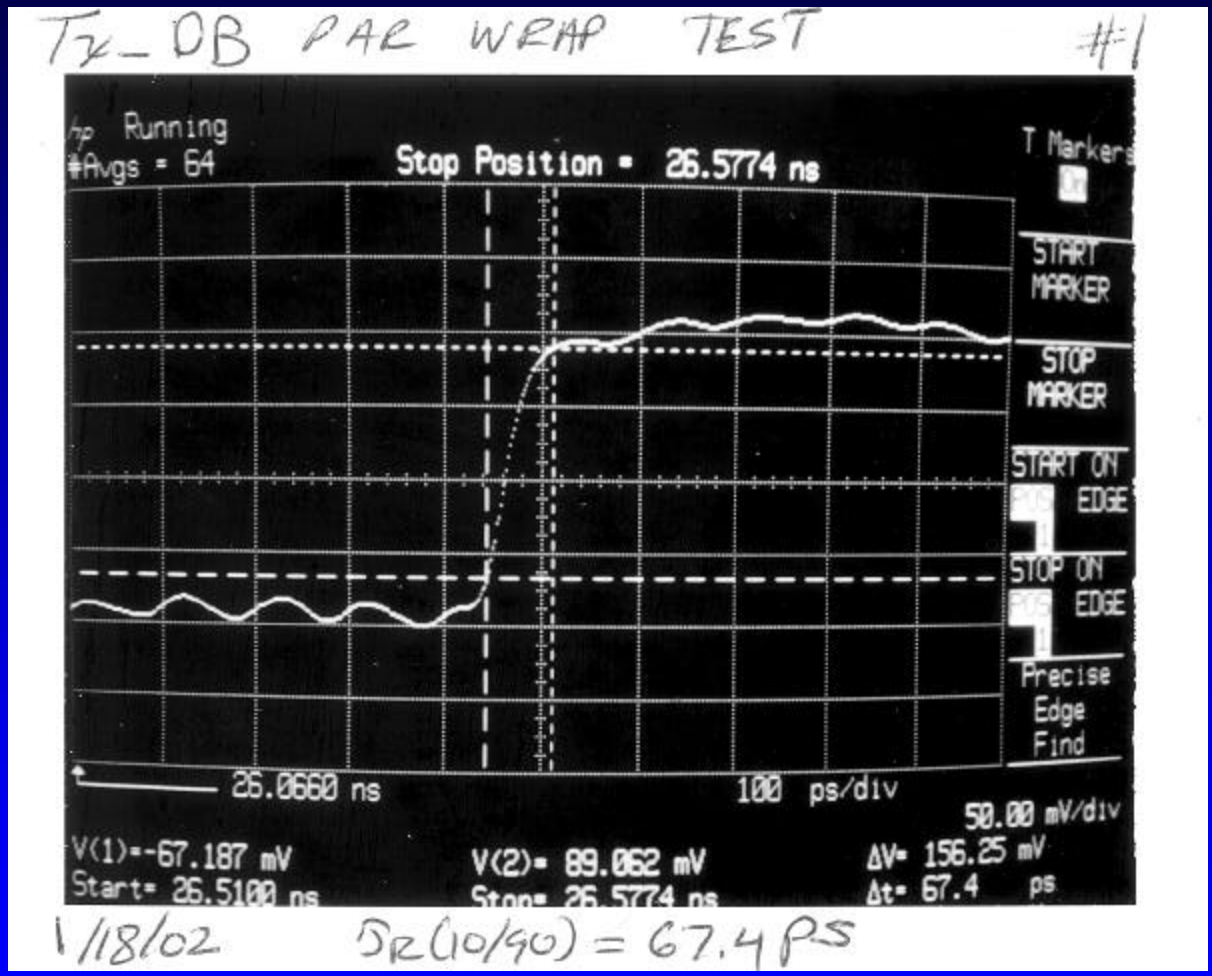
$\tau_{20/80}$ (ps)	$\tau_{10/90}$ (ps)
40	64

SerDes Output Experiment

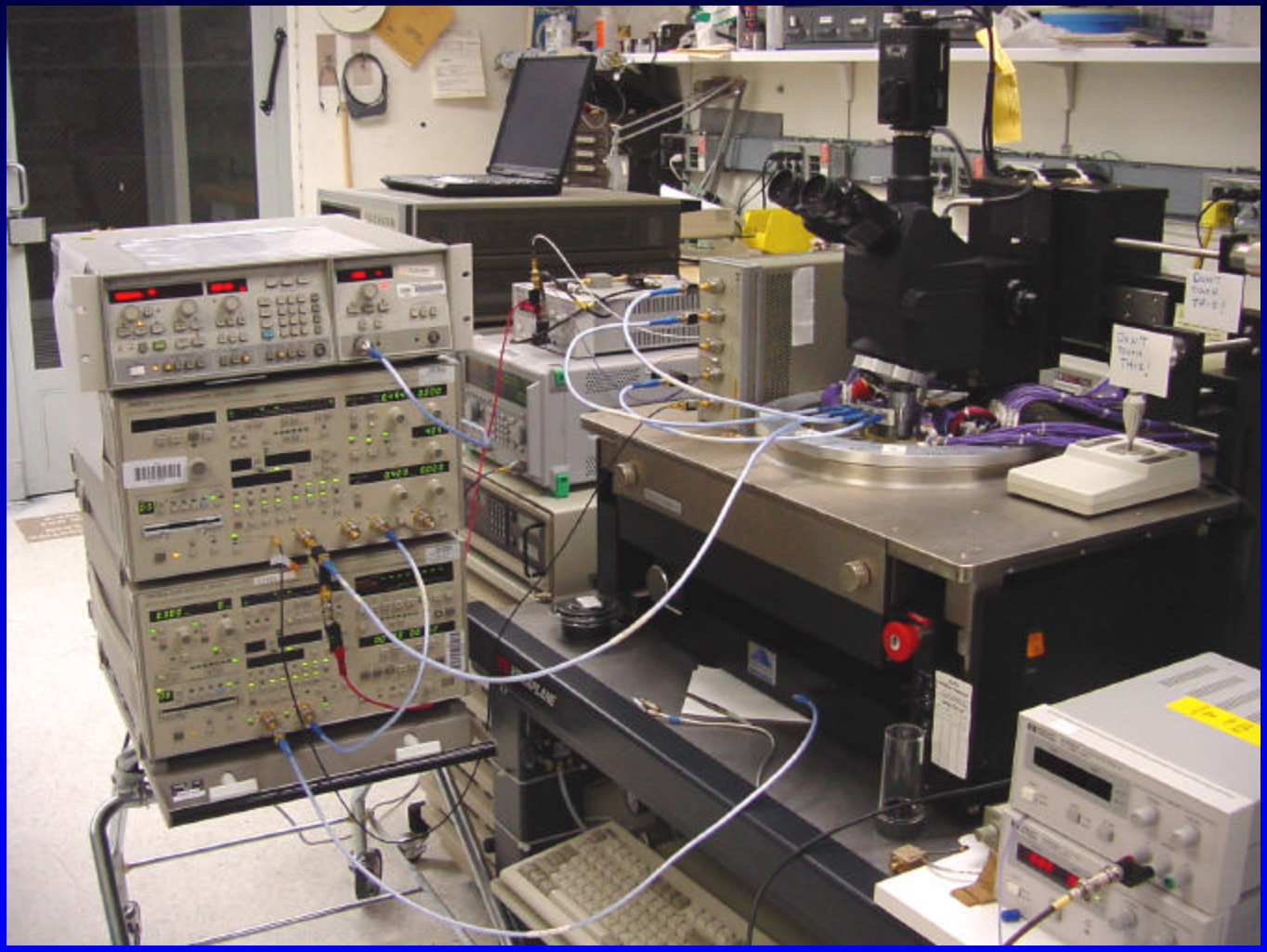


$\tau_r < 20ps$

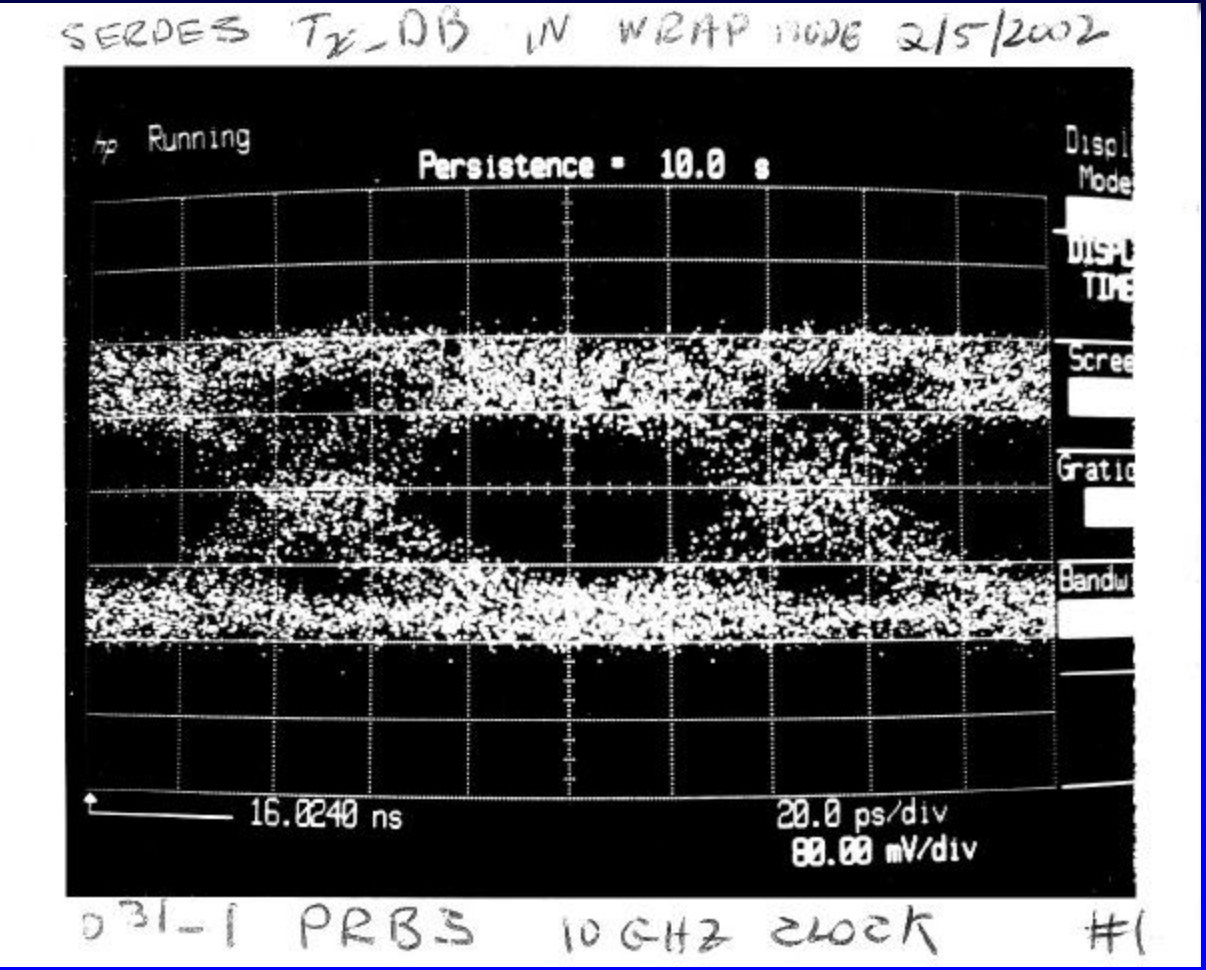
SerDes Output Data



SerDes BERT Experiment

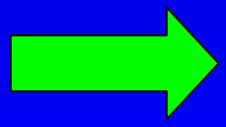


10 Gb/s Eye Diagram



10 Gb/s BERT Results At Wafer Level

Pattern	Comment
$2^7 - 1 \rightarrow 2^{23} - 1$	Error Free Over 30 Min. Experiment
$2^{31} - 1$	Error Rate* $= 1.3 \times 10^{-8}$

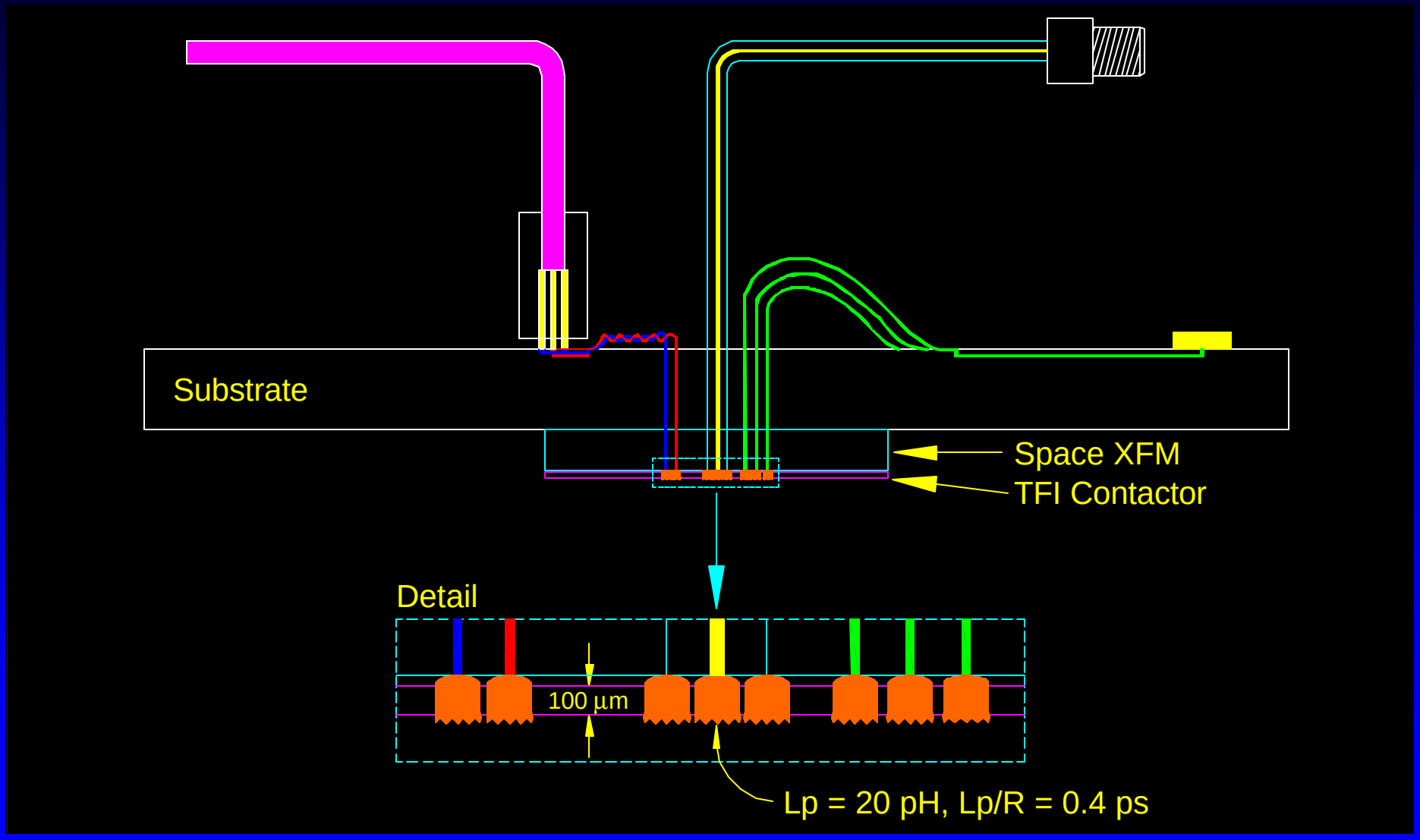


* Repairing R_x Ground Should Allow Long Pattern To Run Error Free

Extending Bandwidth

- Bandwidth Of Current Design Limited By Cobra Head.
  - Rise Time Of High Speed Lines Determined By L/R Time Of Head.
- Paths to Higher Frequencies:
  - Redesign Head For 50 Ohm Path From Coax To Chip.
  - Reduce Distance Between Coax And Chip.

TFI Contactor Reduces L/R Time



Conclusion

- Demonstration Of A New Cobra Probe Card With Increased Bandwidth:
  - 20X Bandwidth Improvement Over Conventional Cobra Probe Card (Micro Coax).
  - 3-4X Bandwidth Improvement Over Conventional Cobra Probe Card (Twisted Pair And Direct Cable To Card Connection).
- High Speed Line Bandwidth Limitation Gated By Cobra Head.

  Paths To Higher Frequencies:
  - Engineering 50 Ohm Cobra Head.
  - Using TFI Contactor.
- New Probe Card Can Be Constructed In 4-6 Weeks.