Introduction to Wafer Level Burn-In

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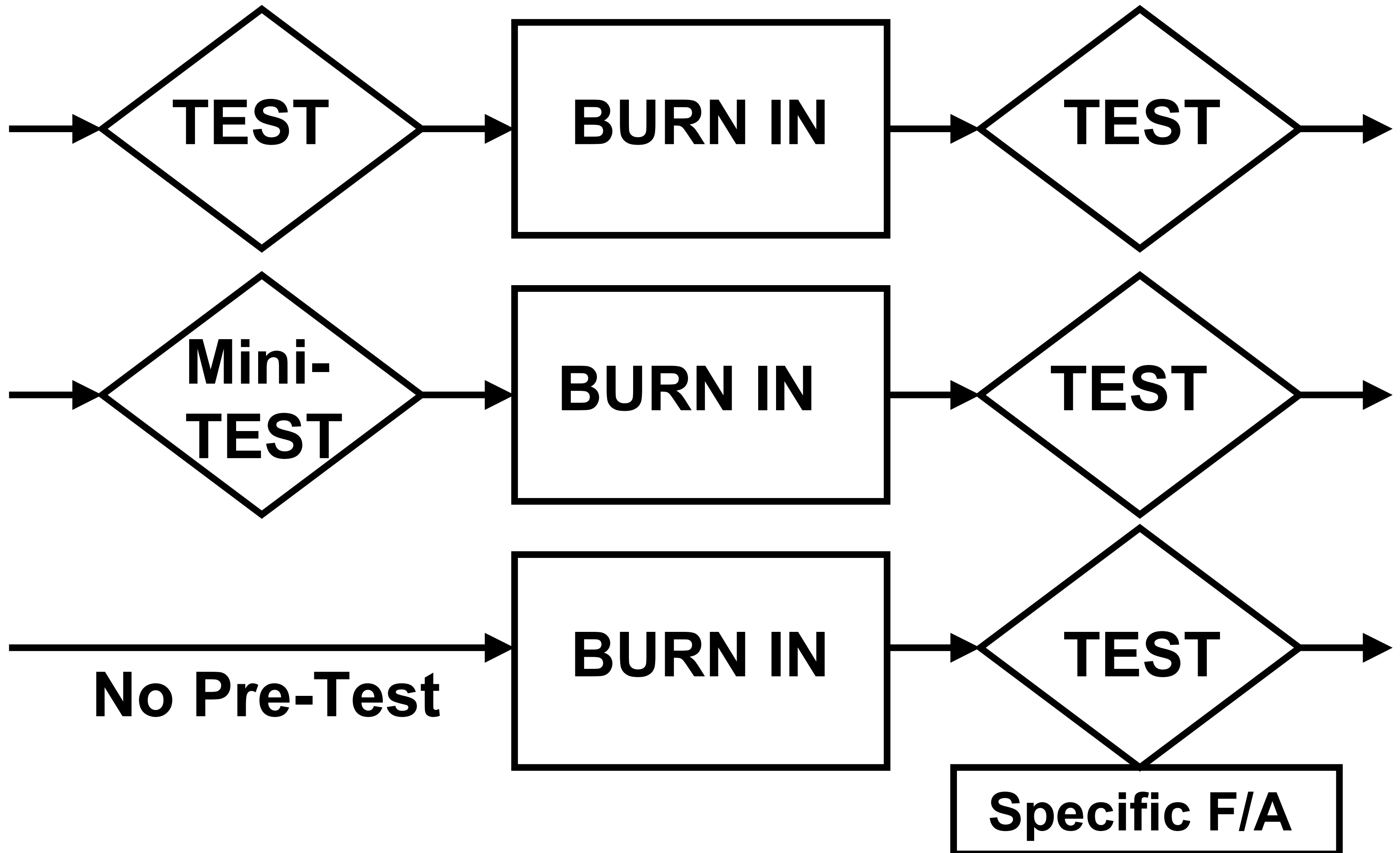
Outline

- Conventional Burn In and Problems
- Wafer Level BI Driving Factors
- Initial Die Level BI
- Technical Challenges
- Viable Wafer Level BI Approaches
- Conclusion

Conventional Burn In

- **Used for years to reduce “infant mortalities”**
- **Mil STD 38510 & Mil STD 883E, Method 1015.9**
- **Typically 125% Vcc, 125° C, 48 to 168 hours**
- **Either DC bias or full dynamic operation**
- **Voltage and temperature life acceleration follow the Arrhenius model:**
  - **Temperature and voltage independently and exponentially accelerate failure modes**
- **Burn In is followed by full final test**

Various Burn In & Test Flows



Conventional BI Problems

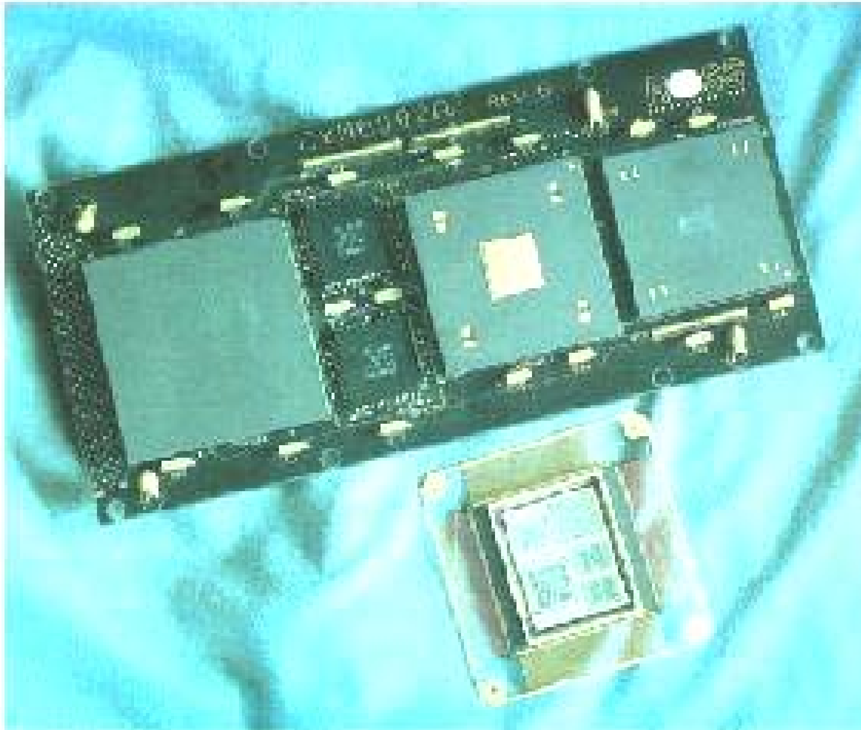
- **Burn In ovens, floor space, and power**
- **Twice as many testers!**
- **Increased cycle time and chip handling**
- **A lot of additional direct labor (cost)**
- **Usually new tooling for each device**
  - **Burn In boards and sockets**
  - **Limits the production ramp up**
- **Customers insensitive to added costs**

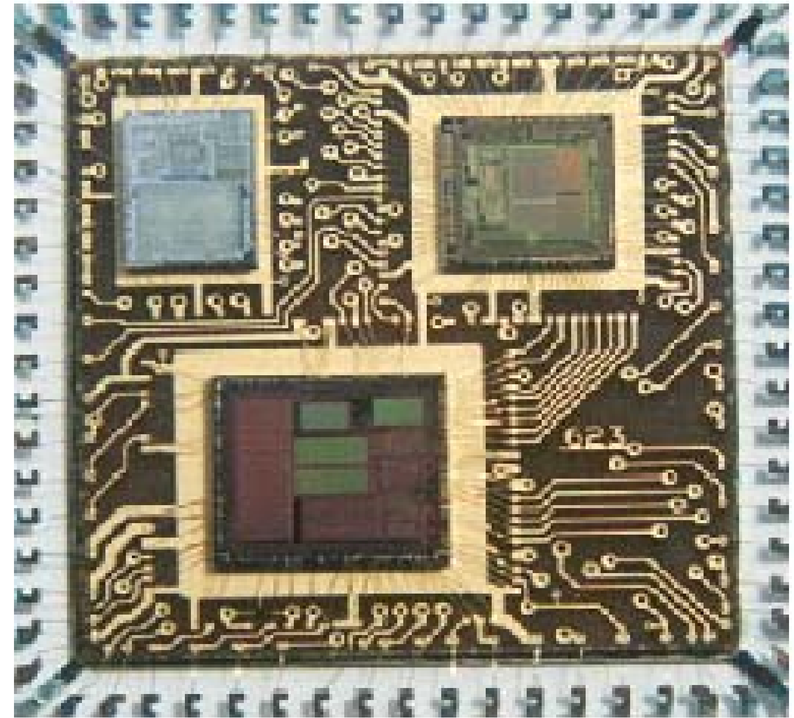
They just want "better reliability"

WLBI Driving Factors

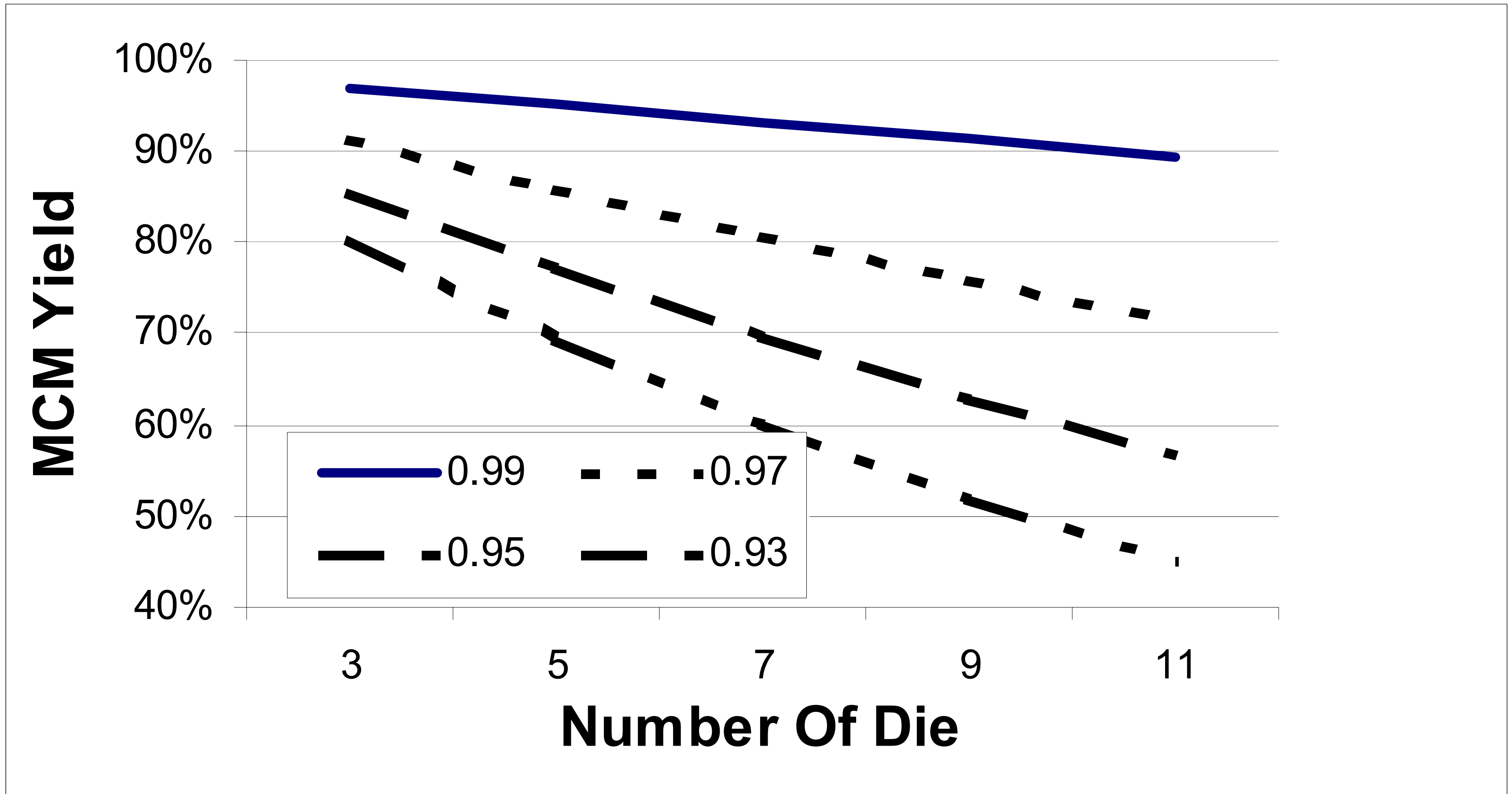
- Cost reduction
  - Burn In was viewed as temporary
  - “We’ll only BI until the new process is stable”
  - When it became stable, *another new process!*
  - Move it closer to the source of the problem
  - Do it cheaper (maybe full wafer BI and test?)
- Known Good Die
  - Customers wanted to buy bare die
  - Needed same reliability as packaged chips
  - Often used in Multi Chip Modules

Multi Chip Modules



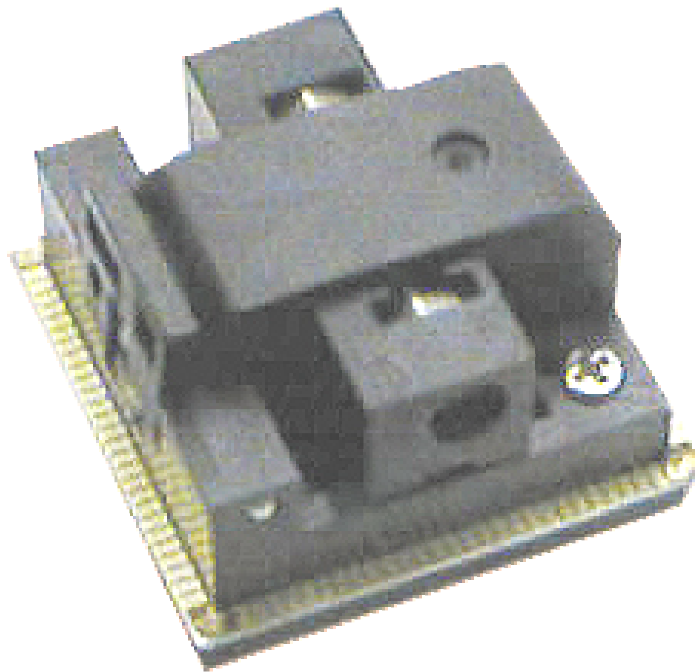


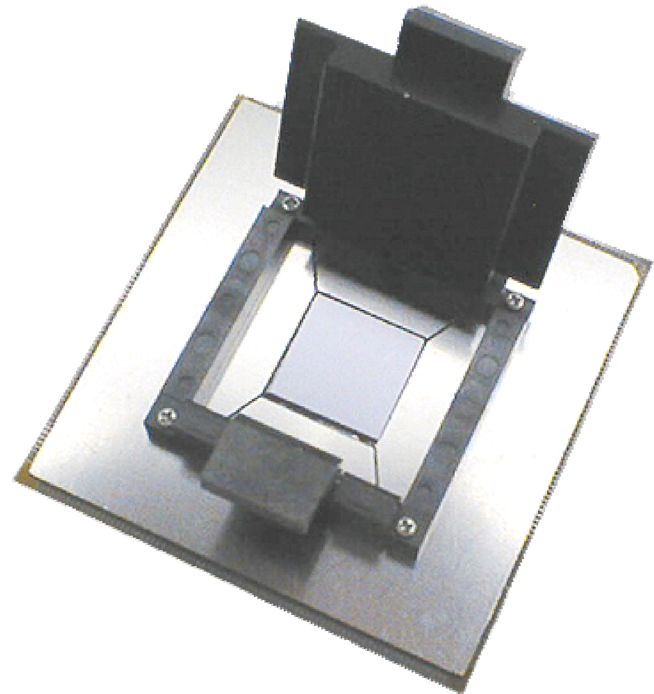
MCM Yields Vs Die Quality



Initial Die Level Burn In

- **Had to address the Known Good Die business**
- **Used temporary die carriers for BI and test**
- **Higher cost, but met the customer's demands**





Technical Challenges

- WLBI took many years and teams of companies to provide viable solutions
- Thermal management due to die density
- Die isolation
  - Density caused issues for stimulus isolation
  - Switching power versus current limit
- Pitch, pad size, and circuitry routing
  - Dealing with small die pitch or I/O fan out
  - Temperature Coefficient of Expansion mismatch
- Wafer to contactor alignment

Large Japan IC Supplier

- Implemented WLBI for die shipments
- Large scale production for the last 3 years
- Three part types in processes down to .17um
- WLBI is added during normal wafer test
- Regular ATE used (often parallel testing)
- Eight additional seconds at 85 degrees C
- Stress done at 136% of rated voltage

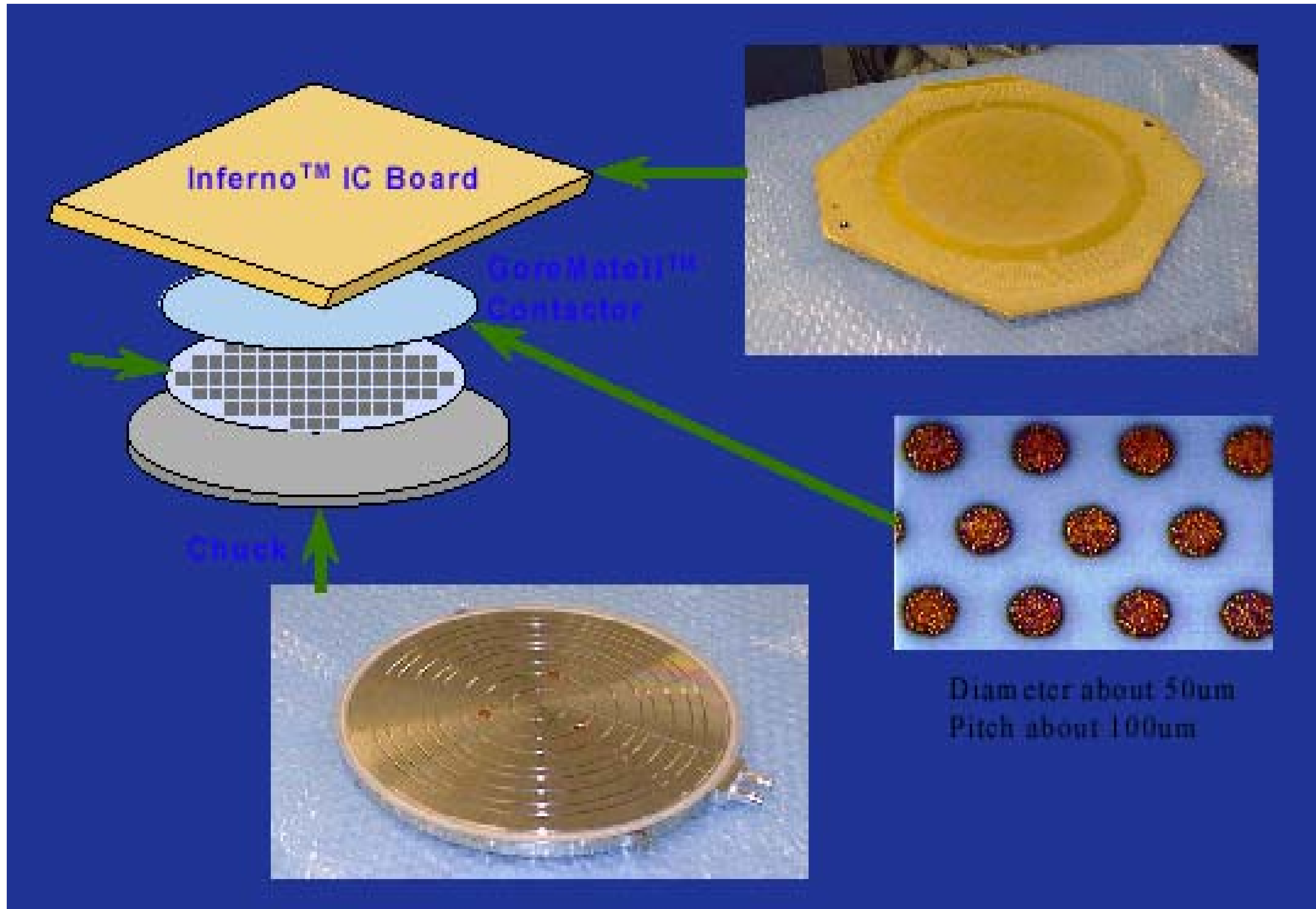
Samsung and Wentworth

- Use a Wentworth Cobra Card with needles for the stimulus channels only
- Samsung uses special ATE
  - Low cost hot chuck probers
  - Low cost stimulus electronics
  - Functional testing is totally separate
- 64 Meg DRAMS, 64 devices in parallel
- 4 touchdowns per wafer
- 15 minutes per wafer, 90 degrees C

Motorola, W. L. Gore, and TEL

- **Joint development program**
- **3 M provided wafer "Inferno" interface board**
- **Contactor material was GoreMate elastomer**
- **TEL supplied BI equipment and automation**
- **Location was Motorola BAT I, Austin, TX**
- **Inferno board with tight line and space pitch requirements was very expensive**
- **GoreMate was consumable and expensive (Gore has left that business; Moto looking)**

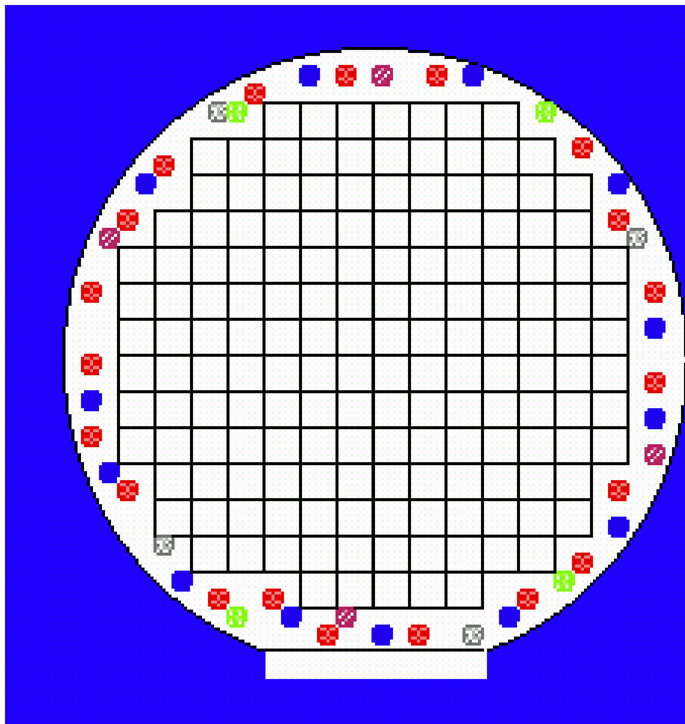
Motorola, W. L. Gore and TEL



Motorola Sacrificial Metal

- Driven by Known Good Die requirements
- Sacrificial metal layer added to wafer
- Parallel bussing of die into clusters
- Burn In I/O contacts are spread out
  - 5” wafers: 4 clusters; I/Os on wafer perimeter
  - 8” wafers: 14 clusters; I/Os on top of clusters
- BI system to wafer I/Os via pogo pins
- DFT features provide dynamic stimulus

5 Inch and 8 Inch Die Clusters



5 Inch And 8 Inch BI Chambers

Motorola Accomplishments

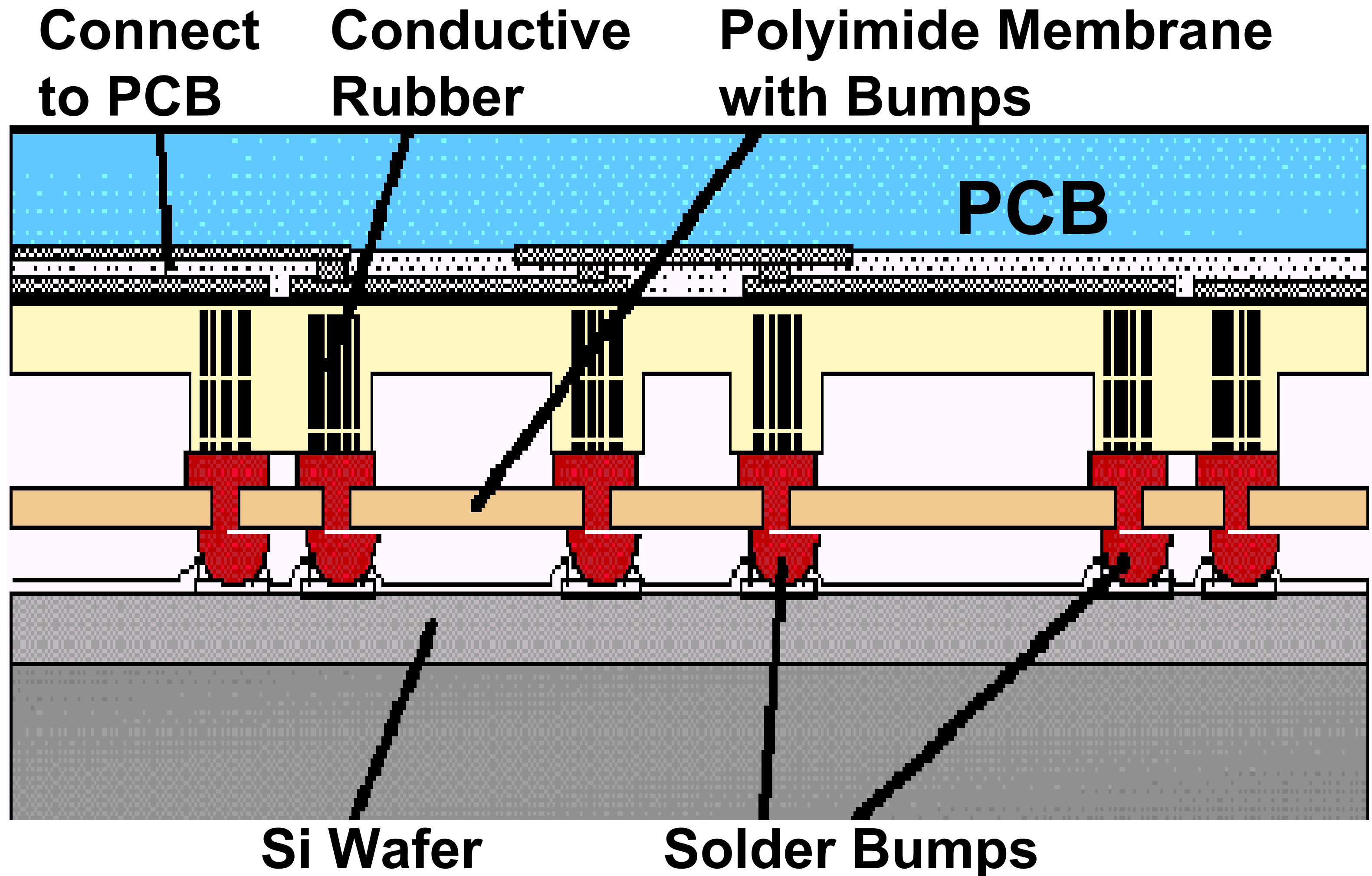
- 5 Inch development began in 1992
- Full production by 1995
- 48 wafers per system
- Over 2 million KGD deliveries

- 8 Inch development began in 1997
- 28 wafers per system
- Production system built in 1999 (Delta V)

Panasonic

- Used for internal memory die requirements
- .5 M devices/year (program began in 1993)
- 15 different part numbers
- Initial full wafer test at 75 C
- 125 C Burn In, typically 2-20 hours
- Controller with 3 ovens per system
- 9 wafers per oven
- TSP membrane probe contactor for wafer interface, vacuum held in place

Panasonic TSP Probe

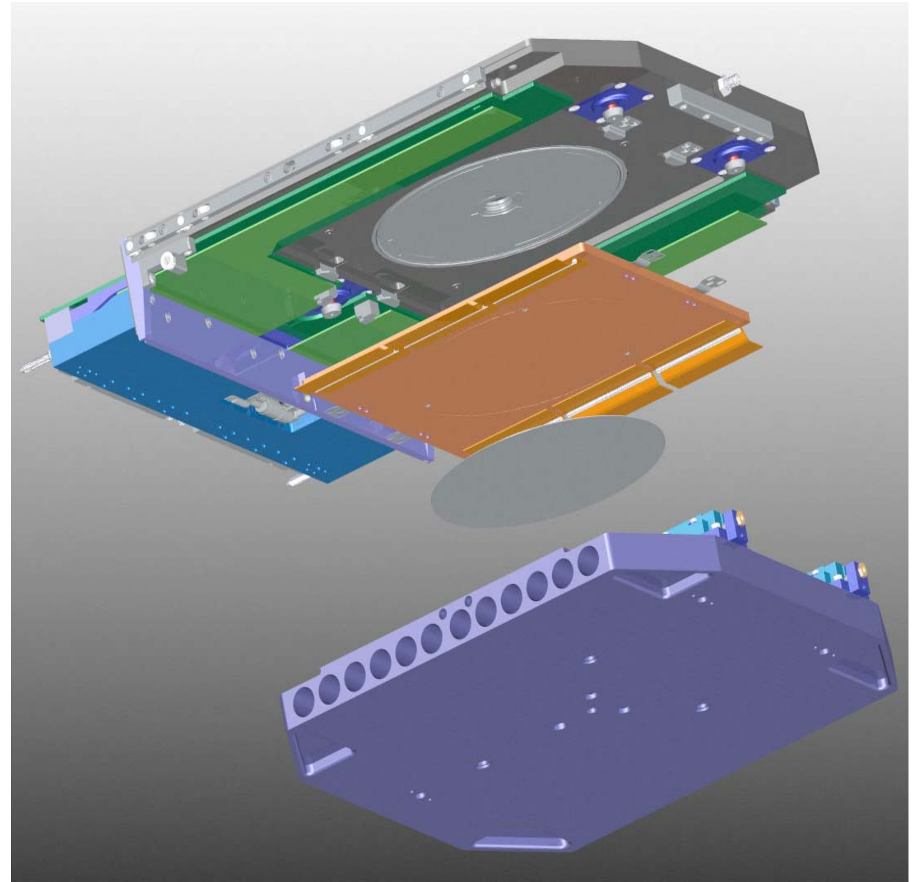


Panasonic

Aehr Test “FOX” BI System

- Partial DARPA funding
- NHK Spring, Yokohama, Japan, (Micro-pogos)
- Electroglas for wafer alignment
- Wafer alignment to the BI PWB is done off-line and Wafer/PWB cassettes are held together with air pressure
- FOX equipment provides stimulus and test electronics, thermal management, DUT power
- Currently being used with Laser Diodes and being evaluated by memory manufacturers

FOX Wafer Alignment/Loading and WaferPak Storage



FOX Wafer BI and Test System

Conclusion

- **Wafer Level Burn In is happening**
- **Multiple vendors provide equipments**
- **Numerous IC suppliers are involved**
- **Primarily driven by customer demands for bare die and Known Good Die**
- **With specialized equipments, processes and designs, it's a costly operation**
- **Cost effectiveness and viability of WLBI totally replacing device BI are still TBD**
- **But WLBI is definitely *moving forward!***

WLBI Is Not For The Timid

- May require design changes and DFT/DFBI
- May require extra fabrication processing
- Expensive to replace depreciated BI ovens
- Burn In itself is becoming questionable
  - New short channel technologies
  - Can’t handle higher voltages acceleration
  - High leakage increase further with temperature
- You may be tossing out or burning up some good parts, shipping “walking wounded,” and/or still passing infant mortalities