Motorola
Wafer Level Burn-in and Test

2002 Southwest Test Workshop

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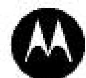
Agenda / Outline

- **Motorola Wafer Level Burn In and Test**
  - **Direct Contact**
  - **Sacrificial Metal**
- **Sacrificial Metal Wafer Level Burn-in and Test Methodology**
- **History of Sacrificial Metal Wafer Level Burn-in and Test**
- **Challenges (Resolved and Present)**

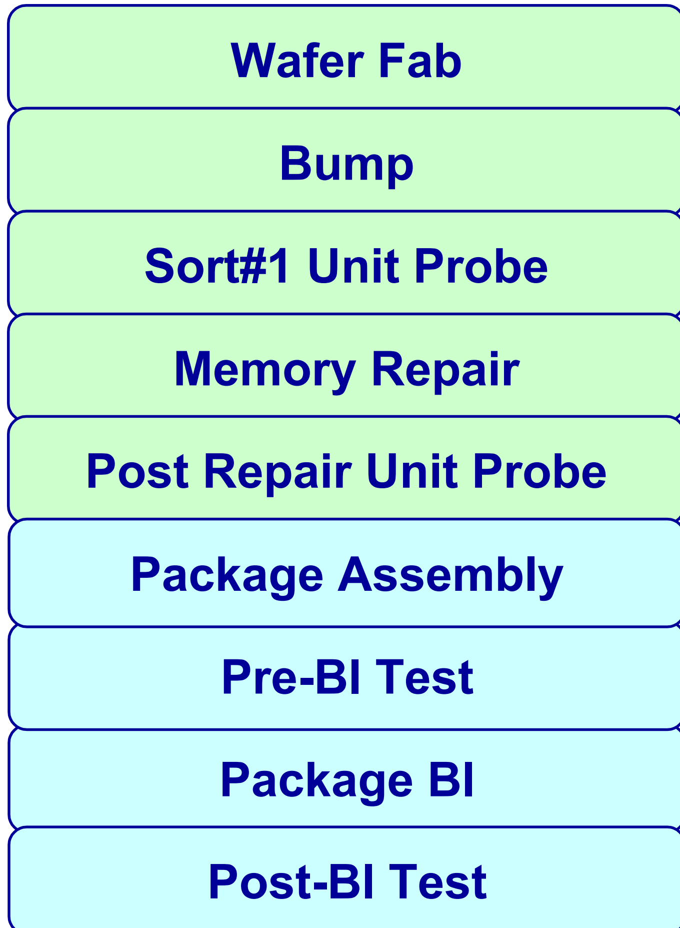
Direct Contact Key Milestones

-Qualified process for C4-FCCBGA for PowerPC product (using Goremate)	June 2001
-Demonstrated test capability for NCSG DSP product and TSPG 32bit MCU	March 2002
-Working to qualify multi-use Goremate replacement	August 2002
-Working to qualify 120um pitch Al wirebond full wafer contactor	August 2002
-Entering product qualification phase for NSCG DSP product and TSPG 32bit MCU	August 2002
-Working to qualify FC contact on eutectic, high Pb, and no PB electroplate PBGA packages	End of 2002



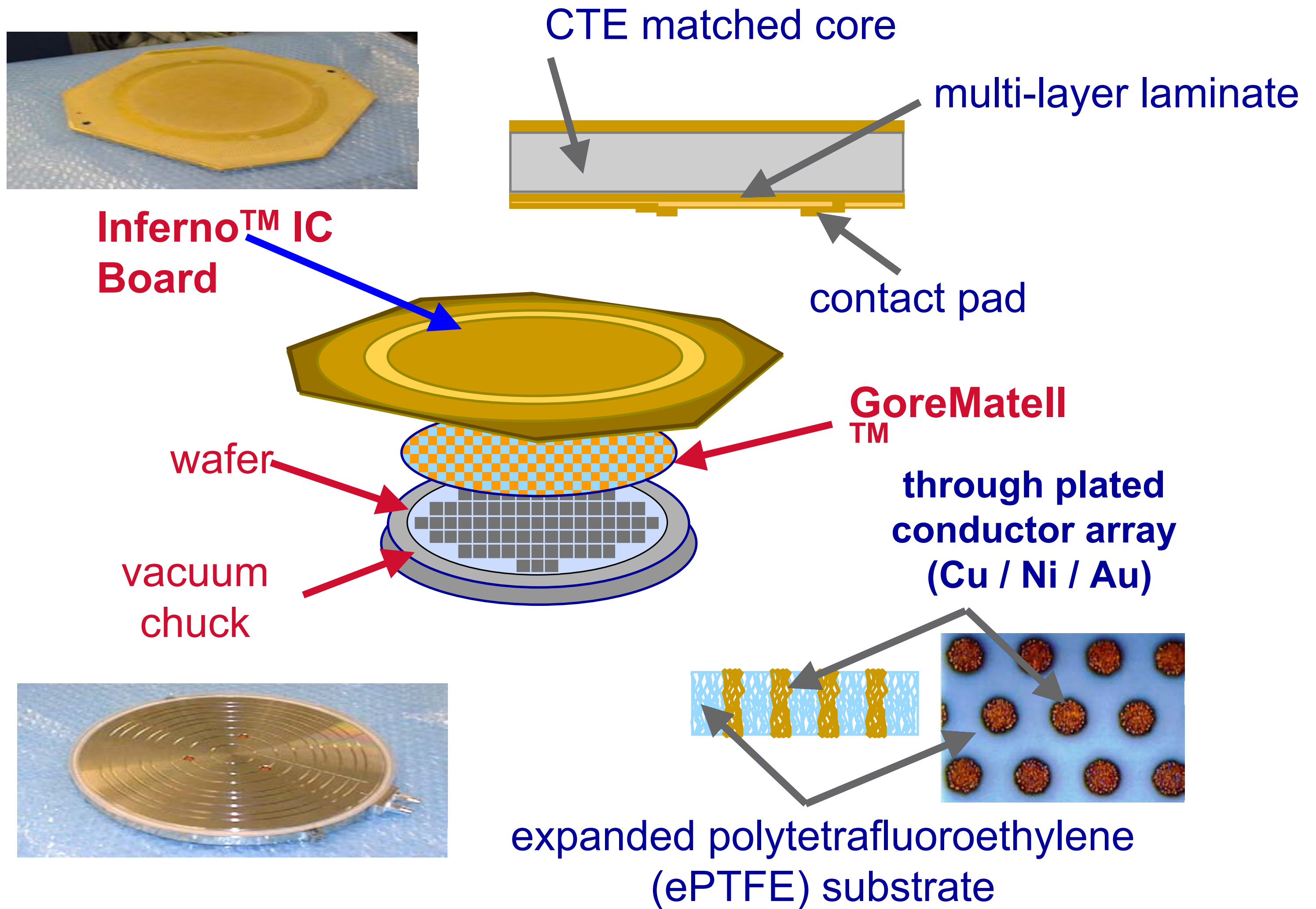
TEL WLBT system installed in Motorola's Final Manufacturing Factory in Austin

Current Package Flow



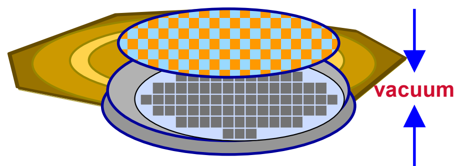
Target WLBT Flow

Standard and WLBT Manufacturing flow for Power PC Devices

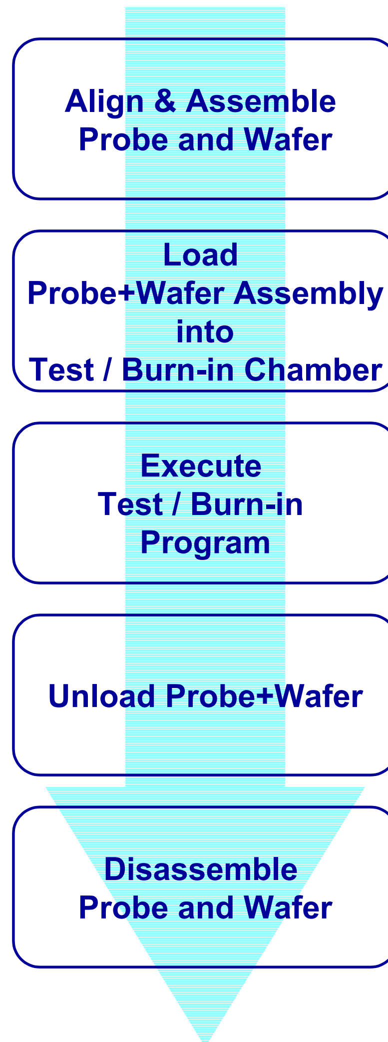


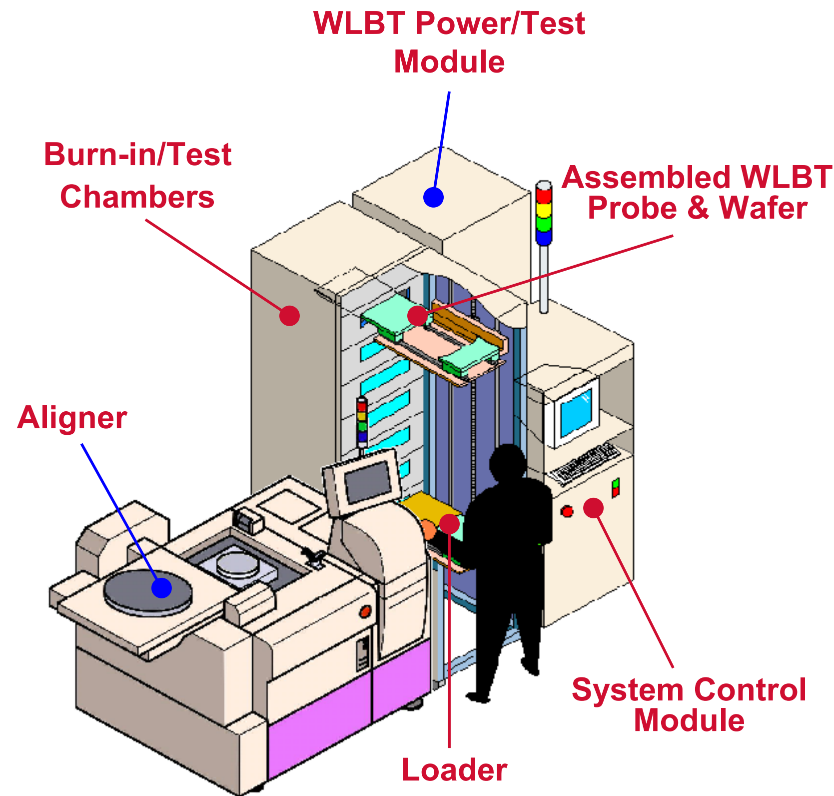
Components of a Full Wafer Contact Solution for Bumped Die Products

WLBT PROCESS OVERVIEW



WLBT Probe & Wafer Assembly





KGD Sacrificial Metal WLBI
- Definitions -

- **Wafer Level Burn-In (WLBI) and Test**
  - Parallel, dynamic, excitation of all devices on a wafer to screen for marginal devices for infant mortality by dynamically stressing the integrated circuit at elevated temperature and voltage. Capable of non-volatile memory cycling, module exercising, and testing.
- **Known Good Die (KGD)**
  - Die having the same quality and reliability level as that of an equivalent packaged part.
- **Sacrificial Metal (SM)**
  - Metal which is temporarily deposited on the wafer to provide electrical signal paths to a die during wafer level burn-in and test. The sacrificial metal is etched away after burn-in and test is complete.

Why the need for WLBI?

- **Smaller form factor requirements in personal communication, computer and automotive markets have increased demand for KGD.**

- **Burn-in for KGD at wafer level requires less test insertions and reduces cycle time than with die level burn-in. Similar cycle time reductions can also be realized for wirebond devices by screening out early life failures before assembly.**

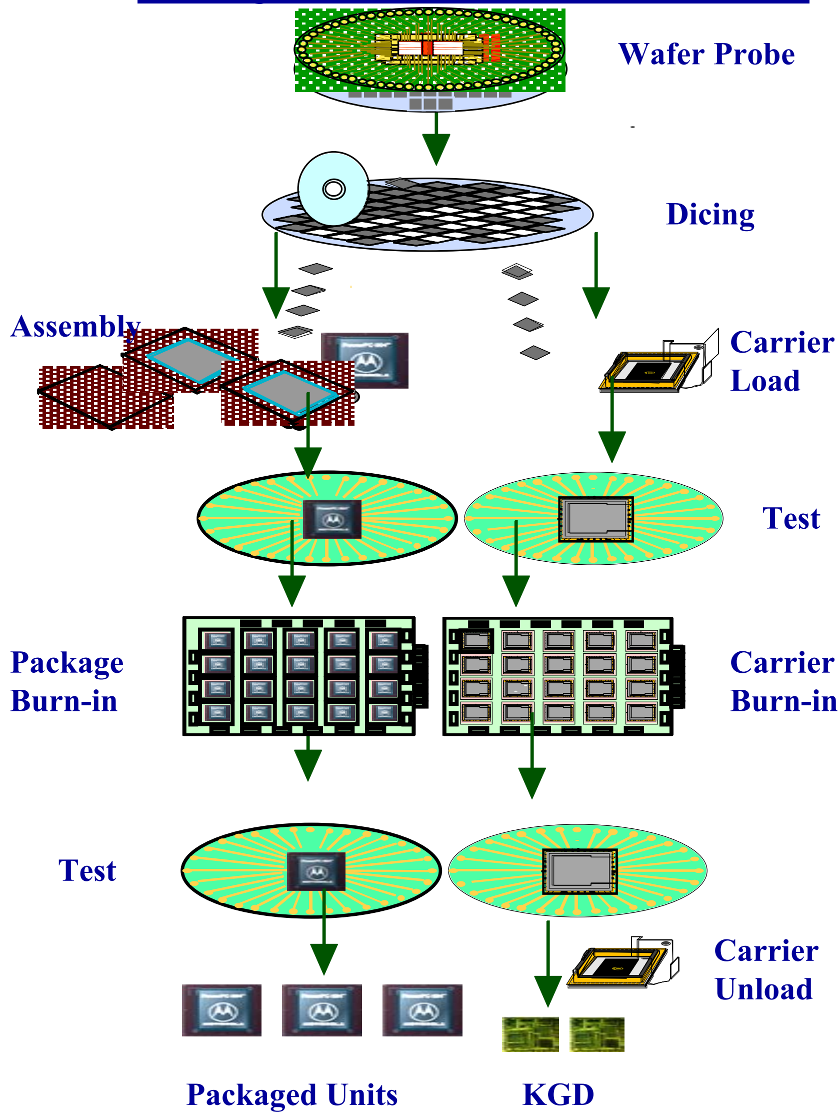
- **WLBI provides quicker feedback to wafer manufacturing, which improves responsiveness to provide more effective process control.**

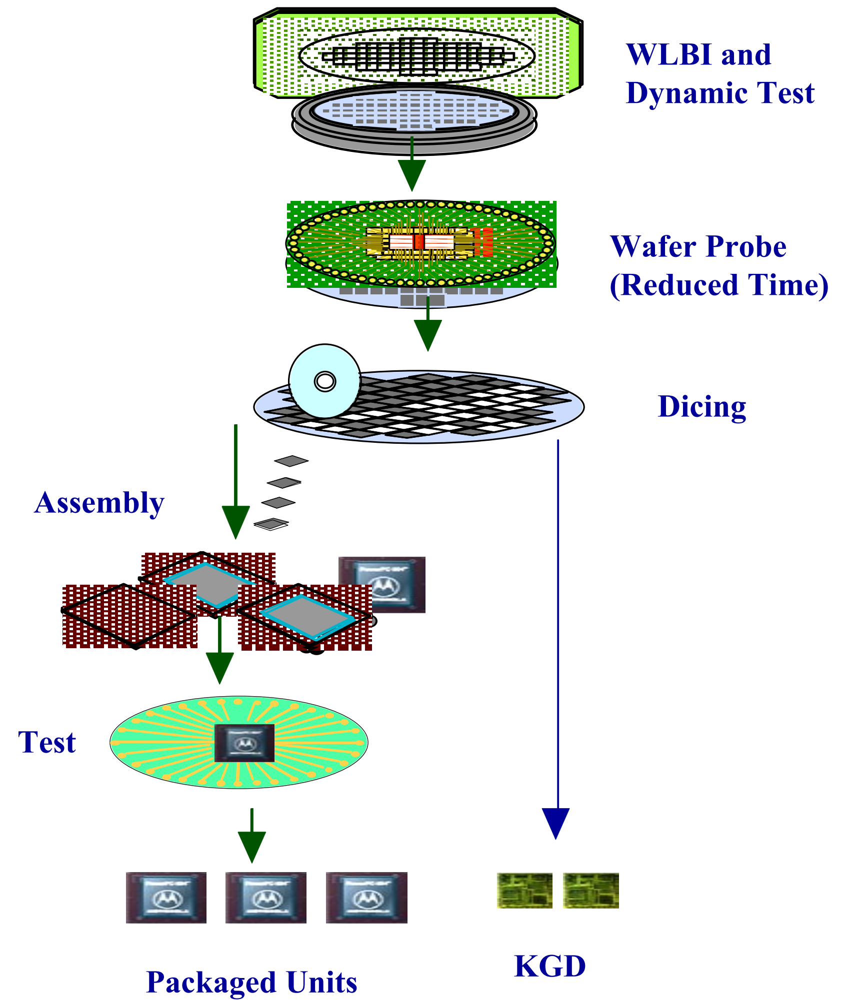
WLBI Technology Partners

The following cooperative effort is currently the only effective WLBI technology in production in the world:

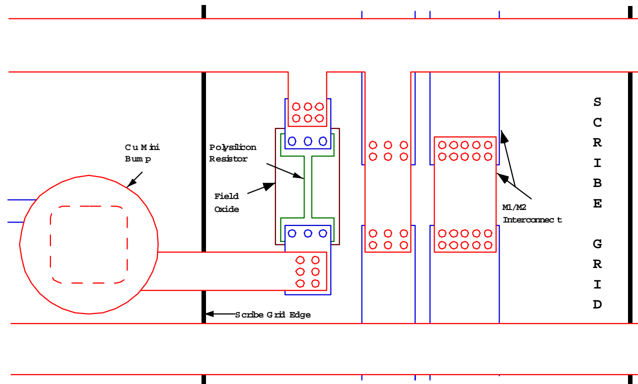
- **Motorola Semiconductor Products Sector**
  - **Transportation & Standard Products Group (TSPG) – Austin, TX**
    - » **Design and product engineering support for WLBI**
  - **Strategic Manufacturing Deployment (SMD) – Chandler, AZ / Austin, TX**
    - » **WLBI circuit definition**
    - » **Production burn-in and data retention bake process**
    - » **Post-WLBI data processing**
    - » **WLBI circuit removal**
    - » **Bump process**
    - » **Saw, tape and reel**
  - **MOS 12 Fab – Chandler, AZ**
    - » **Wafer manufacturing**
    - » **Probe support**
- **Delta V Instruments – Richardson, TX**
  - **Design and maintenance of WLBI systems**
  - **Assembly and repair of WLBI fixtures**
  - **WLBI software support**

Wafer Level Burn-in Methodology



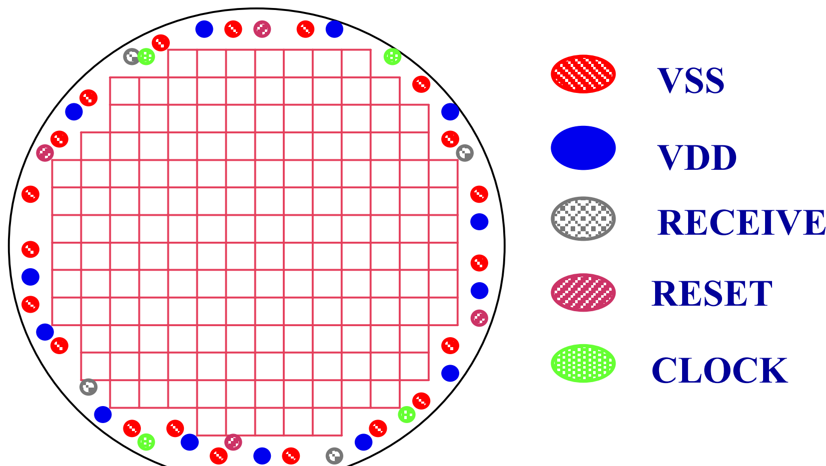


5 inch Wafer Level Burn-In Methodology



Scribe Grid Structure

- Resistor in series with pad
- Cross overs / cross unders for balanced power distribution
- Bridge pass over die edge oxide moat

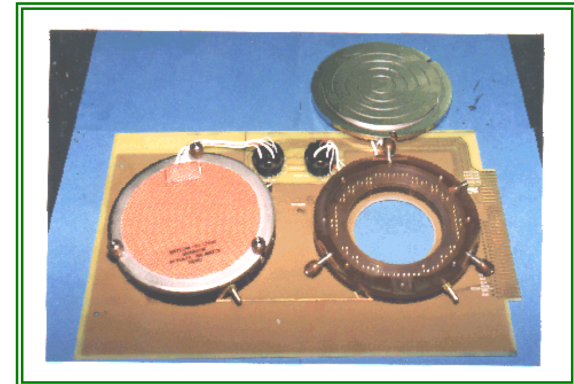


- Contact pogo pads placed at the edge of the wafer

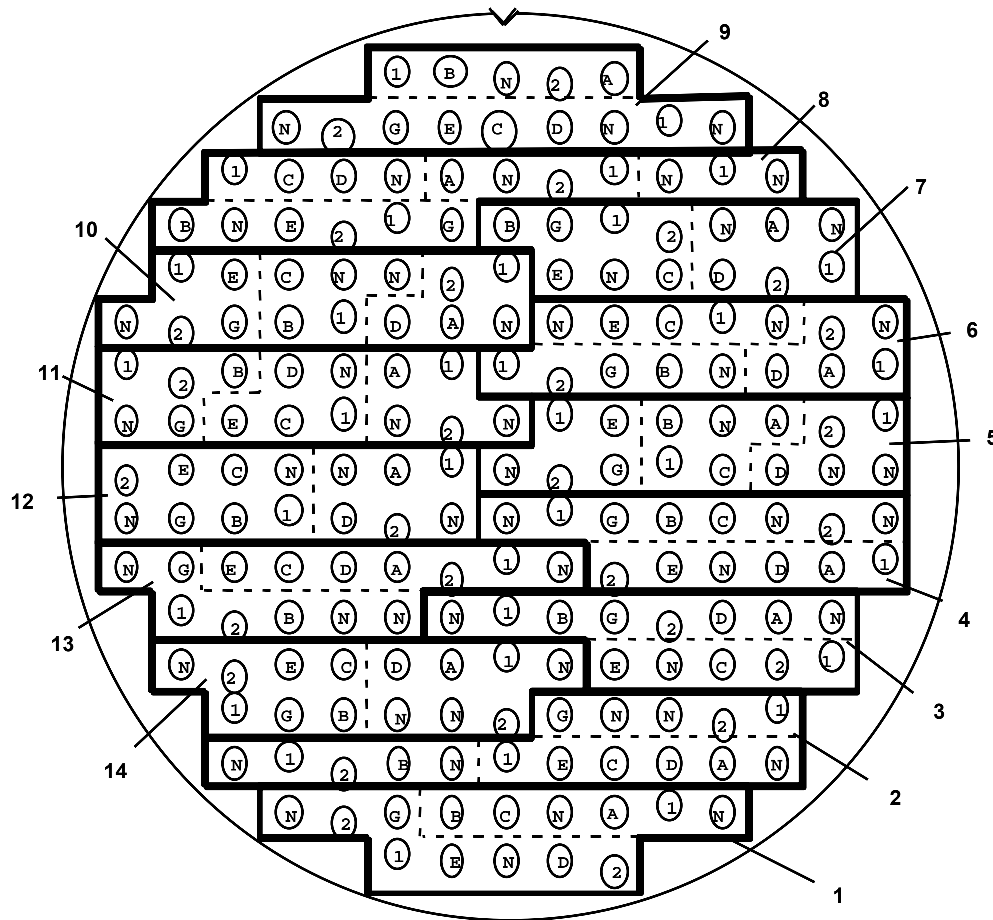
5 inch Wafer Level Burn-In Methodology

Post wafer fab process (with polyimide)

- Deposit, pattern and etch sacrificial metal
  - Parallel electrical bussing of all die per quadrant
  - Photo define burn in contact pads
  - Contact current limiting resistors
  - Contact scribe grid cross-unders
- Burn-In and Data Retention Bake (DRB) test for NVM devices
- Remove sacrificial metal
- Die sales, bump or package



8” WLBI Methodology

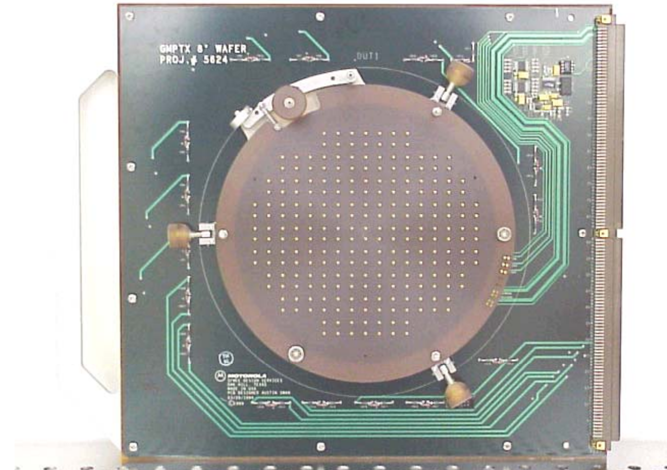


Cluster Arrangement - Viewed Looking at the Wafer Face

8 inch WLBI Methodology

Post wafer fab process (with polyimide)

- Deposit, pattern and etch sacrificial metal
  - Parallel electrical bussing of all die in a cluster
- Wafer level burn in (6 to 24 hours @ 125 °C)
- Data Retention Bake (2 to 24 hours @ 270 °C)
- Remove sacrificial metal
- Bump (flip chip only)
- Wafer probe
- Visual, dice, tape and reel
- Ship to customer



History of Sacrificial Metal Wafer Level Burn-in

5 inch Wafer Program

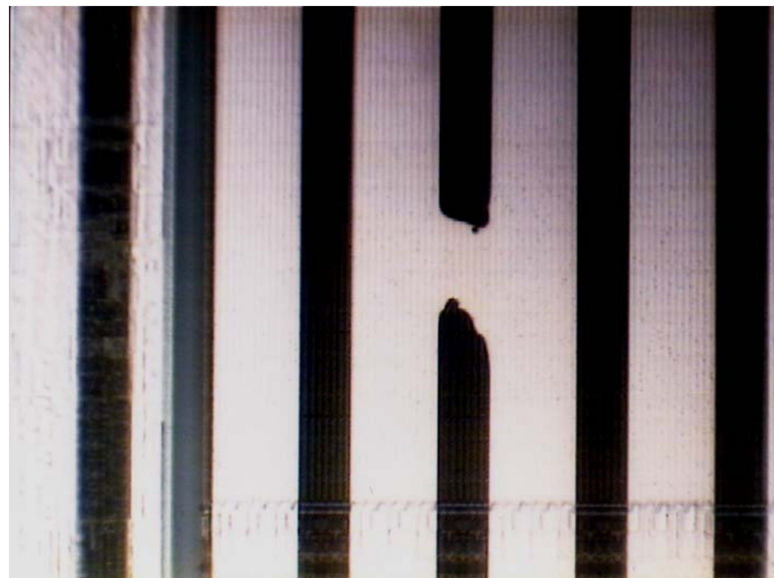
- Development began in 1992
- Eighteen wafer capacity system built in 1994
- Production started in 1995
- Full lot capacity production system built in 1997
- Over 2 million KGD delivered since 1995 with no documented non-volatile memory (NVM) field failures

History of Sacrificial Metal Wafer Level Burn-in

8 inch Wafer Program

- Single wafer engineering system built in 1997
- Successful 8 inch WLBI in 1997
- Prototype Production System Built in 1998
- Production System Built in 1999

Resolved Challenges



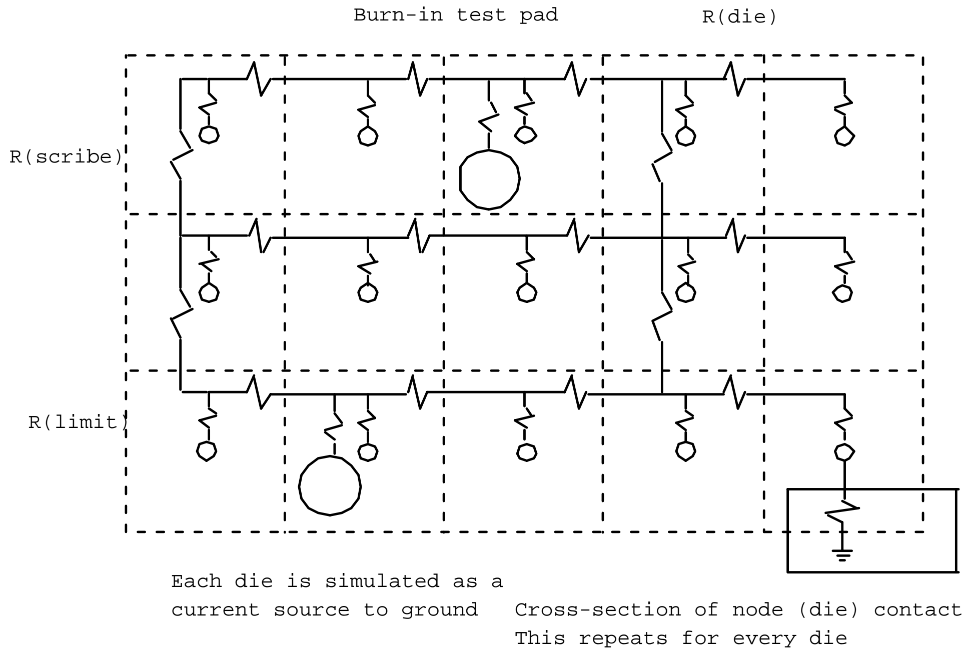
Poor sacrificial metal adhesion

Sacrificial Metal Criteria:

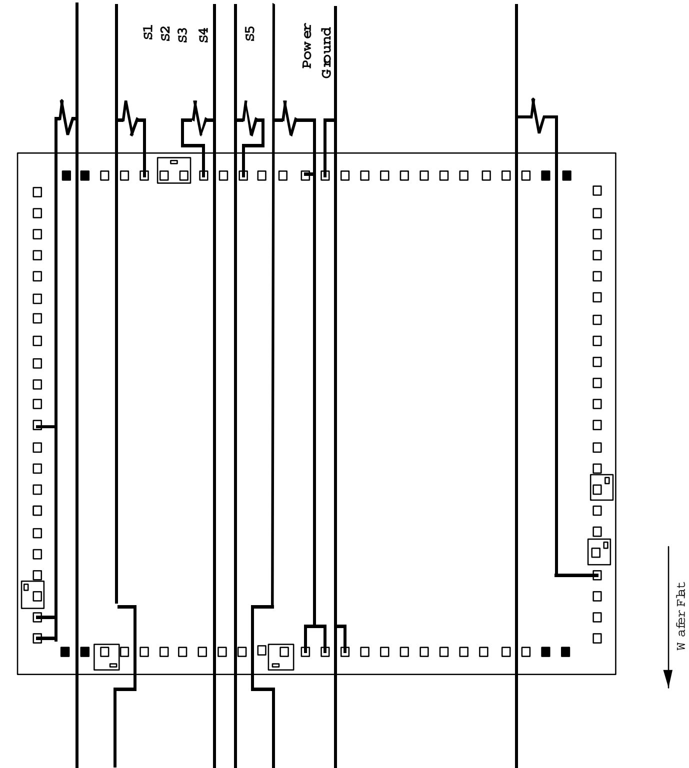
- Good adhesion to polyimide
- Proper conductivity to carry signals and voltages
- Ease of sacrificial metal removal after WLBI and test
- Maintain die pad integrity after sacrificial metal processing
- Toughness to survive contactor and test conditions

Resolved Challenges

Sacrificial Metal Design:



R(die)= total conductor resistance from one die node to the next
R(scribe)= total resistance between two main burn-in conductor within sc
R(limit)= total resistance of the Current limiting resistor circuit



Cluster Scheme

Die Scheme

•**Adequate thickness and width to carry the necessary signals and voltages and maintain balanced power distribution.**

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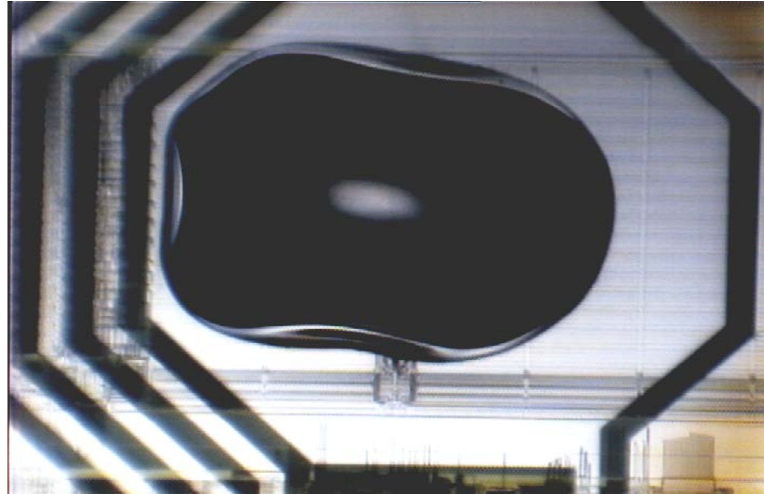
Resolved Challenges

Polyimide Criteria:

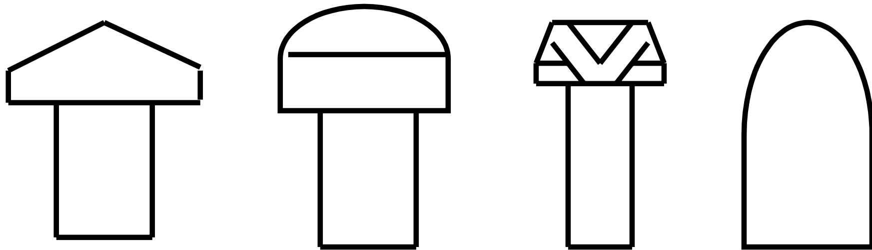


Blistering sacrificial metal

- Proper adhesion to sacrificial metal and wafer during test conditions
- Good definition for adequate step coverage
- Sufficient cure to survive sacrificial metal processing and test conditions

Resolved Challenges

Contactor (Pogo Pin) Criteria:

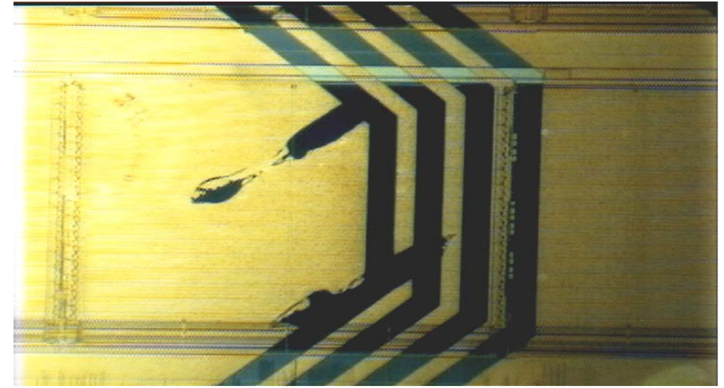


Various pogo pin head shapes

Melted Heater Pin Area

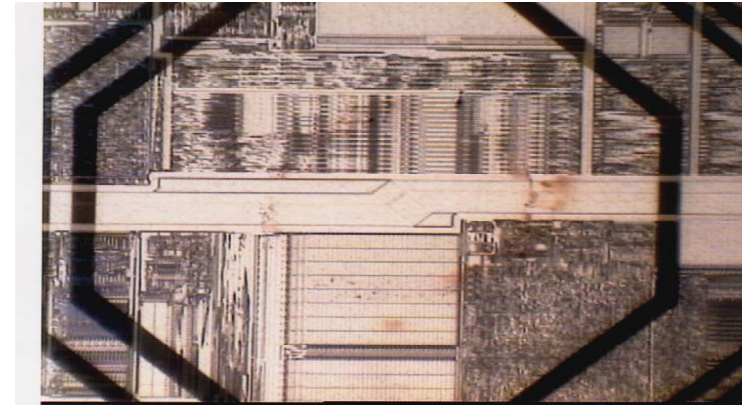
- Custom design spring force, travel distance, head shape, materials
- Mechanically robust at elevated temperature and 1000s of cycles
- Ability to integrate the pogo pins into the WLBI fixture

Resolved Challenges



Pogo Block Material Criteria:

Material A CTE 20 ppm/ºC



Material B CTE 2.5 ppm/ºC

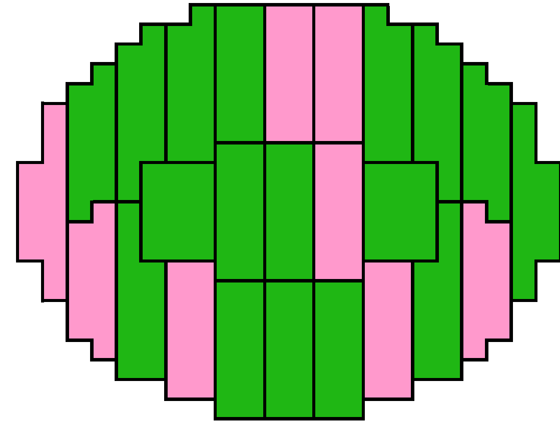
- Cost
- Material availability
- Manufacturability and machinability
- Durability during WLBI and test at elevated temperature
- Maintaining planarity and adequate pogo pin compression during WLBI and test

Resolved Challenges

Yield Improvement Through Enhanced System Communication

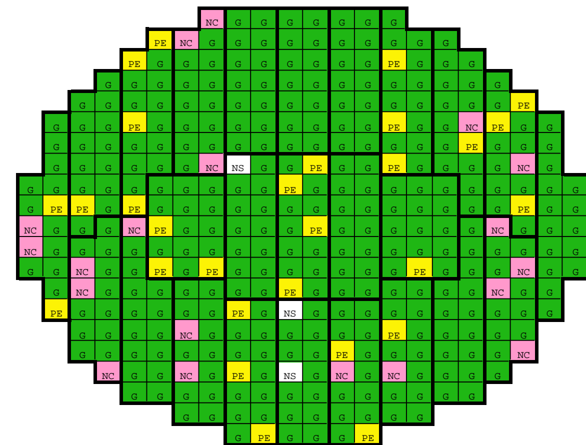
Previous

- Recognized Good / Bad Clusters Only
- Final Test Results at Probe



Current

- Recognize Individual Die
- Generates Wafer Map Pass / Fail Codes Per Die



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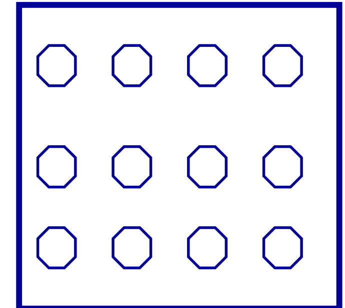
Present Challenges

- **High Contact Count (HCC)**



	Current	HCC
# Pogo Pins	About 600	About 3000

- **WLBI Cold Temperature Test (-40 C)**

Summary

Sacrificial Metal Wafer Level Burn-in and Test

- **Sacrificial metal wafer level burn-in is a low cost test solution to achieving known good die.**

- **Motorola has been in production utilizing this technology since 1995.**

Acknowledgments

This speaker would like to acknowledge the teamwork from various Motorola SPS groups, Delta V Instruments, and Despatch Industries that contributed to the development and continuous improvement of this Sacrificial Metal Wafer Level Burn-in and Test program.

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