Solutions to Technical Challenges for WLBI

Steve Steps

AEHR TEST SYSTEMS

Major Technical Challenges

- "Only" three major challenges
  - Thermal
  - Mechanical
  - Electrical

Major Thermal Challenges

- Adding heat or usually removing heat in the order of hundreds of watts

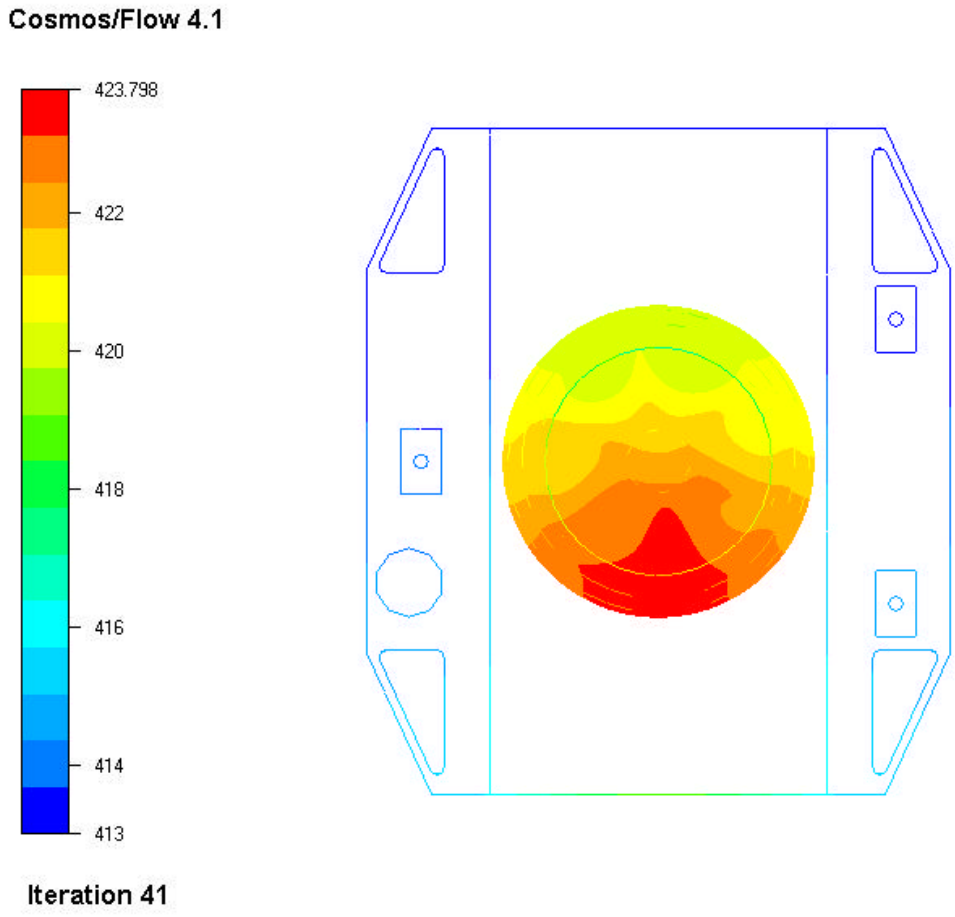
Thermal Chuck

- Uniform wafer temperature
  - Independent of yield
  - up to 150 C
- Dissipates high power per wafer
- Simple, air cooled design

Major Thermal Challenges

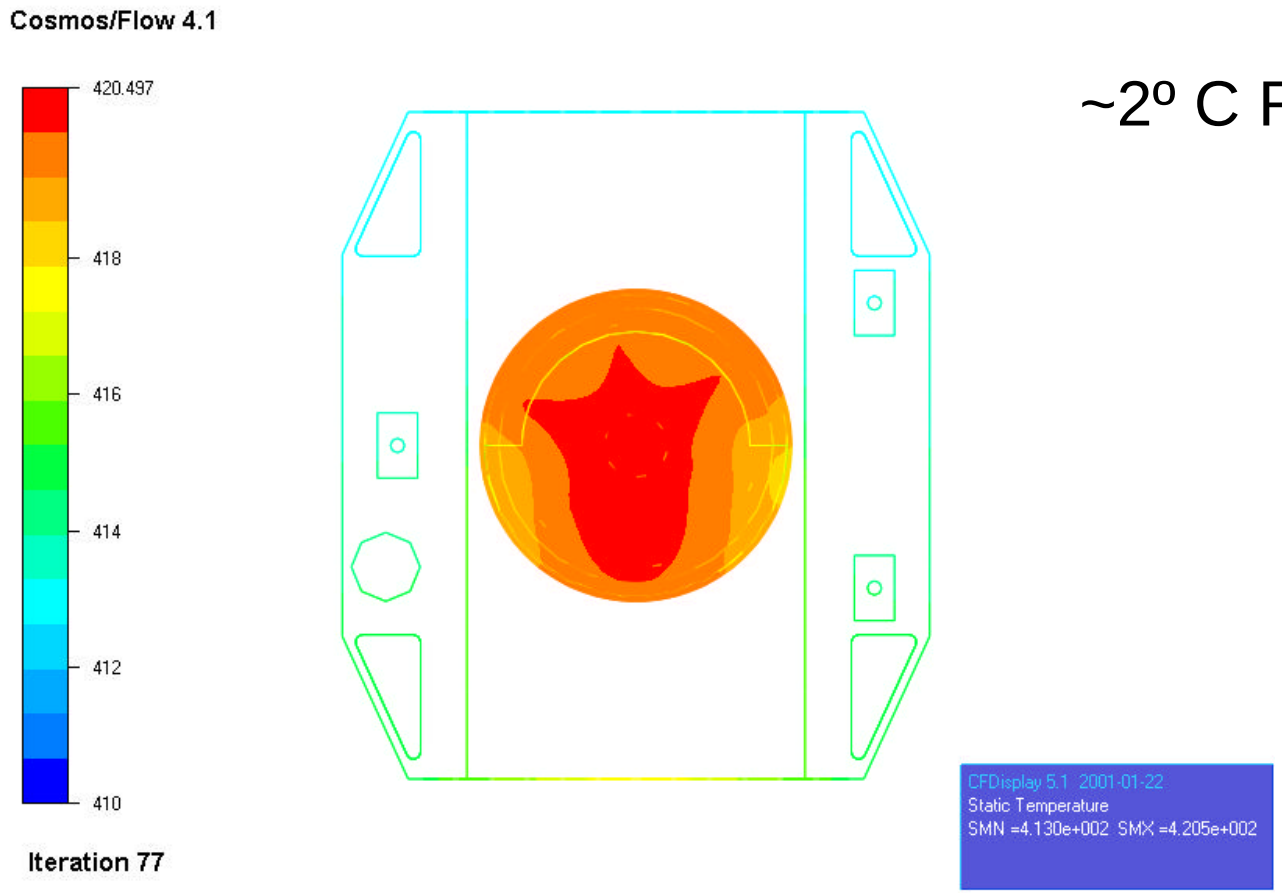
- Adding heat or usually removing heat in the order of hundreds of watts
- Maintaining constant temperature across wafer

Thermal Chuck



~4º C Range

Chuck With Optimizing Heaters



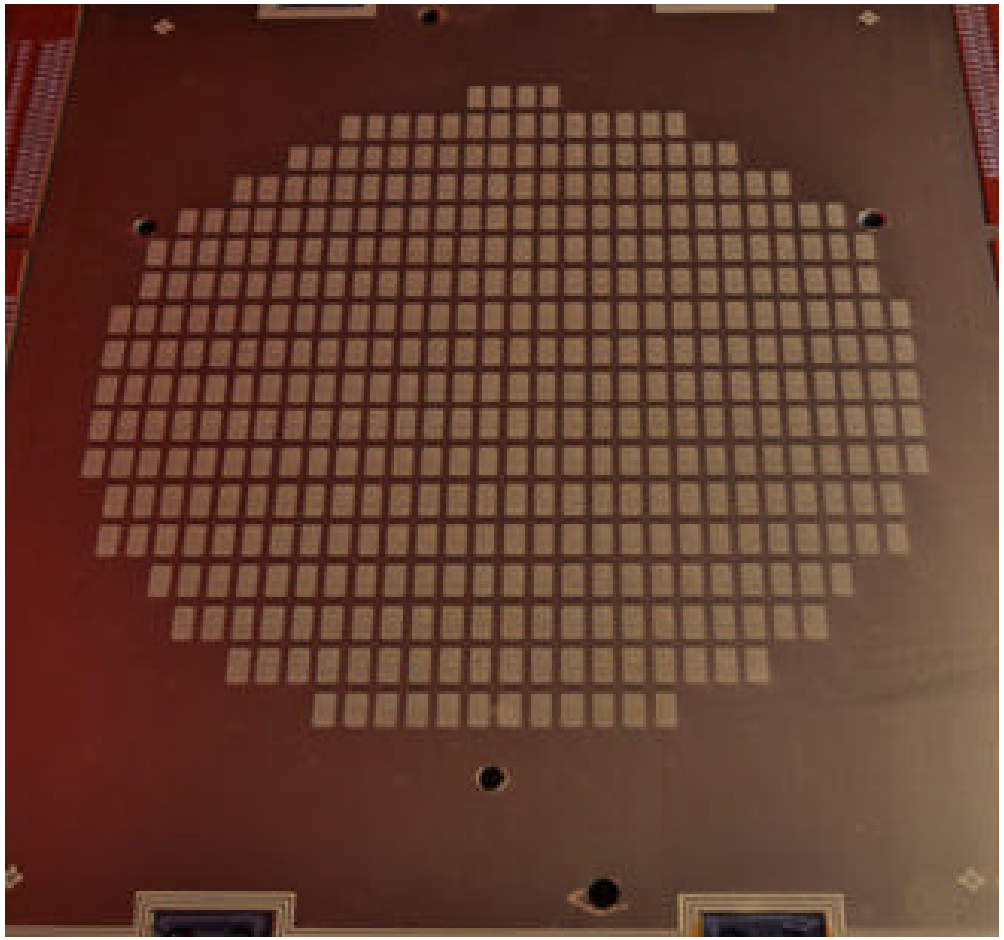
~2º C Range

Major Thermal Challenges (cont.)

- Maintaining constant temperature across wafer
- Adding heat or usually removing heat in the order of hundreds of watts
- Coefficient of thermal expansion mis-match
  - 8” Si wafer edges expand from wafer center by over 50 microns from 25 to 150 degrees C.
  - PC board will expand about 250 microns over same range.

Interconnect Substrate

- Functions like a PC board
- CTE matched with wafer
- Contactor also CTE matched to wafer



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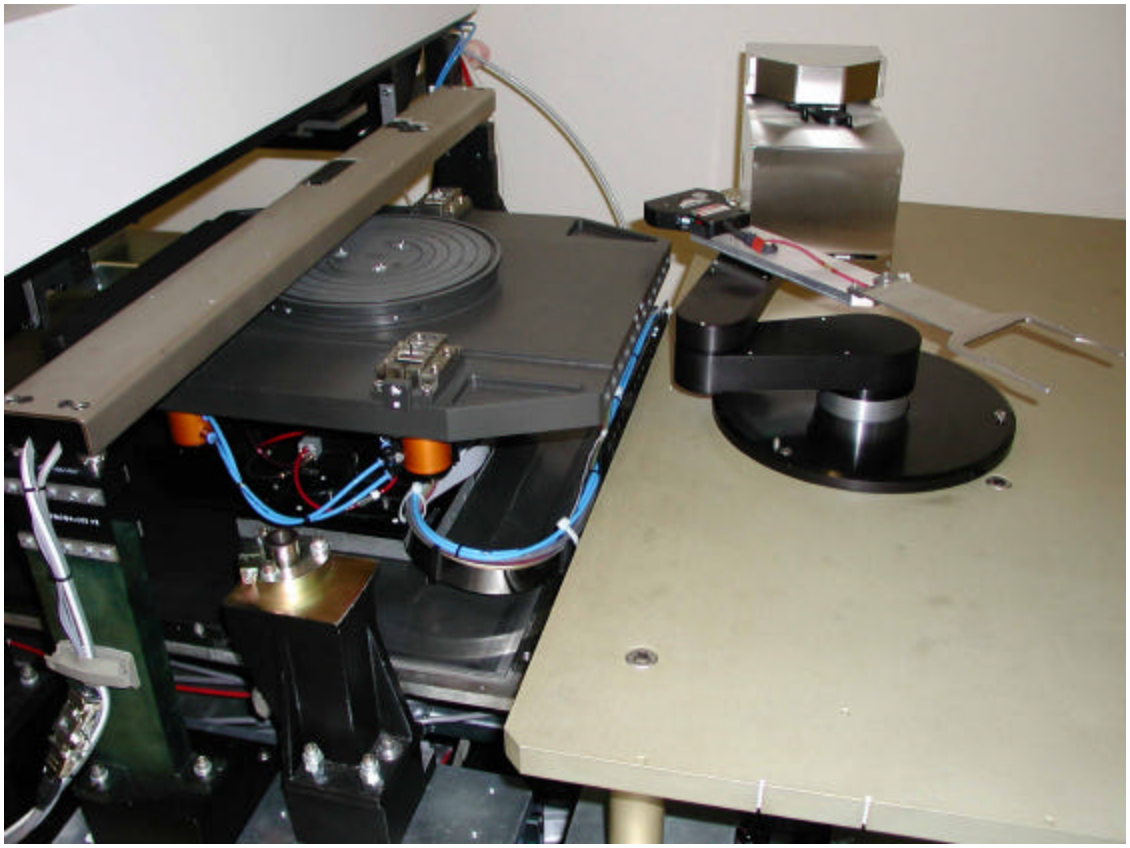
Mechanical Challenges

- Aligning wafer to contactor

WaferPak™ Alignment Station

- Loads and unloads wafers between WaferPak and cassette
- Aligns the wafer to the probe/contactor using both upward and downward cameras

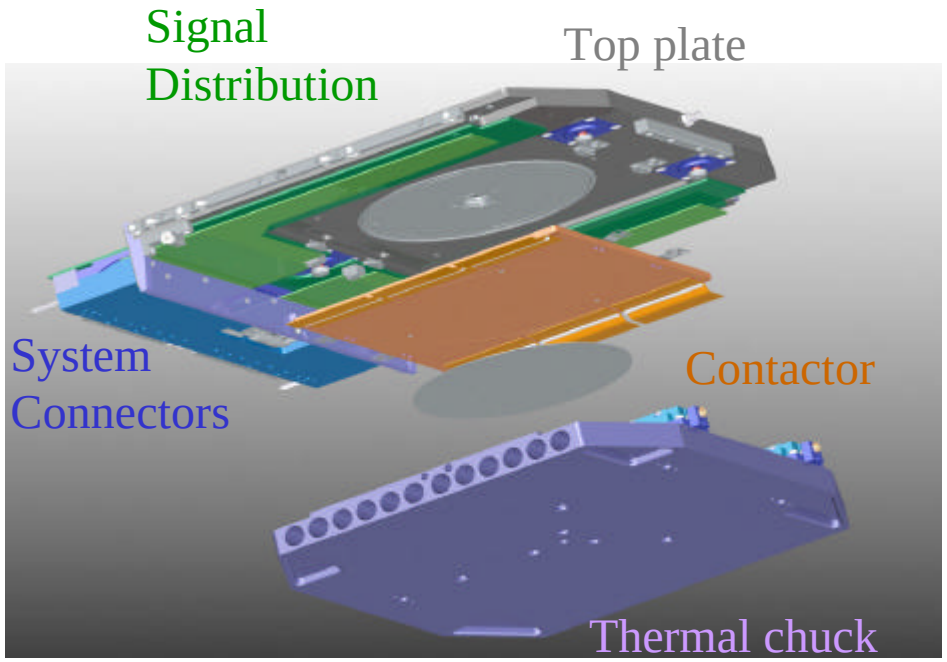


Mechanical Challenges (cont.)

- Aligning wafer to contactor
- Cost effective

WaferPak™ Modular Components

- Cartridge based solution simplifies hardware
- Loaded WaferPak is like a Burn In Board
- One Alignment Station per customer site versus per wafer

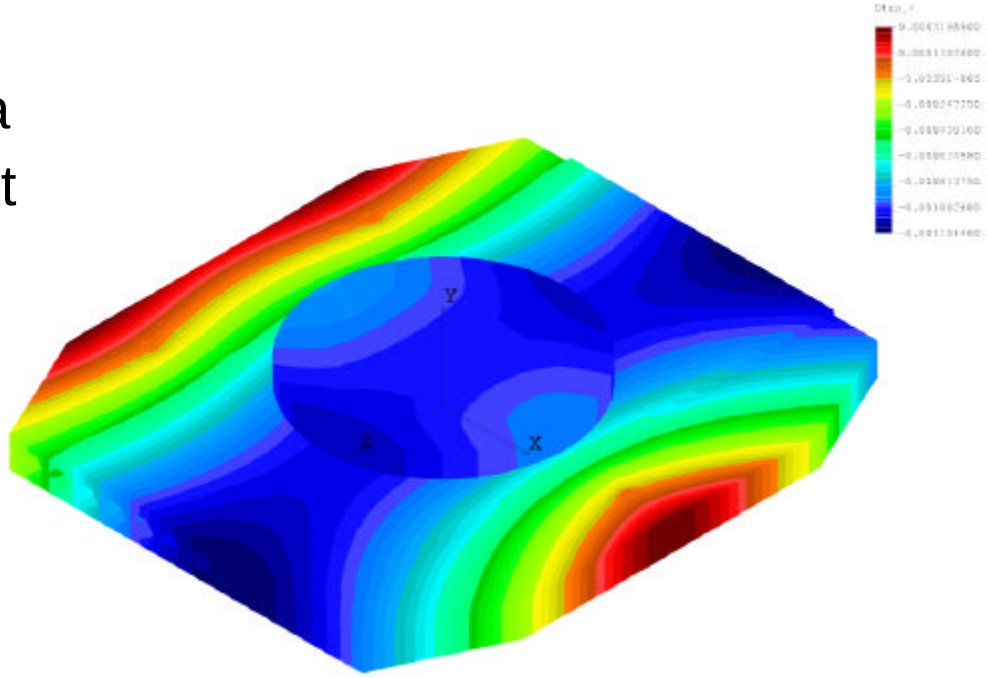


Mechanical Challenges (cont.)

- Aligning wafer to contactor
- Cost effective design
- High contact pressures
  - 8” SDRAM wafer with 50 pads/die, 500 die requires 25,000 pin contactor
  - At 10 grams per pin about 250 kg required
  - Maintain planarity to microns at these forces

Thermal Chuck Flatness Test Results

- Thermal chuck analyzed and designed to provide a very flat surface in contact with the wafer
- Used Cosmos Finite Element Analysis tools



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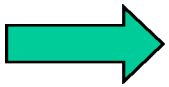
- How to generate and control such high forces

Contactor Force Control

- Pressure based versus Vacuum based
  - Not limited to one atmosphere
  - More precise, uniform control of force
  - Any leaks drive away contamination
  - Can control location of force
- Probe to force versus to position
  - Required for most contactor technologies
  - Compensates for non-planarity



Full wafer contact produces on-axis forces

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- Cost effective design
- High contact pressures
  - 8” SDRAM wafer with 50 pads/die, 500 die requires 25,000 pin contactor
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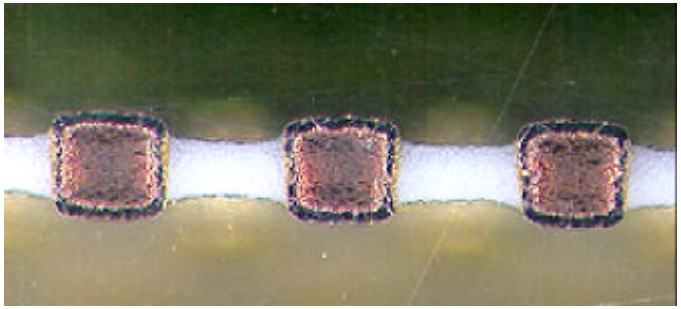
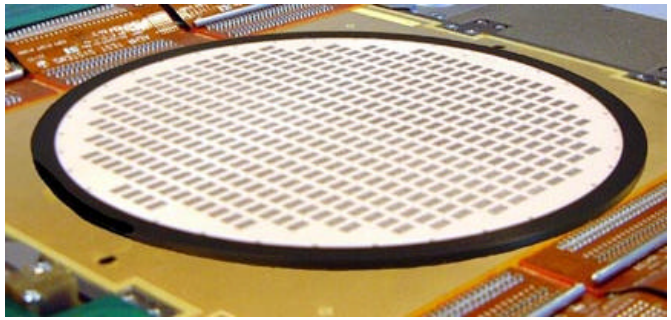
  - Maintain planarity to microns at these forces
- How to generate and control such high forces
- Best contactor varies per application

Contactor Choices

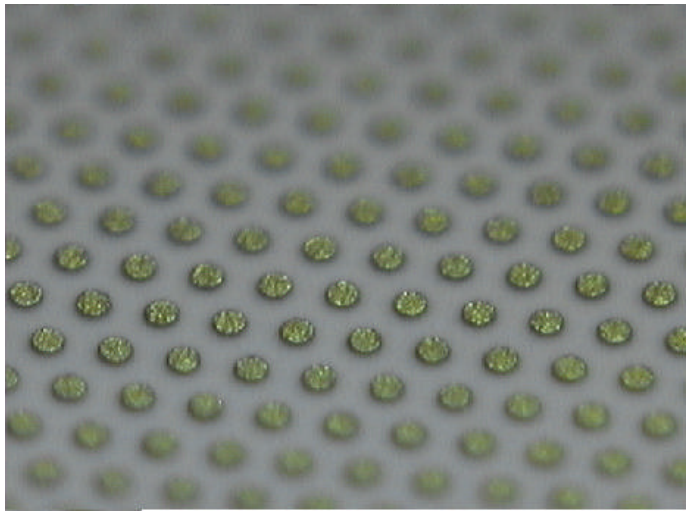
- Highly modular system supports multiple contactor technologies for Au, Al, Cu, UBM or solder balls
- Consumable Sheet
  - Lower NRE
- Micro pogo spring
  - High touchdown life
  - Great for relocated pads
- Ultra fine pitch

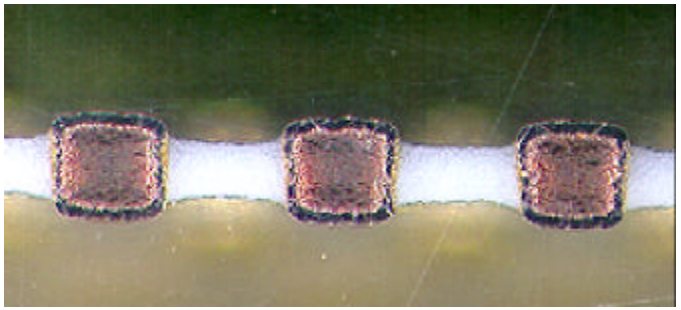




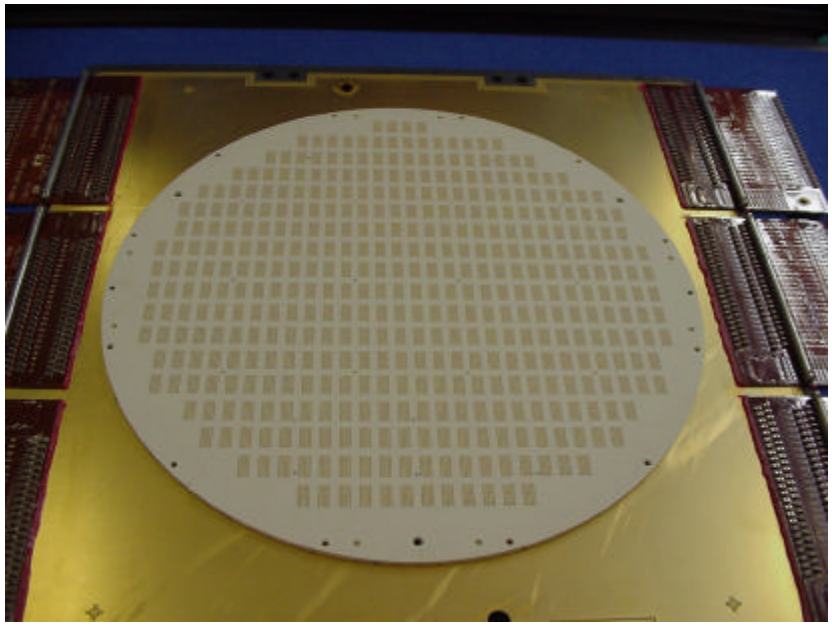
Sheet Based Z-axis Contactor

- Available in single-use or many-use sheets
- Interconnect board precisely aligned to wafer
- If sheet pattern is regular, then sheet position can be random
- If sheet is patterned, then must be aligned



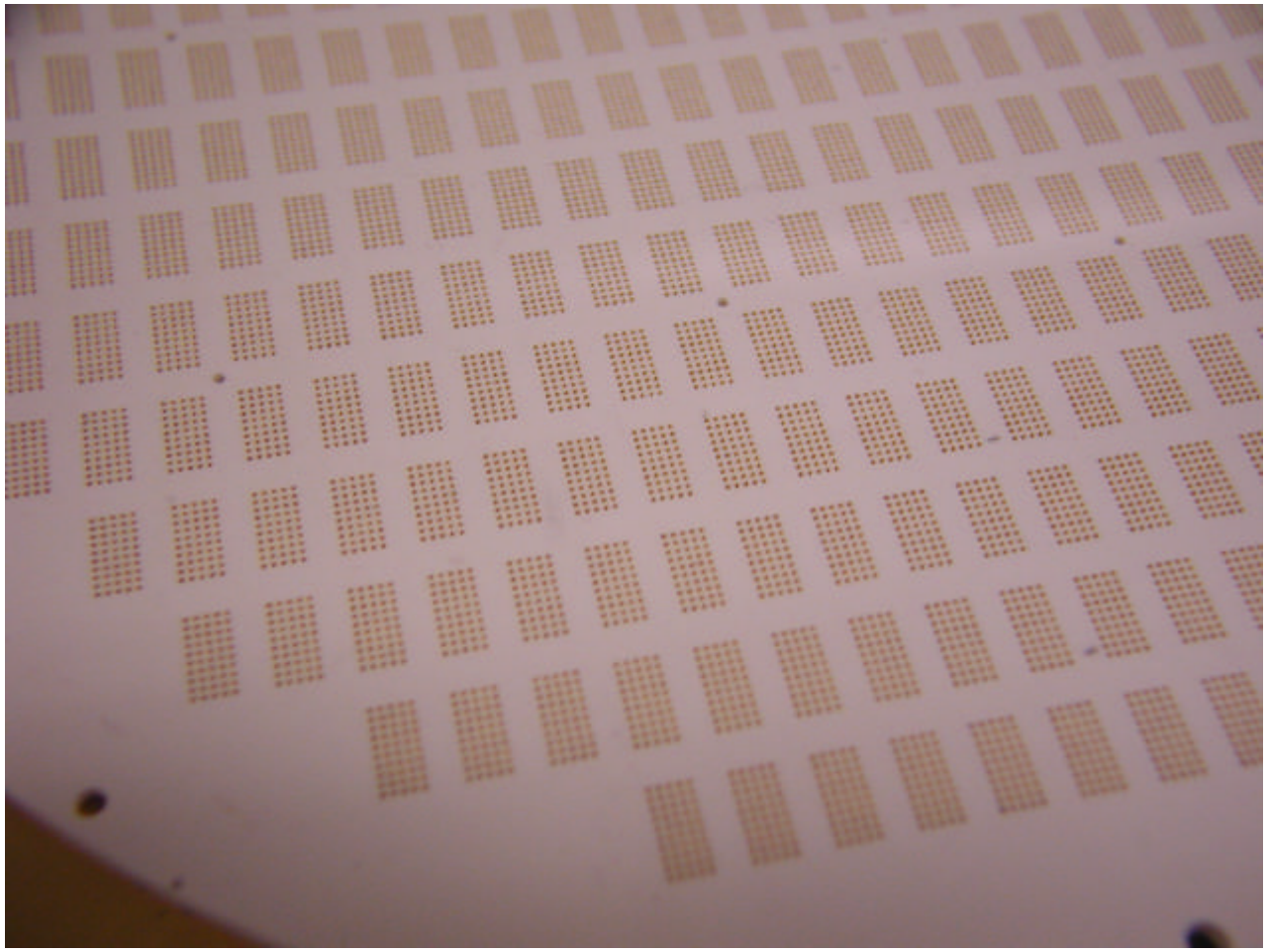


Micro Pogo Spring Contactor

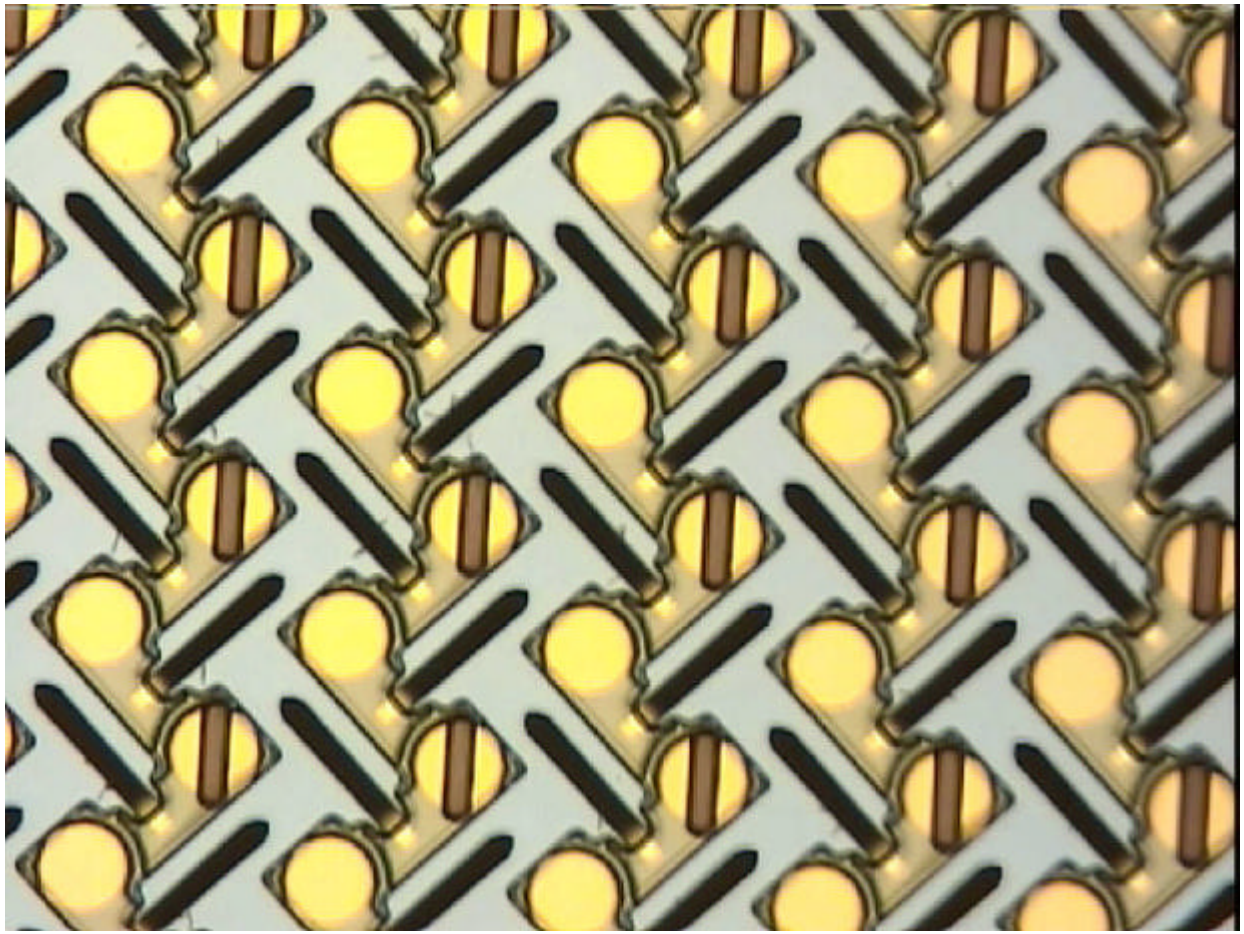


- High touchdown life
- High compliance
- Works with most pad metallurgies
- Multiple pitches available

Micro Pogo Spring Close-up



NanoSpring™ Contactor



Contactor Array
80 micron pads

Major Electrical Challenges

- How to deal with 25,000 or more signal lines
- Cannot remove bad die
  - How to deal with signal line shorts
  - How to deal with die power shorts

System Electronics

- Leverage experience in parallel test design
  - Signal lines and data lines are paralleled to vastly reduce total interconnect count between wafer and system electronics
- Individual die power lines prevent shorted die from interfering with good die
  - Capability to control & monitor power on individual die basis

Does It Really Work?

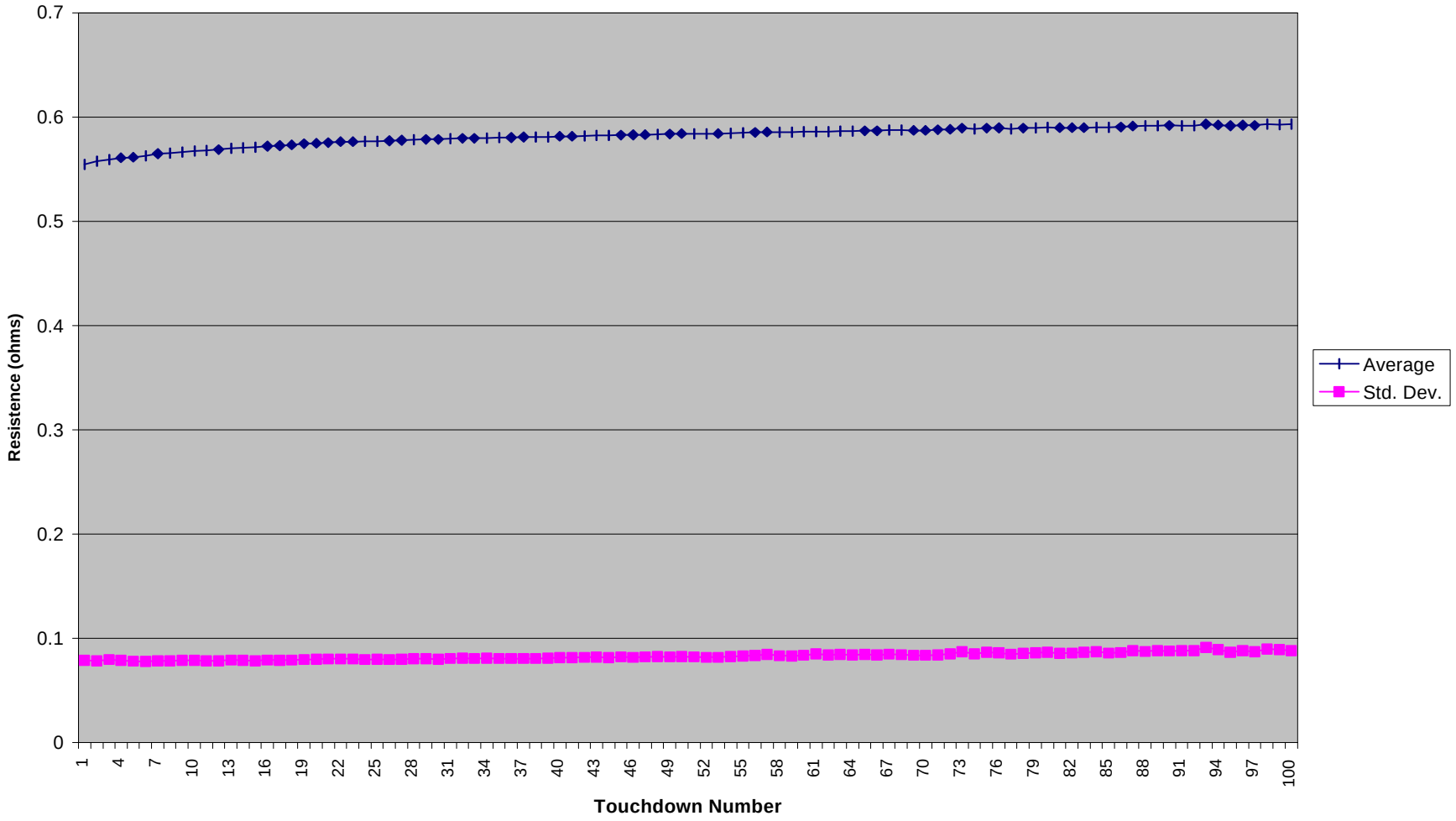
- Is Full Wafer Contact really possible?

SDRAM Wafer Map

Does It Really Work?

- Is Full Wafer Contact really possible?
- Is the contact reliable?

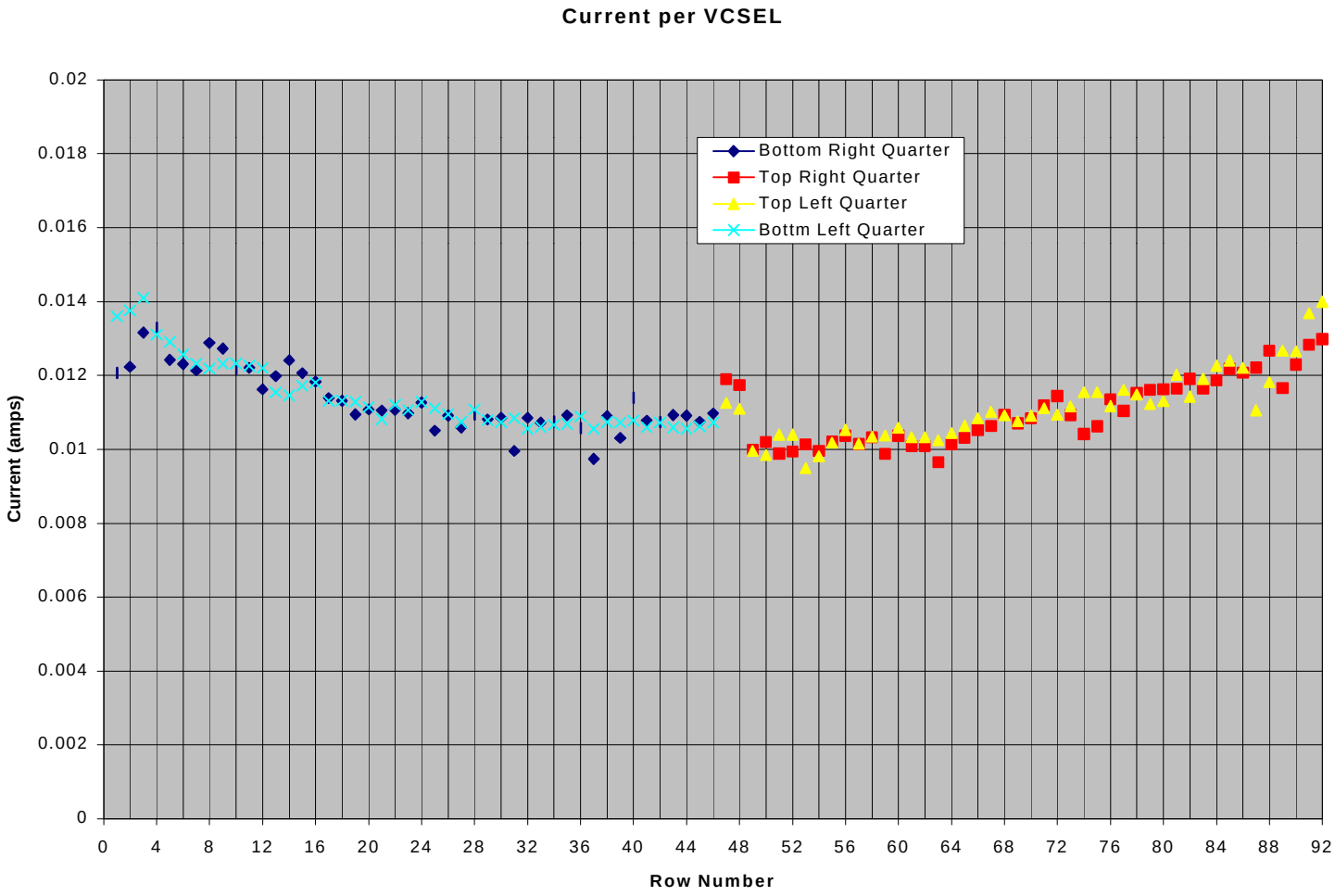
Per Touchdown Resistance



Does It Really Work?

- Is Full Wafer Contact really possible?
- Is the contact reliable?
- Can it scale?
  - Across varying wafer CTE?
  - Across varying wafer sizes?
  - Across nearly 3 orders of magnitude in force?

Laser Diode Burn-In



Full Wafer Burn & Test Status

- Took longer than expected
- Many technical barriers
- Has been demonstrated across
  - Wafer sizes from 2” to 8” (300mm shortly)
  - Different wafer types (CTE)
  - SDRAMs to VCSELs (Laser Diode)
  - Different pad metallurgies
  - Widely varying contactor technologies

Full Wafer Burn & Test Has Arrived

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