High Throughput Challenges for 300mm Wafer Testing

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Agenda

- Overview
  - Test Equipment Introduction
- 300mm Prober Challenges
  - Thermal and Probing Issue
  - SACC Cart
- TRE Probe Card challenges
  - Electrical Performance
  - Mechanical Performance
- Summary
- Acknowledgement

Overview

DRAM mass productions are shifting toward 300mm. Reducing testing cost is the major concern of Test Engineering. PSC, FFI and TEL have cooperated to implement for 300 mm DRAM test.

Tester Resource Extension (TRE) probe card has doubled the tester parallel testing capacity to 128DUT/station testing.

In our paper, we will give an overview of the project to implement 128DUT wafer test at PSC.

Powerchip Semiconductor Corp.

PSC Fab Overview

	Fab I	Fab II
Facility	8"Fab	12"Fab
Cleanroom Space	11,000 sqr. meters	14,000 sqr. meters
Cleanness	Class 1	Class 100T
Mass Production Time	Oct. 1996	Oct. 2002
Full Monthly Capacity	40,000 wafers	35,000 wafers
Process Technology	DRAM-0.165/0.15um Logic-0.18/0.15/0.13um Flash-0.25/0.18/0.15um SRAM-0.18um	DRAM-0.13um and below

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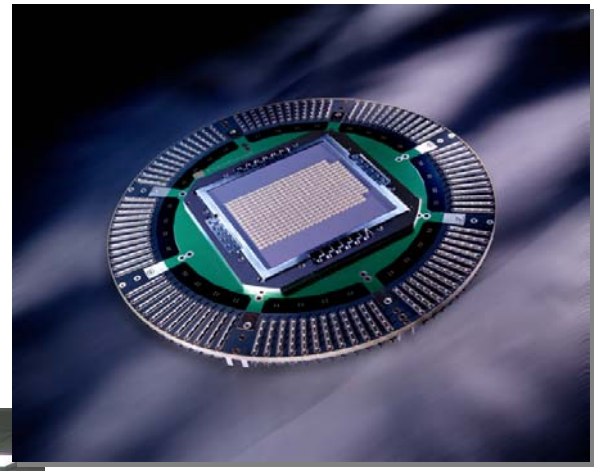
Testing Equipment Introduction (1)

TEL Prober
P-12Xln

Advantest Tester T-5375



FFI Probe Card
PH100 / 128DUT

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Testing Equipment Introduction (2)

Tester

DR : 2048 Pins / 64DCTU / Station
I/O : 1280 Pins / 256PPS / Station

Prober

Pin to pad XY +/- 2um
Pin to pad Z +/- 5um
SACC CART

Probe card

128DUT TRE Probe Interface
Number of Probe > 6000Pins
XY Positioning Accuracy < 20um
Probe Head : PH100

TRE probe Interface has doubled parallel testing capacity from 64DUT to 128DUT/station testing.

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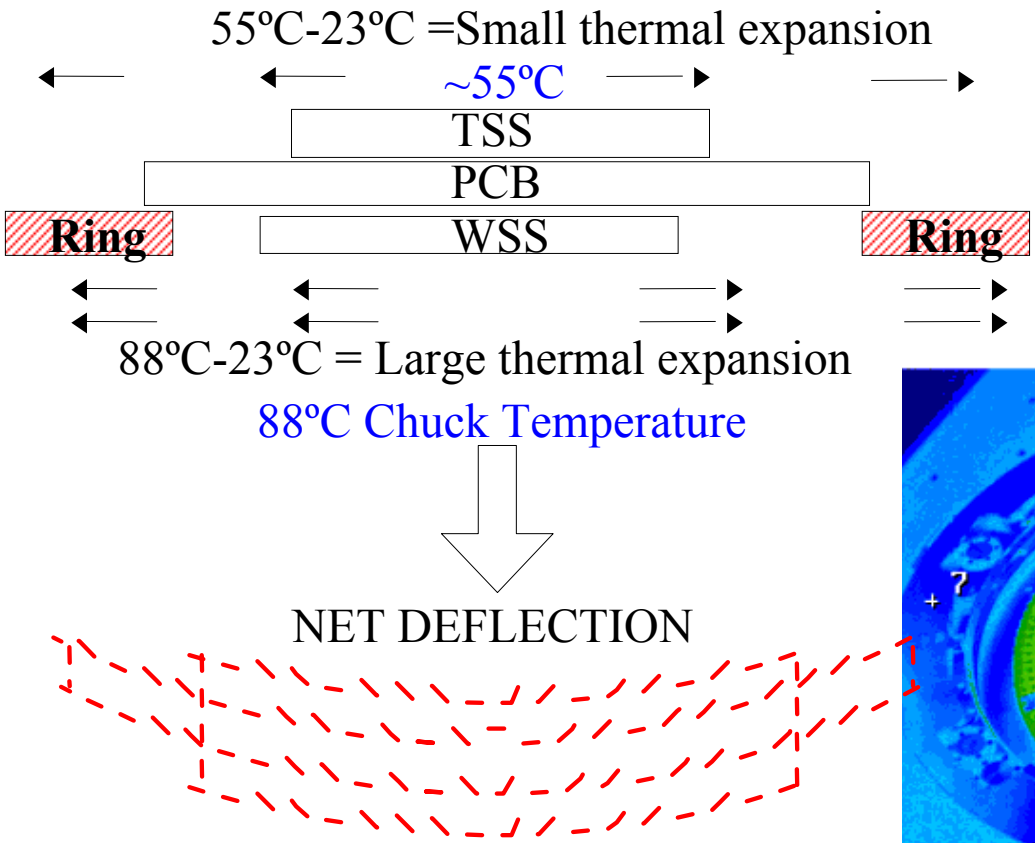
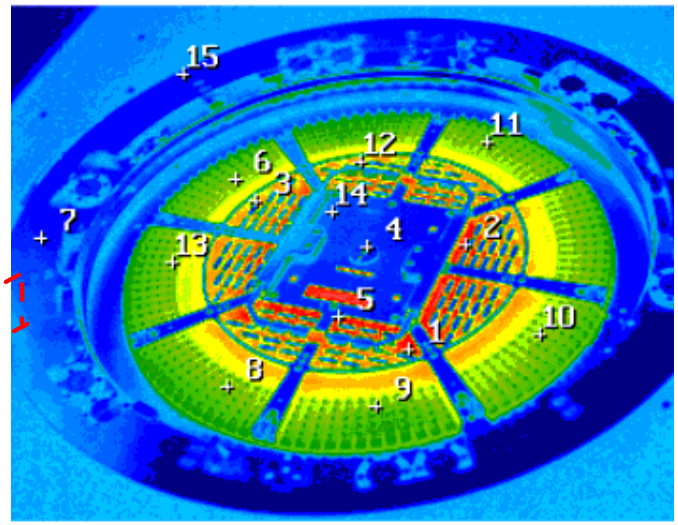
Problem : Thermal Z-Deflection of Probe Card





Effect: Long Per-heat Time and Unstable Probe Mark

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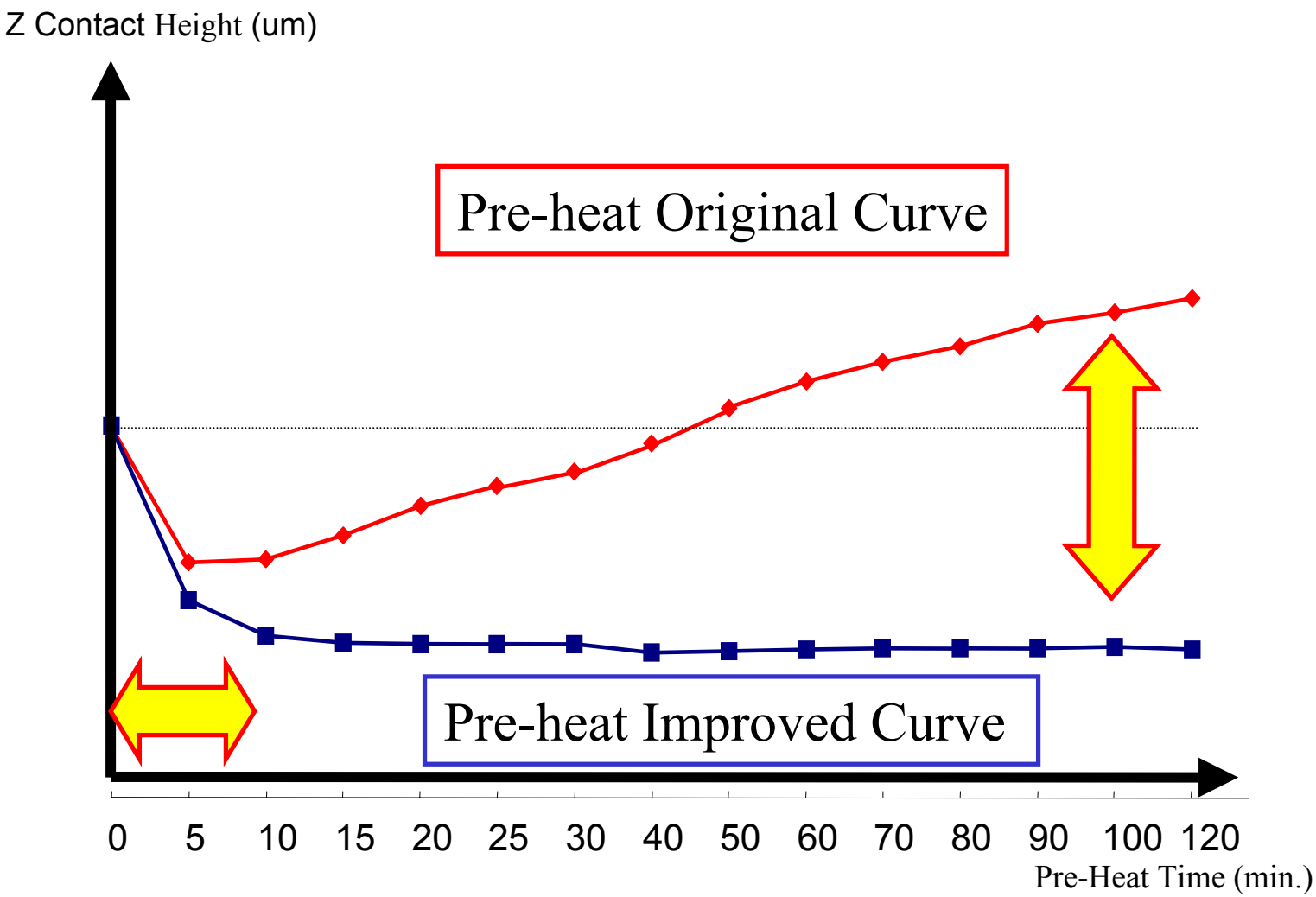
Throughput Improvement & Stable Contact (1)



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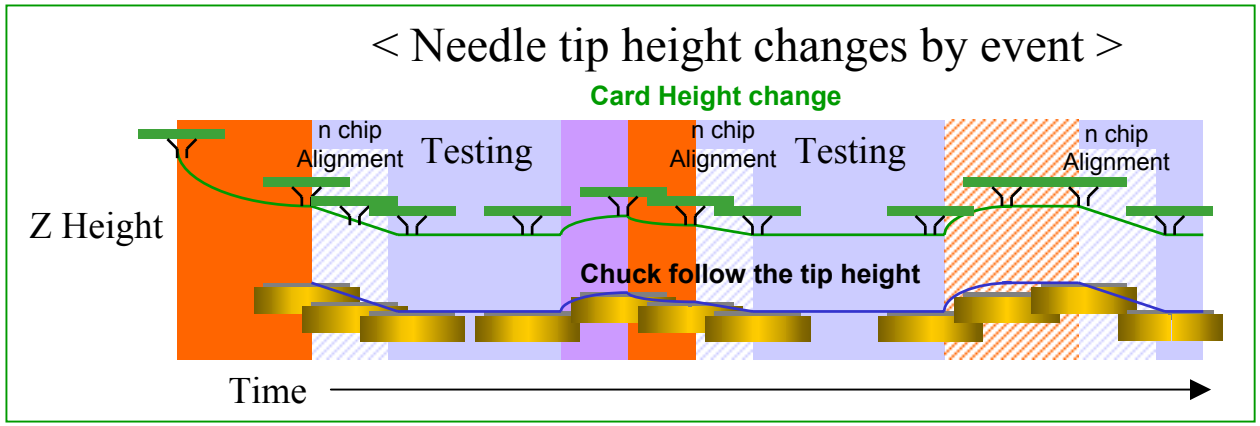
Throughput Improvement & Stable Contact (2)

- **Effort 1** : **New WSS**
- **Effort 2** : **New P/C Card Holder Concept**
- **Effort 3** : **P/C Card Holder Controlling**
- **Effort 4** : **New Pre-heat Method**
- **Effort 5** : **Throughput Improvement Sequence on Prober**
- **Effort 6** : **N-Chip Alignment (Smart Soak)**



Conclusion:

- **Pre-heat time improved**
- **Idle time reduced**
- **Probe mark more stable**
- **Re-create contact height by each index based on tip position**

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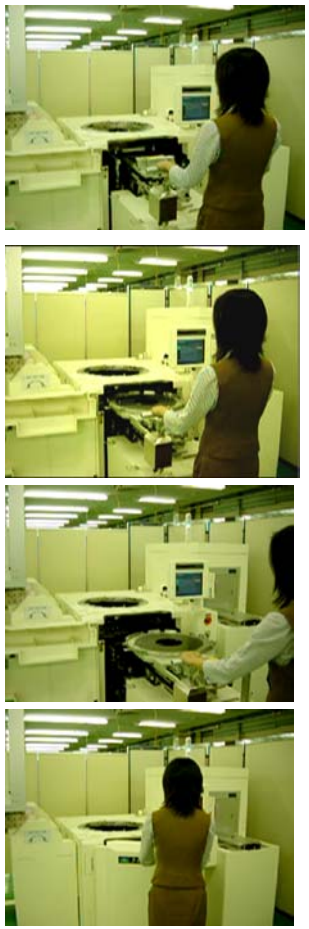
SACC Cart Safe Operation



Safely Secured – Uses Minimum Operator Space
Contributes to using a floor space efficiently

- Safe for operator (Bigger, heavier, longer distance)
- Safe for heavy, expensive probe card
- Improved throughput including floor operation
- Remove low usage option from each stage
- C.O.O down

Remove SACC unit from each prober loaded to CART

Operate few SACC CARTs for entire test floor

SACC CART

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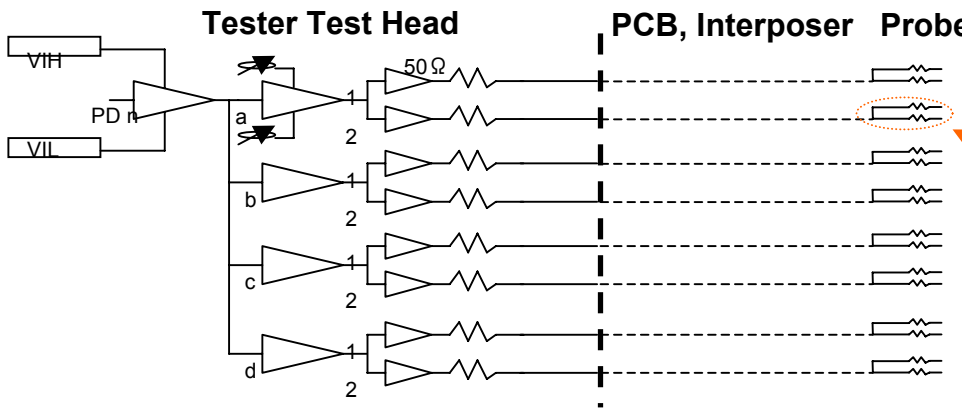
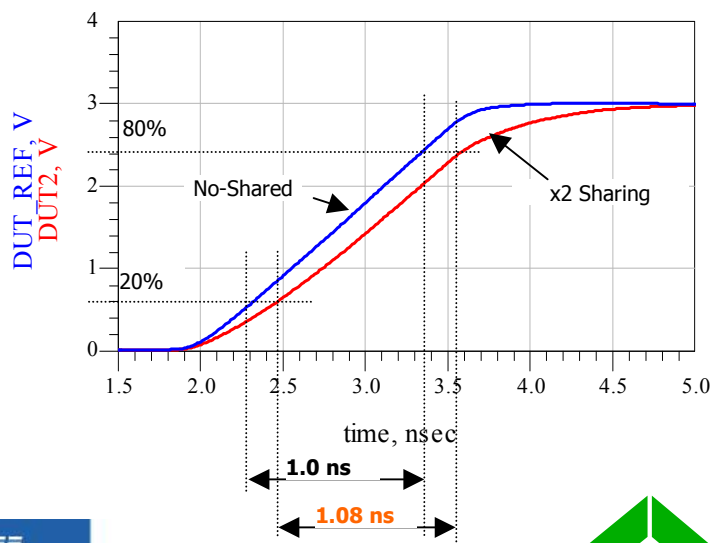
128 DUT Probe Interface Electrical Performance Driver Tr/Tf Input- 66 MHz, x2 Sharing

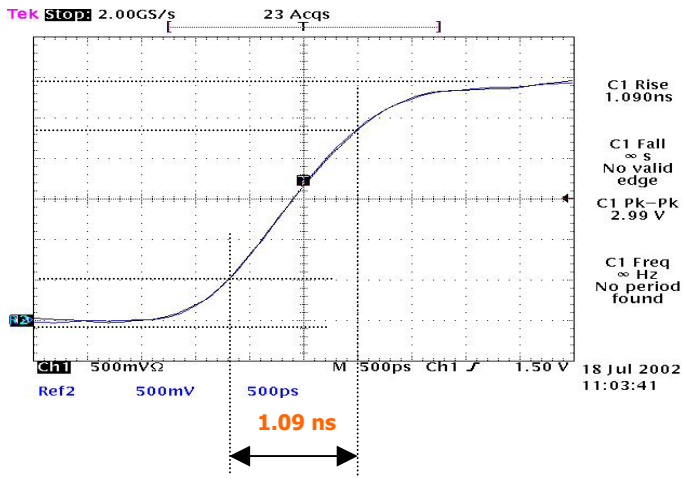


Branched Trace Length Less Than 10 mm In Probe Head

Simulation



Measured Waveform



Measured at Spring

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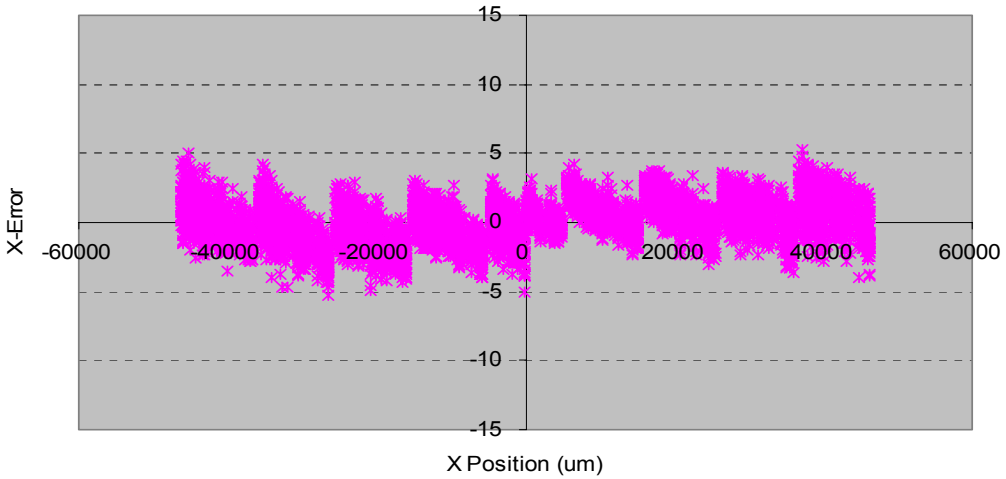
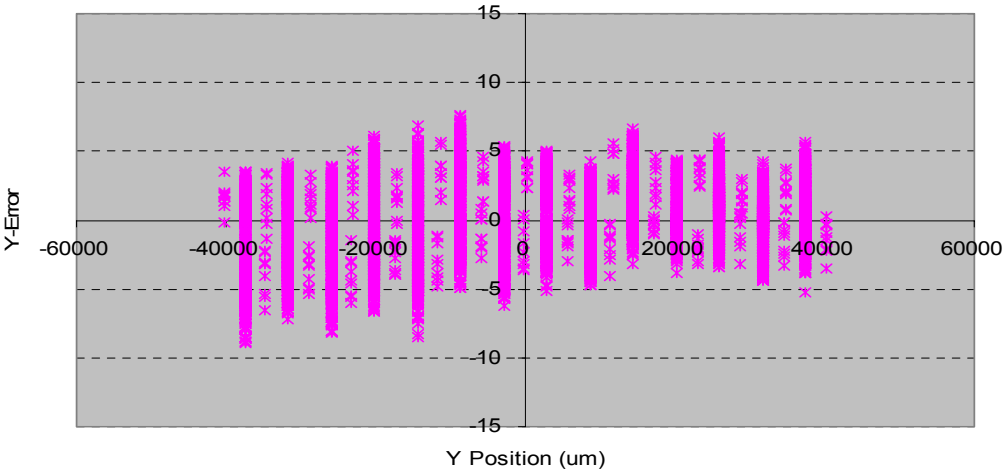
128 DUT Probe Interface Mechanical Performance Scrub Positioning

X-Error (um)
<+/-5um



Y-Error (um)
<+/-8um



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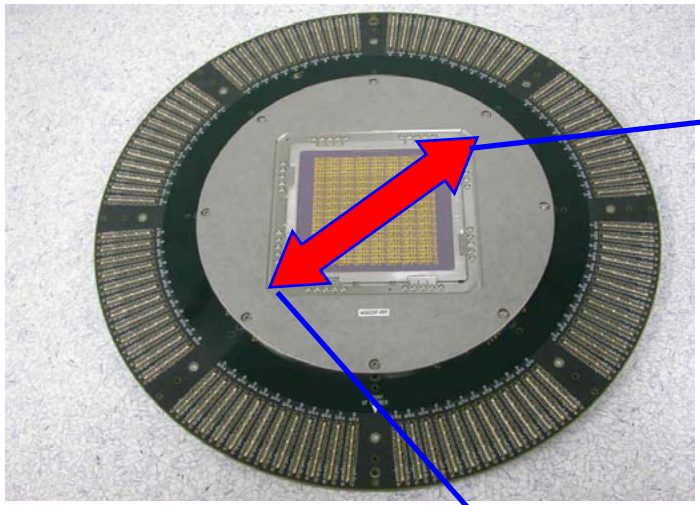
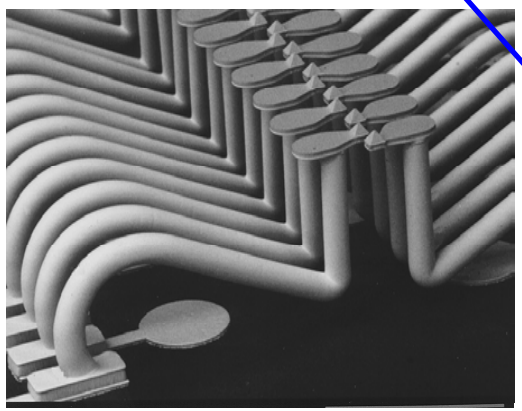
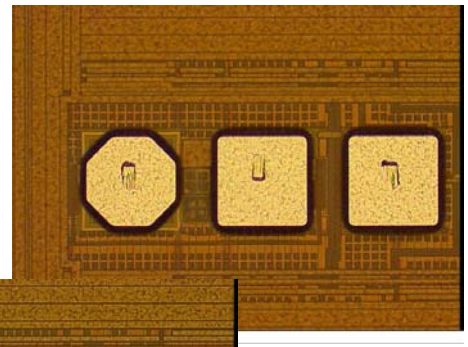
128 DUT P/C Probe Mark & Tip

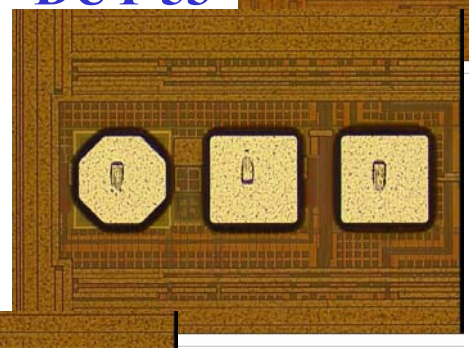




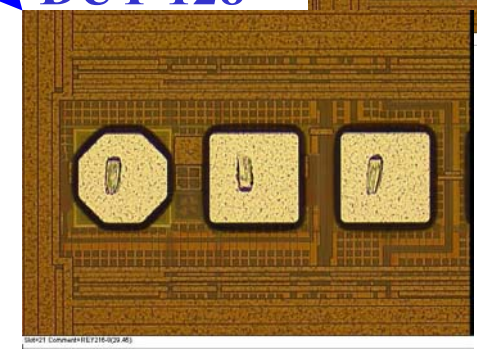
DUT 1



DUT 53



DUT 128



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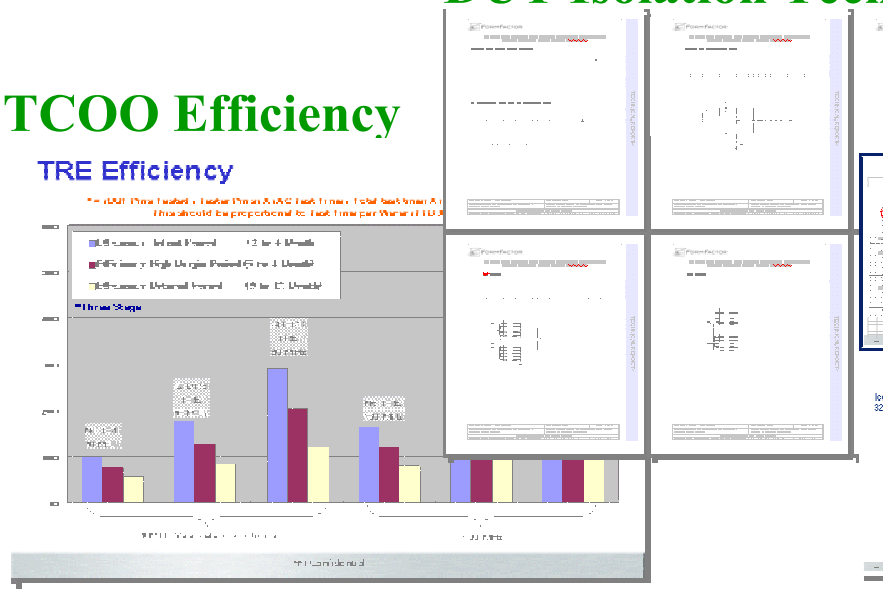
FFI High Performance Probe Interface

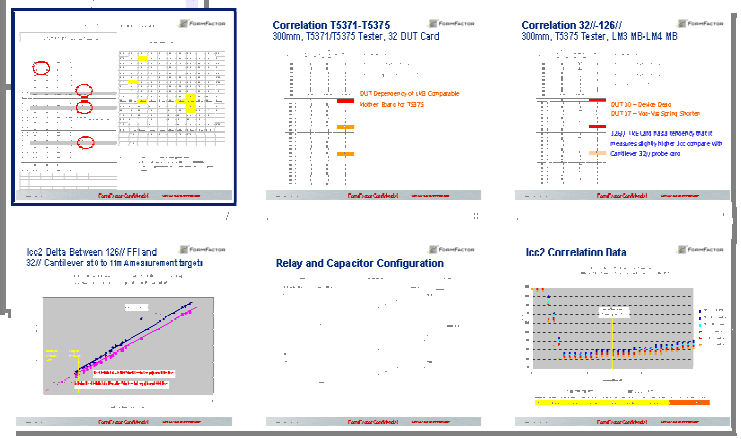
- Touchdown, Parallelism Optimization
- Test Methodology Consultation
- Hardware/Software Solution
- Onsite Implementation/Integration Support

DUT Isolation Techniques

TCOO Efficiency



Test Program Optimization



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Summary (1)

PSC TRE Project

1) Manpower: PSC 6 Engineers, FFI 5 Engineers, TEL 40 Engineers
2) Cost: >$US 2.85 Million
3) Time: ~15 Months

PSC TRE Project effective

1) Throughput : 120DUT > 1.6 X 64DUT
2) Save more Test Equipment, Manpower, Space Cost

Summary (2)

Future Challenge:

1) Device / Pad / Pitch Shrink

2) More Accuracy Contact

3) New Material Development

4) Cleaning Technology

5) High Speed or High Parallelism Testing

Summary (3)

FFI, as Solution Provider, contributed this project providing:

- High Performance High Parallelism Probe Interface
- Test Methodology and TCOO Reduction Consultation
- Effective Implementation/Integration Service

TEL

- Maintain Pin To Pad (XY and Z) Contact Accuracy with High Parallelism Under All Thermal Conditions
- Provides Total Solution for Test Cell and Operations (Operator, Probe Card, Test Result)
- Co Development Work With Customers to Encompass All Applications and Roadmap Requirements

Acknowledgement : Special Thanks

PSC

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