Multi-site Probing for Wafer-Level Reliability

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Outline

- Introduction
- Multi-Site Probing Challenges
- Multi-Site Wafer Level Reliability Examples
  - TDDB
  - NBTI
- Conclusions

Traditional Reliability

- Long-term reliability is often equated to packaged parts tests
- Predictive of lifetime which is the key for designers
- Slice the wafer; package the devices; apply the stress in a special oven
- Packaging a wafer requires time, and several steps at extra cost
- Separate packaging handling operations may introduce damages and limits the number of available pins
- Spatial correlation is often lost
- If a lot of wafers is “defective” you have to do it all over

Wafer Level Reliability

- On-wafer does not require extra steps and is immediately available!
- On-wafer differentiates damage introduced by packaging operations!
- Spatial correlation is preserved!
- As oxides become thinner the effects of packaging damage due to ESD are unknown. ESD effects on new gate materials are unknown
- Cu difficult to bond. In general, for interconnect reliability additional Al bond pads are required

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Multi-Site Probing Opportunities

- Stressing many devices at the same time, or
- Devices can be grouped in categories, thus stress groups of devices can be created
- Different oxide thickness, or device types, can be stressed at the same time
- User defined parameter tests pre- and post-stress, can be achieved individually or by group
- Instrumentation and software are required to have features to manage multiple devices and conditions

Instrumentation

- Voltage measurement resolution 2 μV and forcing voltage resolution 100μV
- Current measurement resolution 10fA and force current resolution 50fA
- Switching Matrix < 0.1pA leakage per channel and fast switching times
- Support matrix or multiplexor cards

I. Software

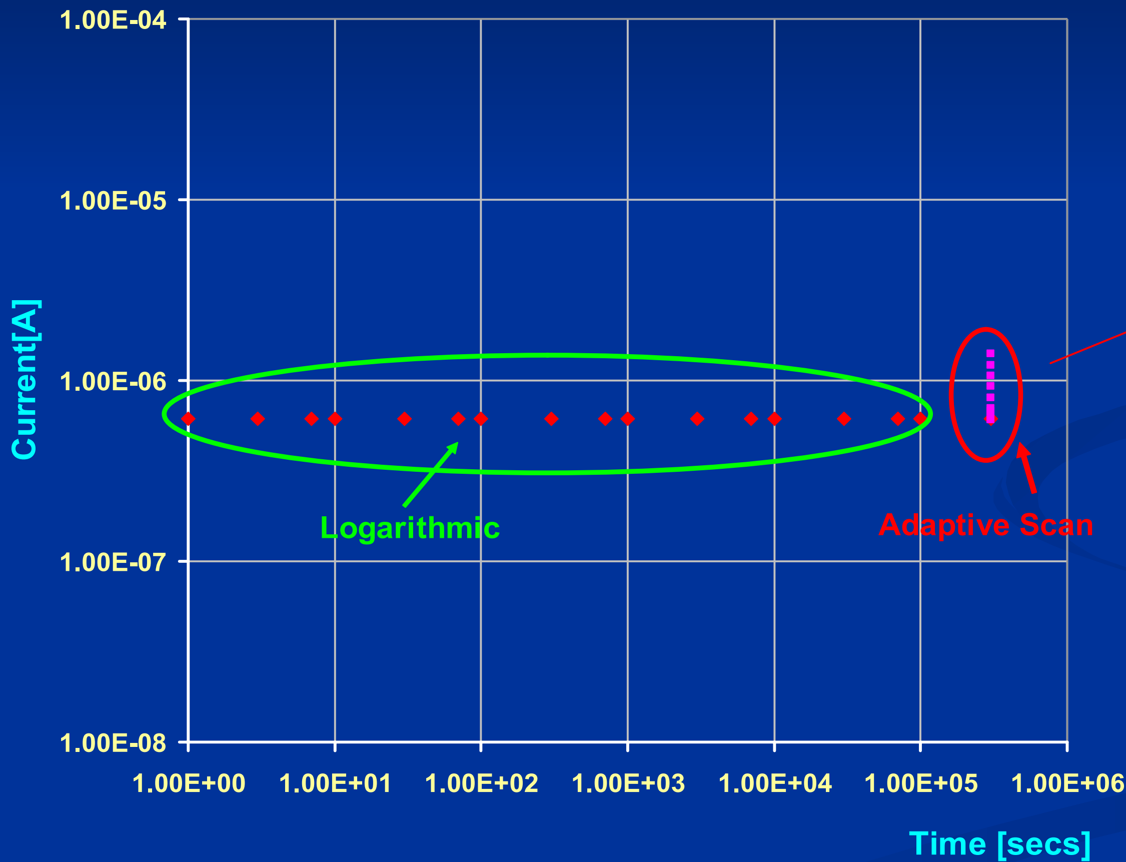
- Traditional package level testers can group test hundreds of devices, however because the number of devices and tester architecture their scan time can be in hours
- Software must scans in milliseconds to determine the exact time to breakdown, or NBTI phenomena, etc
- Prevents relaxing the devices under stress. This is, the devices are always under stress, unless they are being measured
- Each DUT may be stressed individually, or devices grouped in multiple sets

II. Software

- Effectively the system has a per-pin architecture
- Scanning can be linear, logarithmic or the intelligent, rules based, Owl Adaptive Scan™
- The intelligent Owl Adaptive Scan™ changes the scan frequency as device parameters change, thus breakdown, or other phenomena, can be accurately determined

Adaptive Scan™

- Owl Adaptive Scan™ adapt to changes in the device behavior and can determine soft breakdown



TDDB

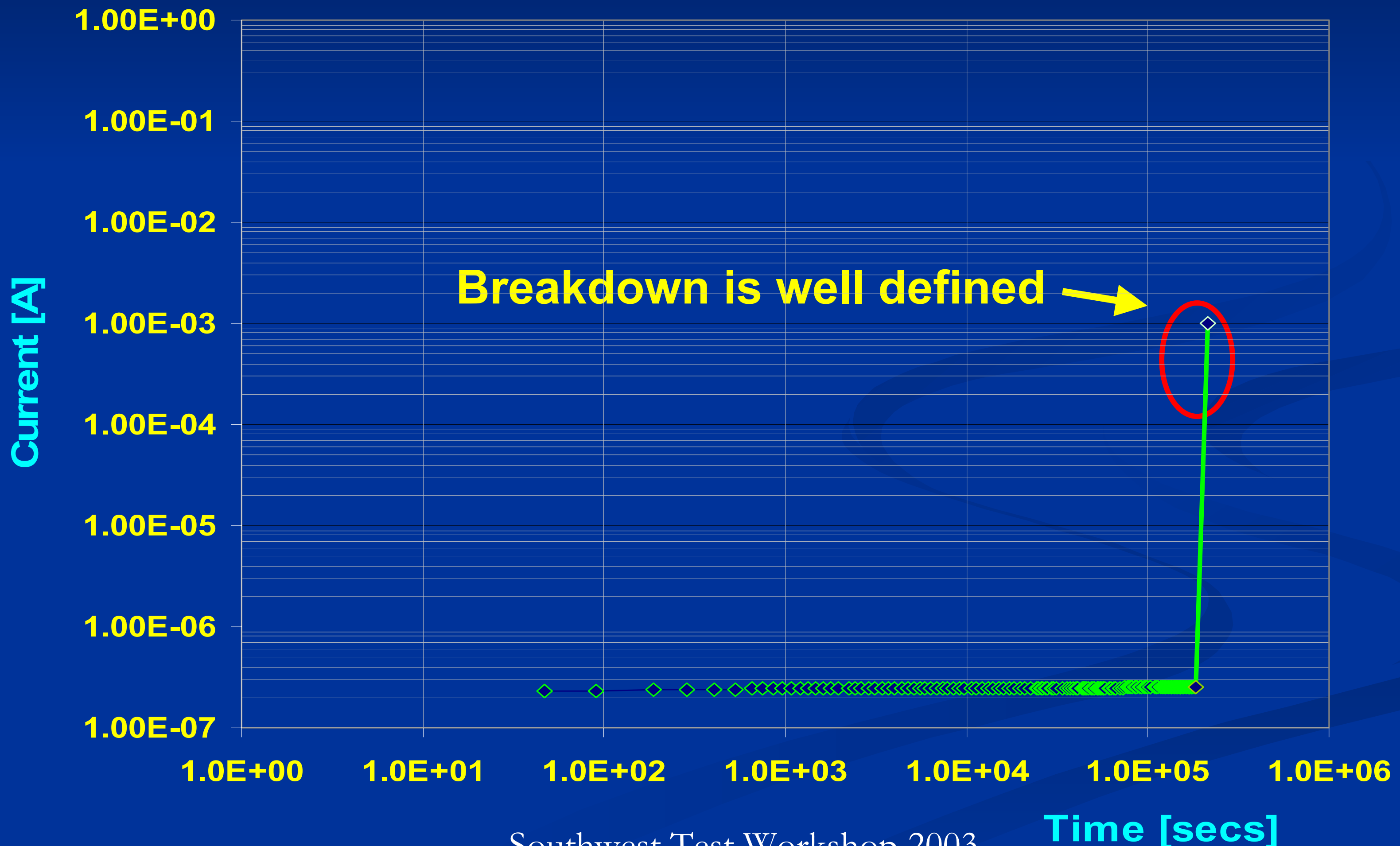
- For oxides > 4nm oxide breakdown and breakdown model is well understood.
- For oxides <4nm there is a need to determine
  - What is breakdown?
  - How do you model it?

Oxide Breakdown

- For thick oxides there is a clear breakdown.
- Thin oxide breakdown is not clearly defined
  - There is a soft breakdown
  - Self annealing effect?
  - How do we define this breakdown and how do we determine it experimentally?

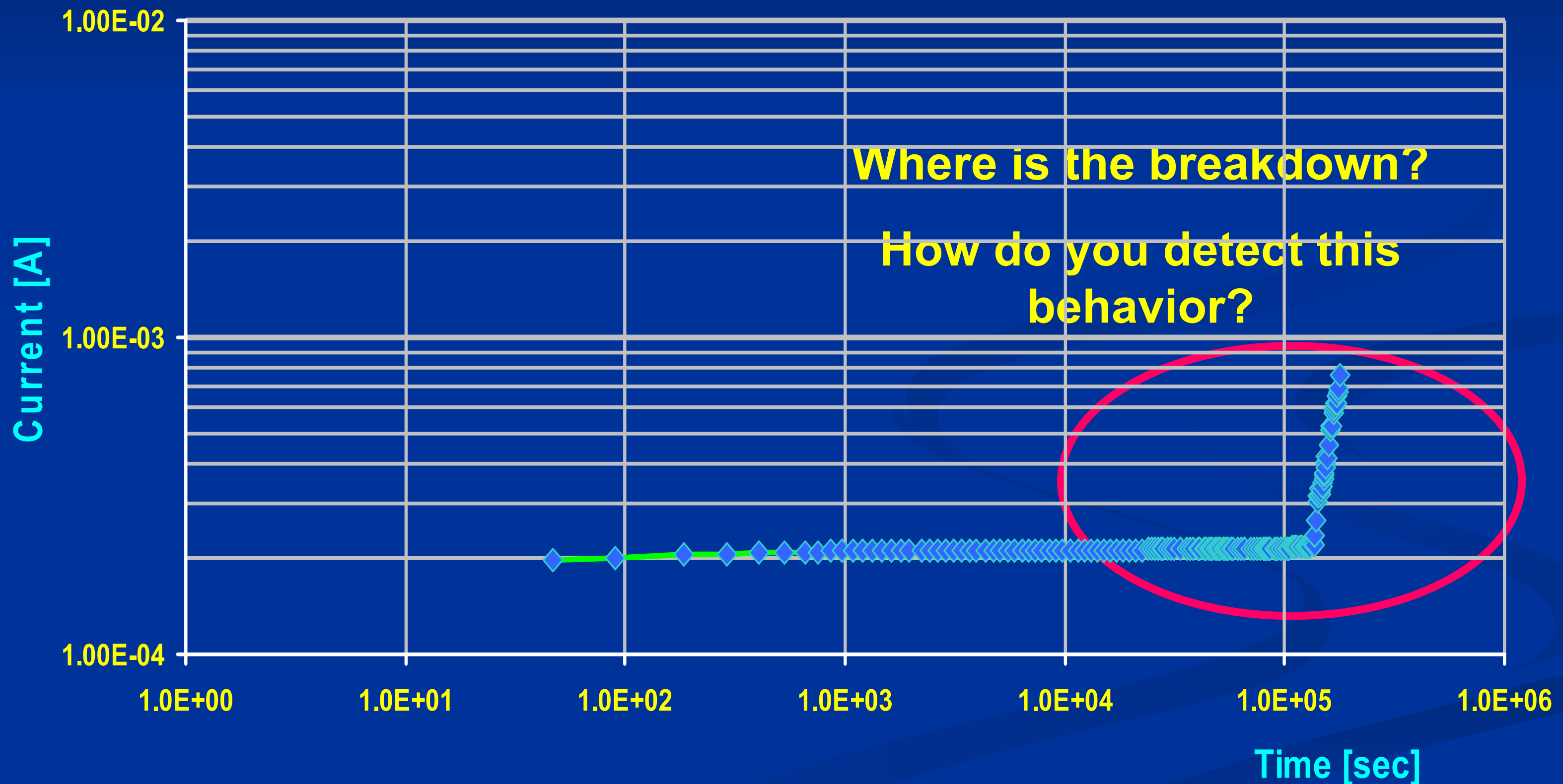
Thick Oxide Breakdown Behavior

- Thick oxides have a "hard" breakdown

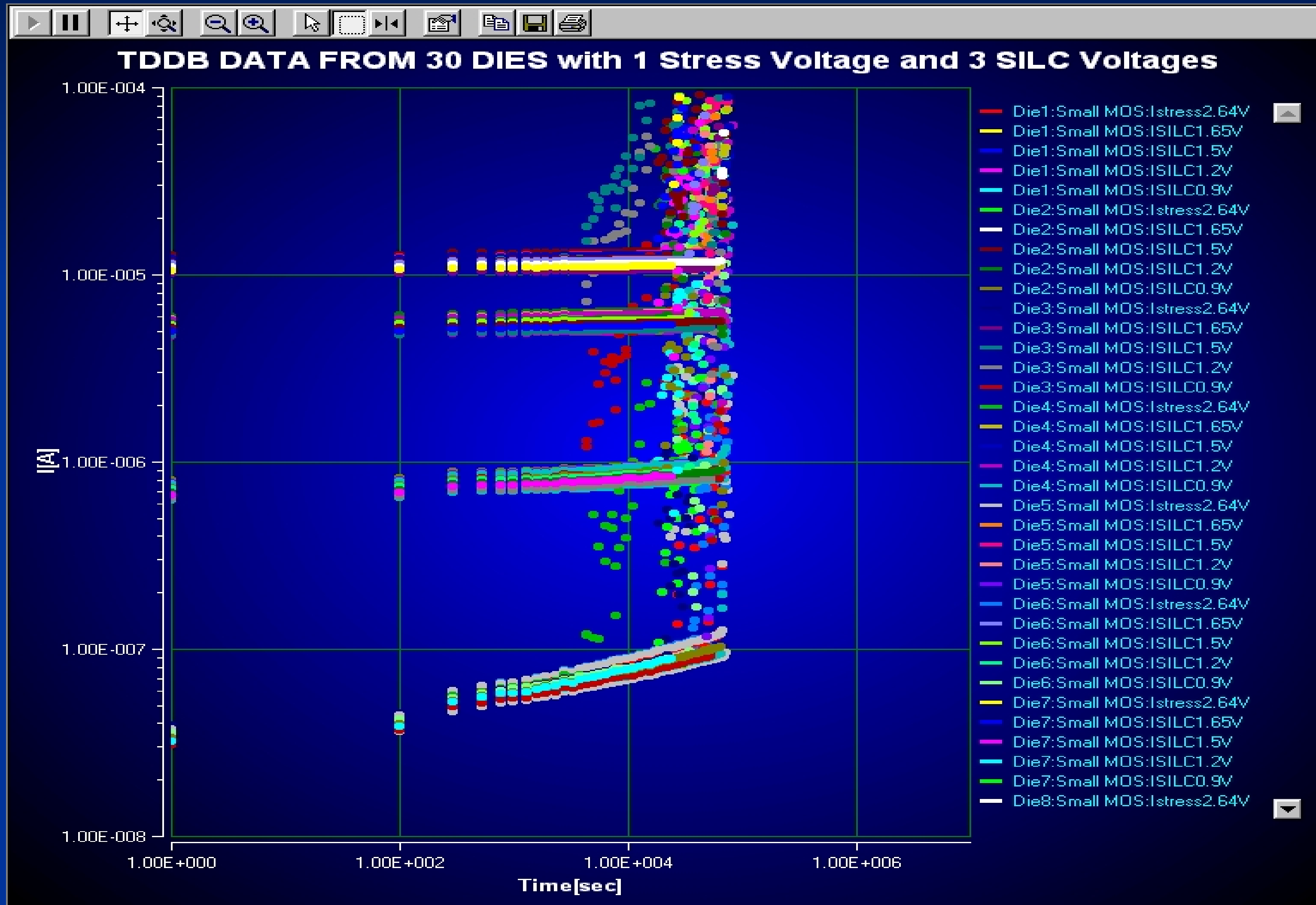


Thin Oxide Breakdown

- In thin oxides the breakdown is not well defined and the challenge is to detect this atypical behavior

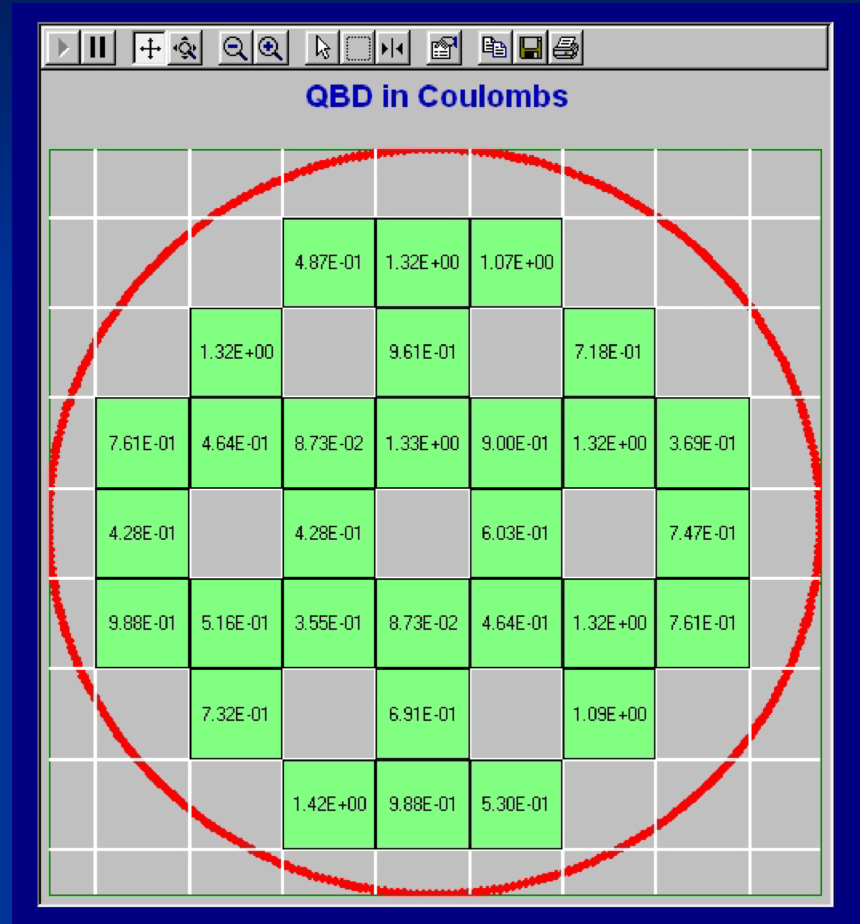


TDDB Data From Multi-Probe



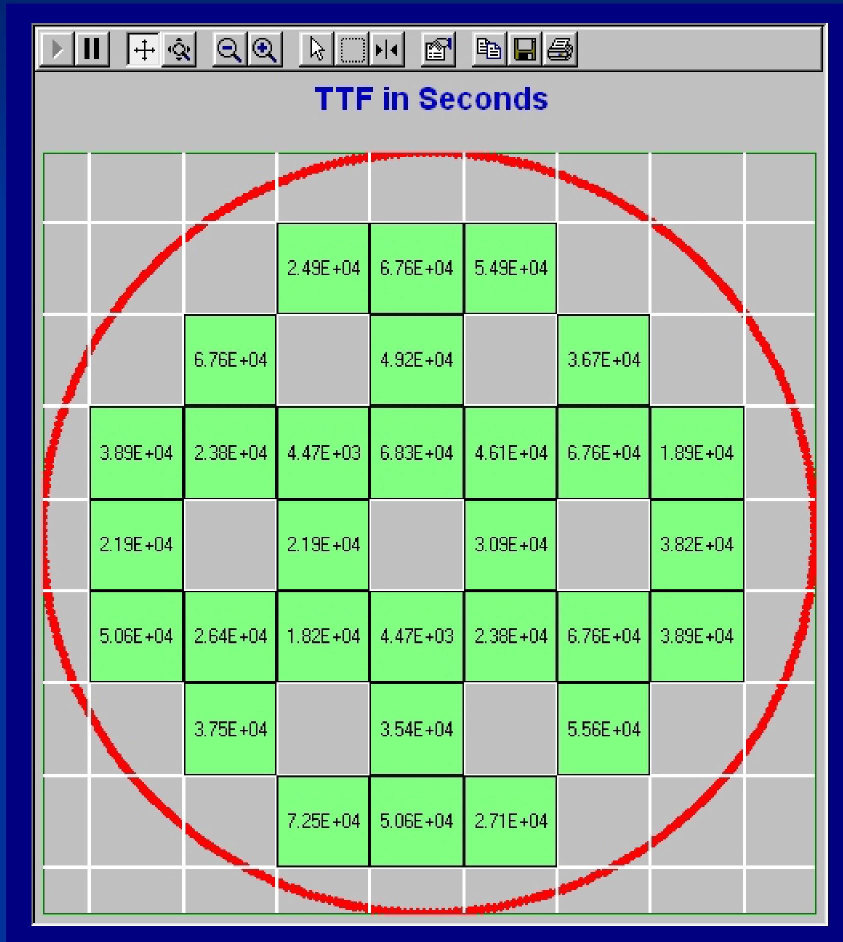
QBD

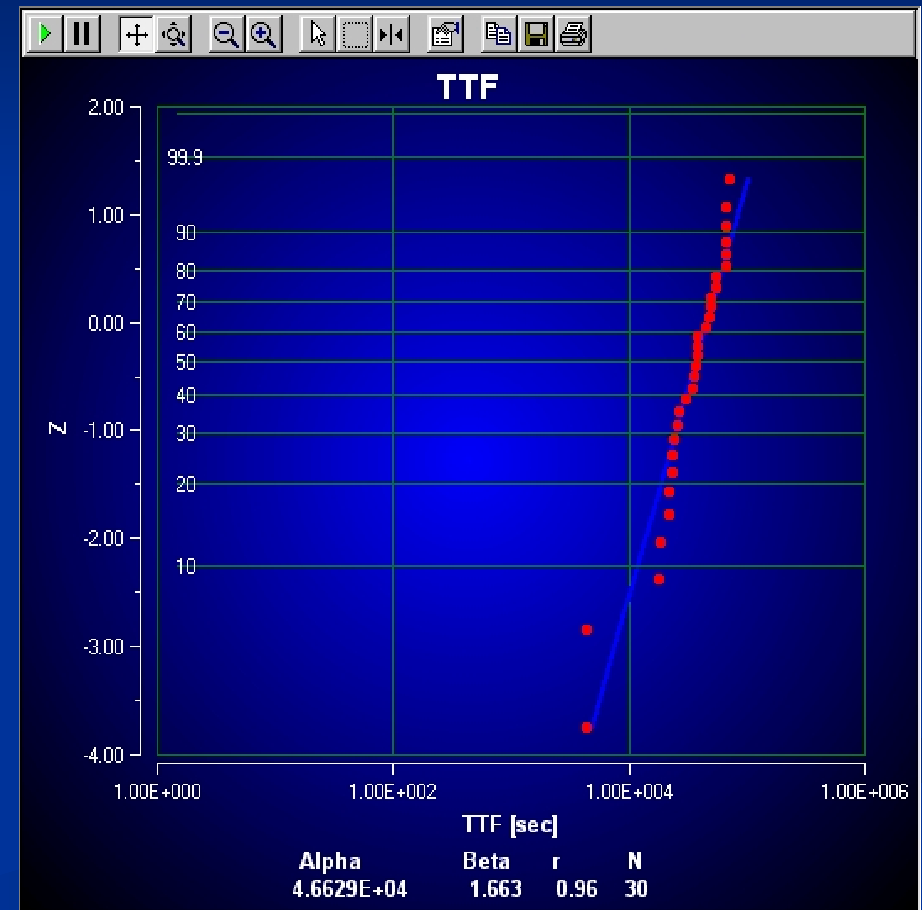
- Spatial resolution is preserved
- Weak dies, if present, can be located immediately
- Further analysis can be done to verify the causes of early failure



TTF wafer map and Weibull Plot

- Spatial resolution and statistical data is obtained at the same time





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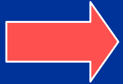

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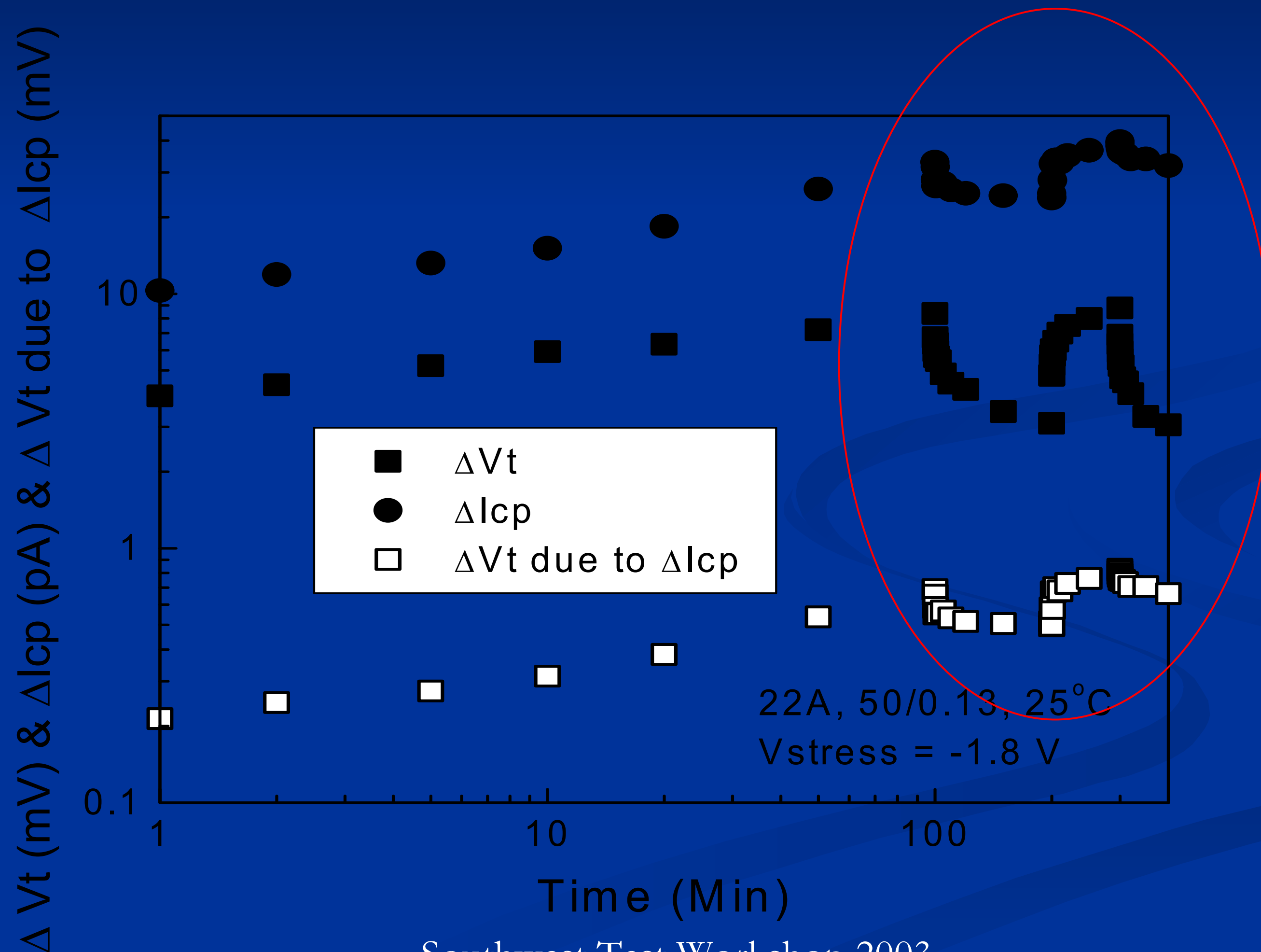
NBTI Measurement Issues

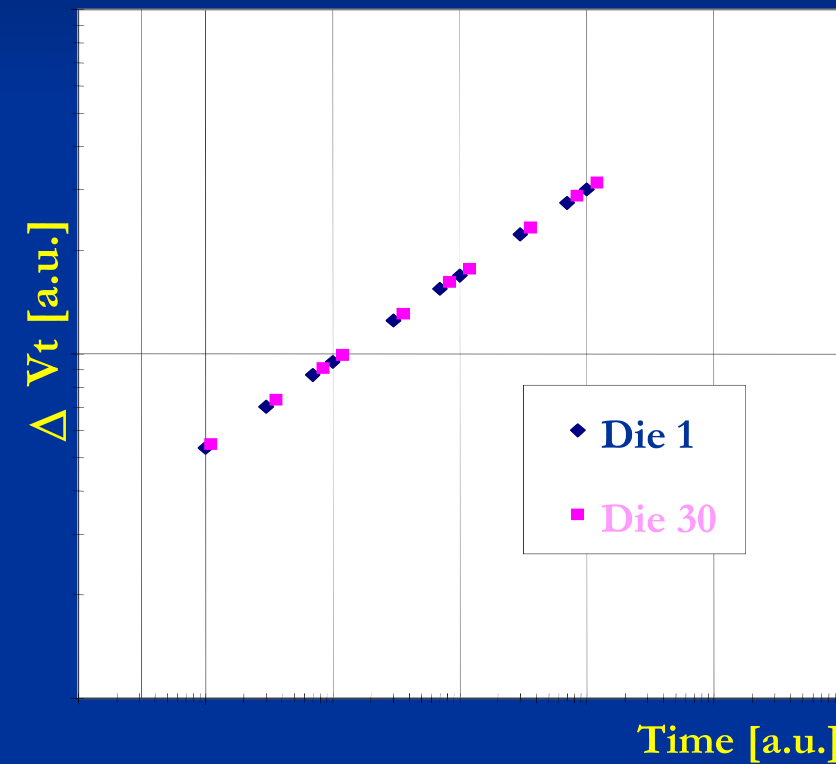
- NBTI is a mechanism that degrades PMOS devices
- Removing stress can recover the device
- Recovery time is very short
- In actual circuits devices may not recover, however during measurements:
  - If the instrumentation is not fast enough then it will give false information

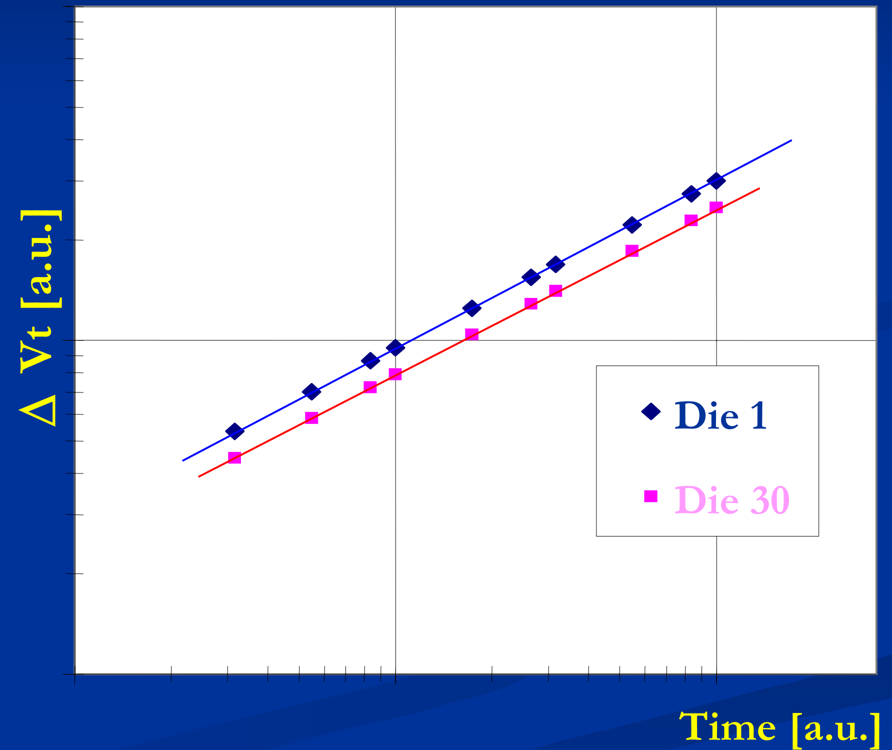
STUDY OF Sub-Quarter-Micron PMOSFET NBTI UNDER DC and AC STRESS

Erhong Li, Sharad Prasad, Sangjune Park and John Walker ,PV2003-06 p408 Electrochemical Society Proceedings, Paris 2003



Stress Relaxation Effect in NBTI





I. Conclusions

- In this presentation we have highlighted several advantages and opportunities of multi-site wafer level probing for reliability measurements
- Multi-site wafer level probing offers the distinctive advantage of rapidly and accurately characterize new materials or products.
- A challenge for multi-site probing is to have and properly configure equipment and software to take full advantage of the architecture
- Actual measurement times must be in milliseconds

II. Conclusions

- System must avoid relaxation effects
- It is key to design an appropriate probe card pattern for testing multiple sites common to several tests, and schedule tests to maximize probe card test coverage
- Multi-site probing offers exciting challenges, but great benefits, to characterize new materials or products and predict accurately their reliability:
  - e.g TDDB: In one touchdown is possible to measure and calculate the Voltage Acceleration factor, Γ
- Probe card and prober should must be able to withstand high temperatures for a full characterization set

User Interface