MEMs Technology in Testing

Richard Chuang

Sales Manager

SCS Hightech Inc.

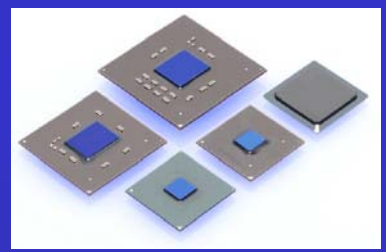
Overview:

1. Where are we ?
2. Core Technology
3. accipiter® Structure
4. In the real world
5. What's next?

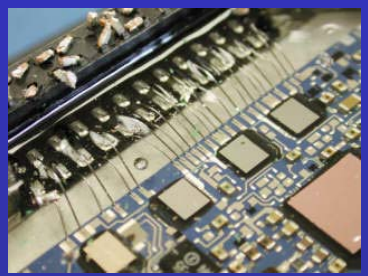
Where are we?!

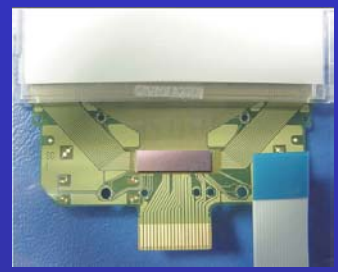
Technical Trend

- **Package**
  - Lighter / Thinner/ Shorter/ Smaller
- **Performance**
  - Higher Speed/ Lower power
- **Process**
  - Smaller Geometry / Smaller reliability margin



Flip Chip
MCM
Direct Die Attach (COB)





Final test on Wafer Level

Core Technology:

Micro Tip Process

MEMs & Integration….

- Advanced die testing
- Better Reliability
- Economical Manufacturing

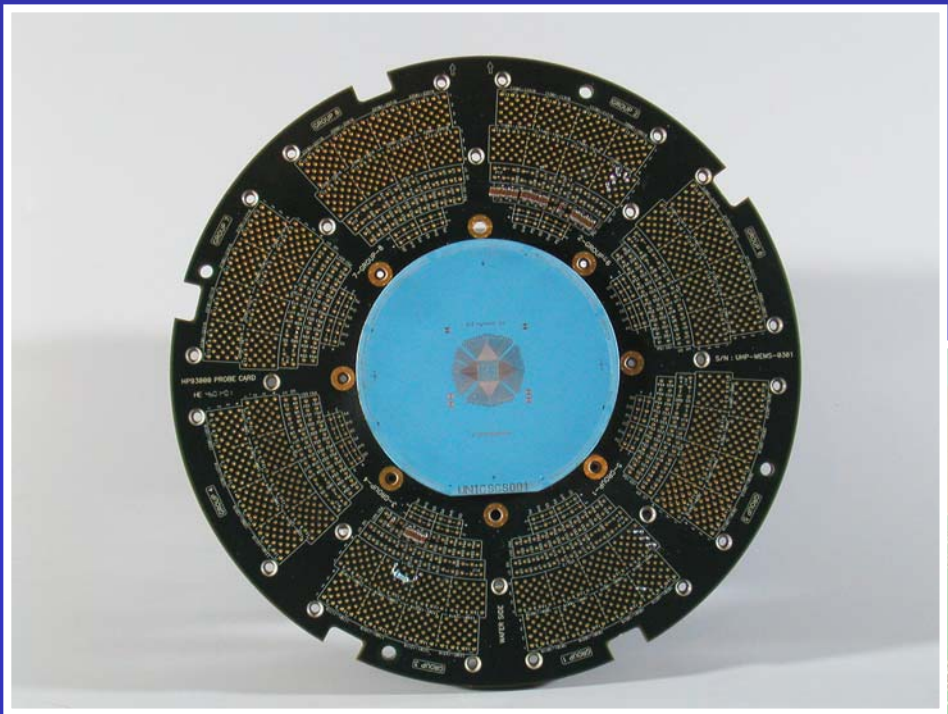
Ceramic Technology

Ultra LTCC …

- Multiple Layers
- High Vias
- Large Areas
- Extreme Flatness
- CTE Factor
- Bandwidth

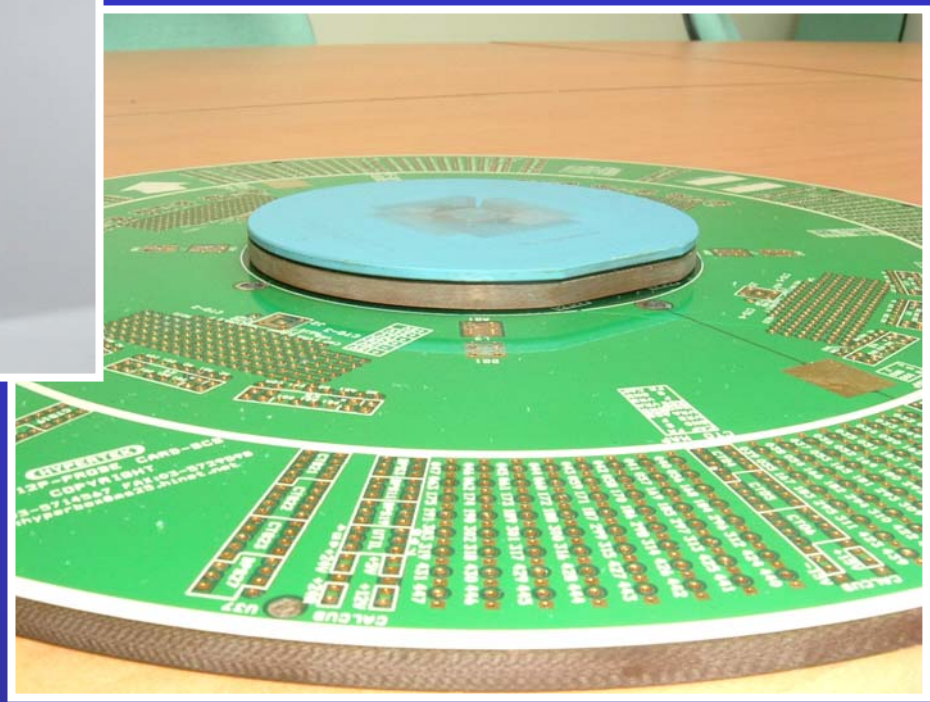
**Low Temperature Co-fire Ceramic is co-fired at 900 C*

1. accipiter® Structure:

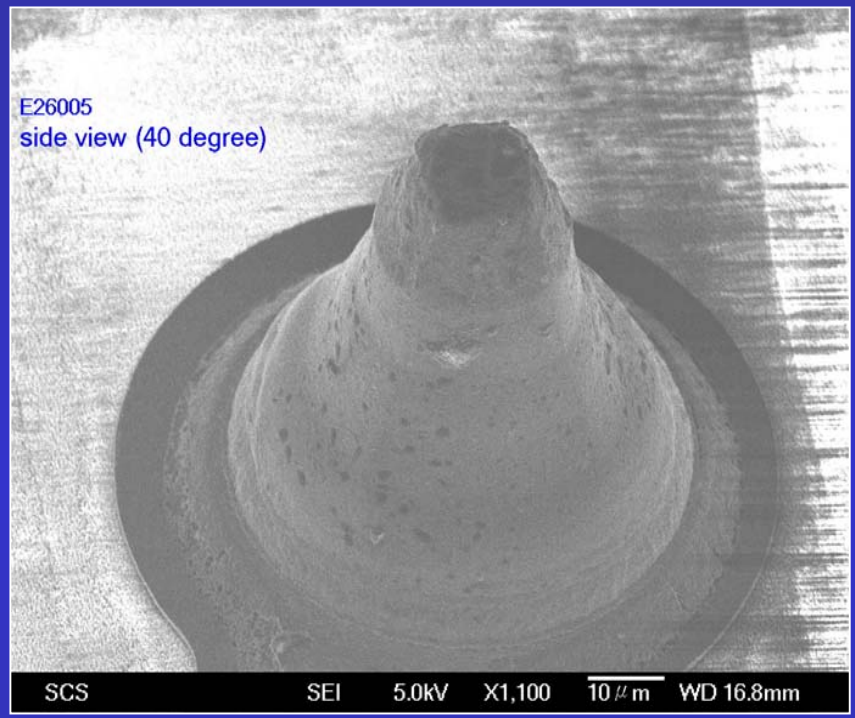


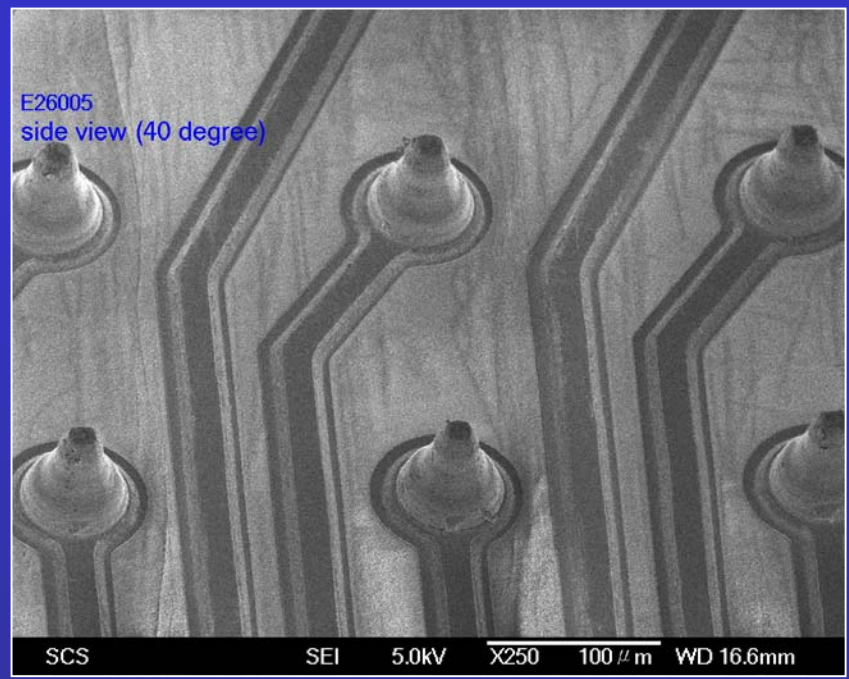
*for Agilent 93000 , probe depth 120 mil

*for Credence/Quartet , probe depth 320 mil

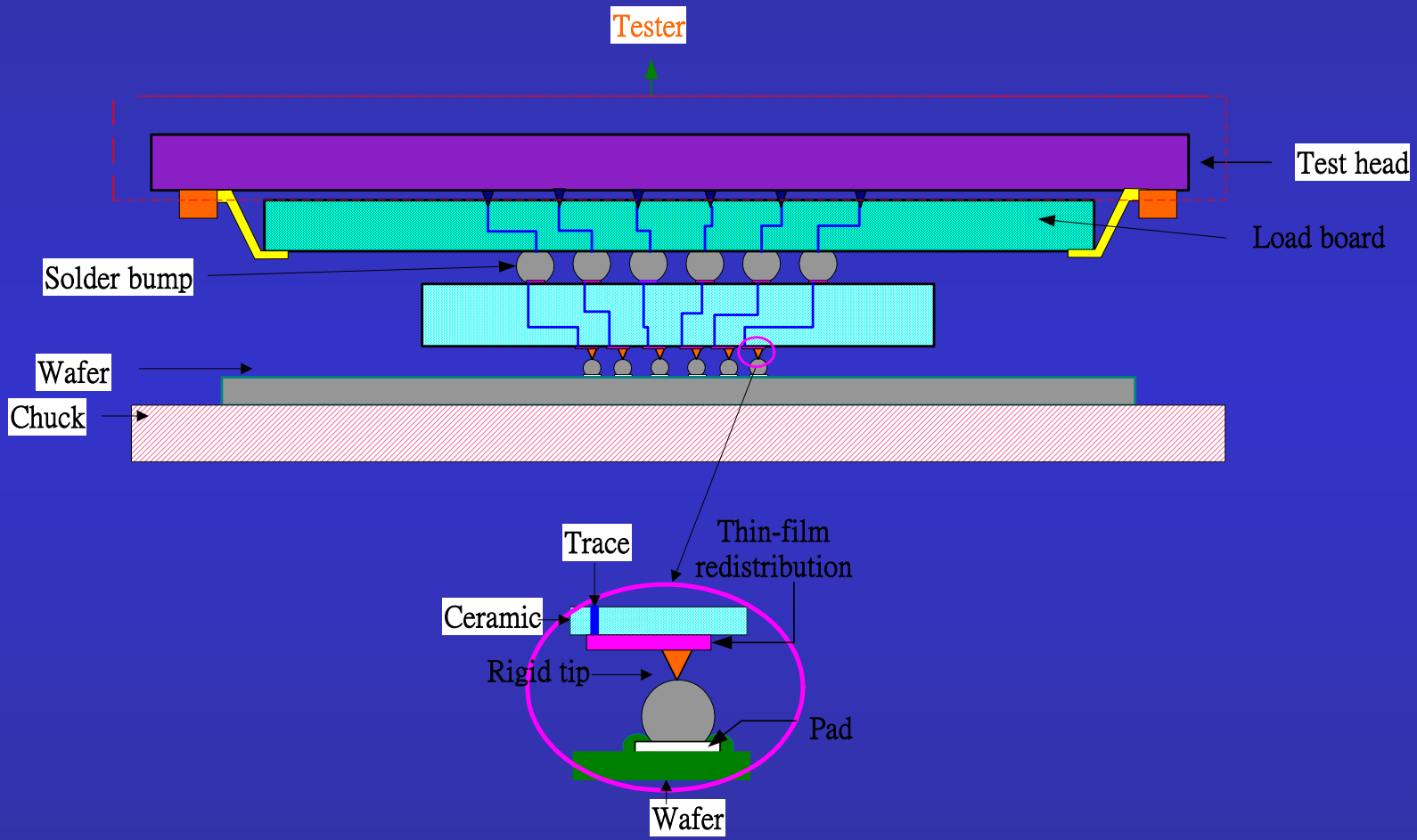


1. accipiter® Structure:





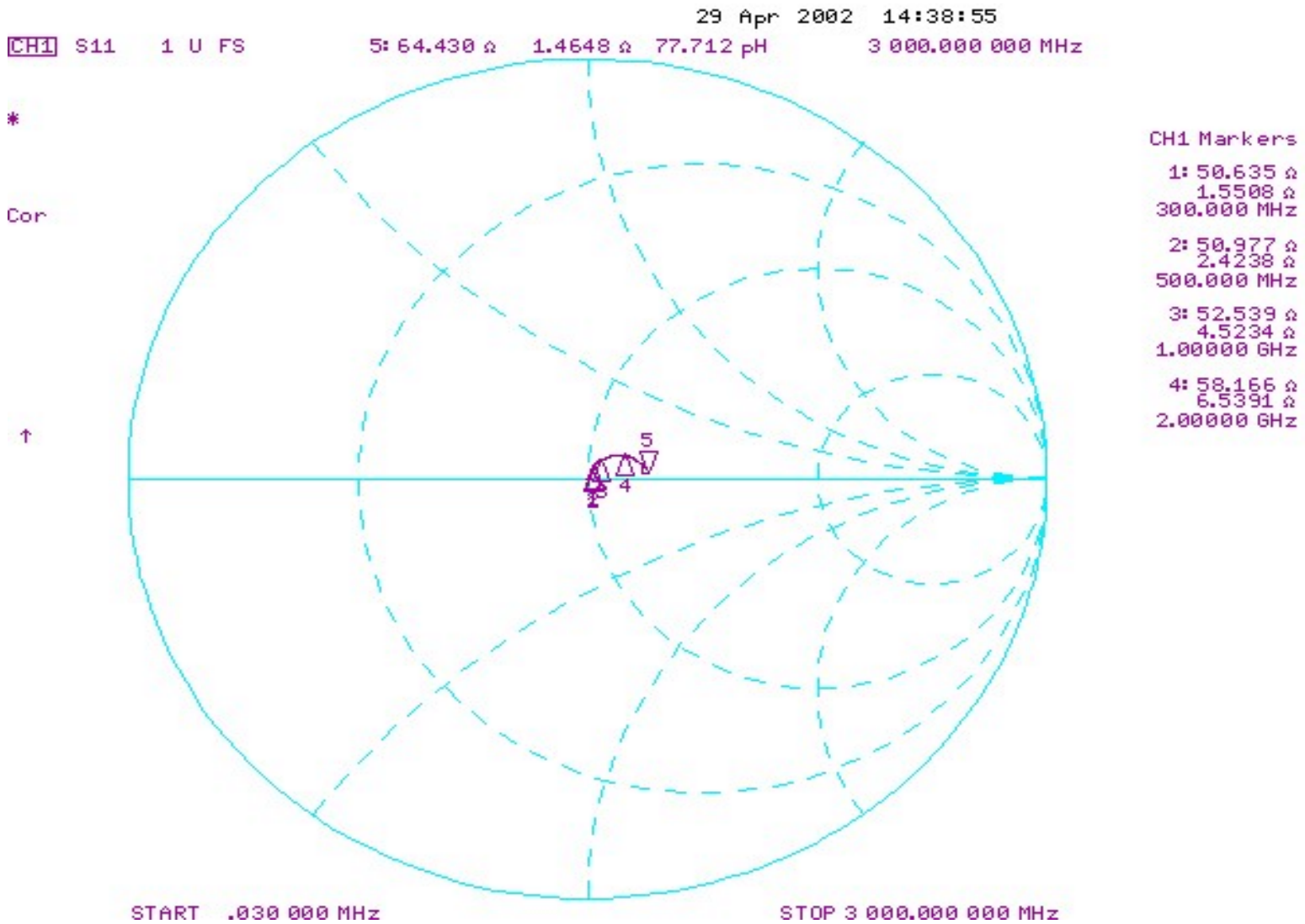
1. accipiter® Structure:



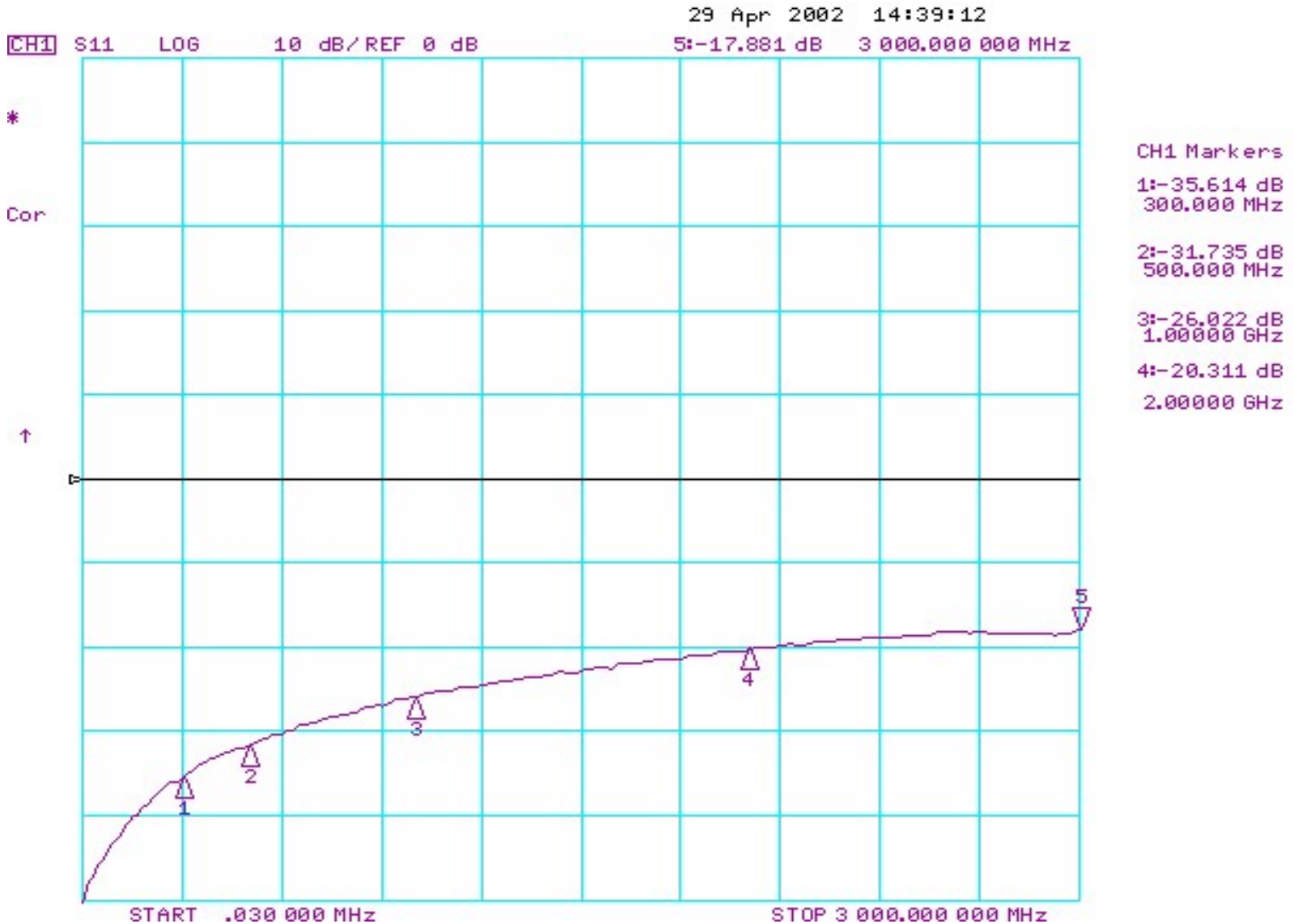
Benefit of MEMs + ULTCC:

- **Up to 2048 I/O design.**
- **Non- pin count relative cost structure.**
- **High Speed Device Probing-3GHz bandwidth**
  - Low impedance -- shorter trace length
  - High noise inhabitant -- dielectric constant : 7.8
- **High accuracy - same level with fab process**
- **Low contact damage- tip dimension 7 ~ 12 μm**
- **High Planarity- within 3 μm**
- **Less than 2 weeks for repeat order.**
- **Long life time. Estimate 1M insertions.**

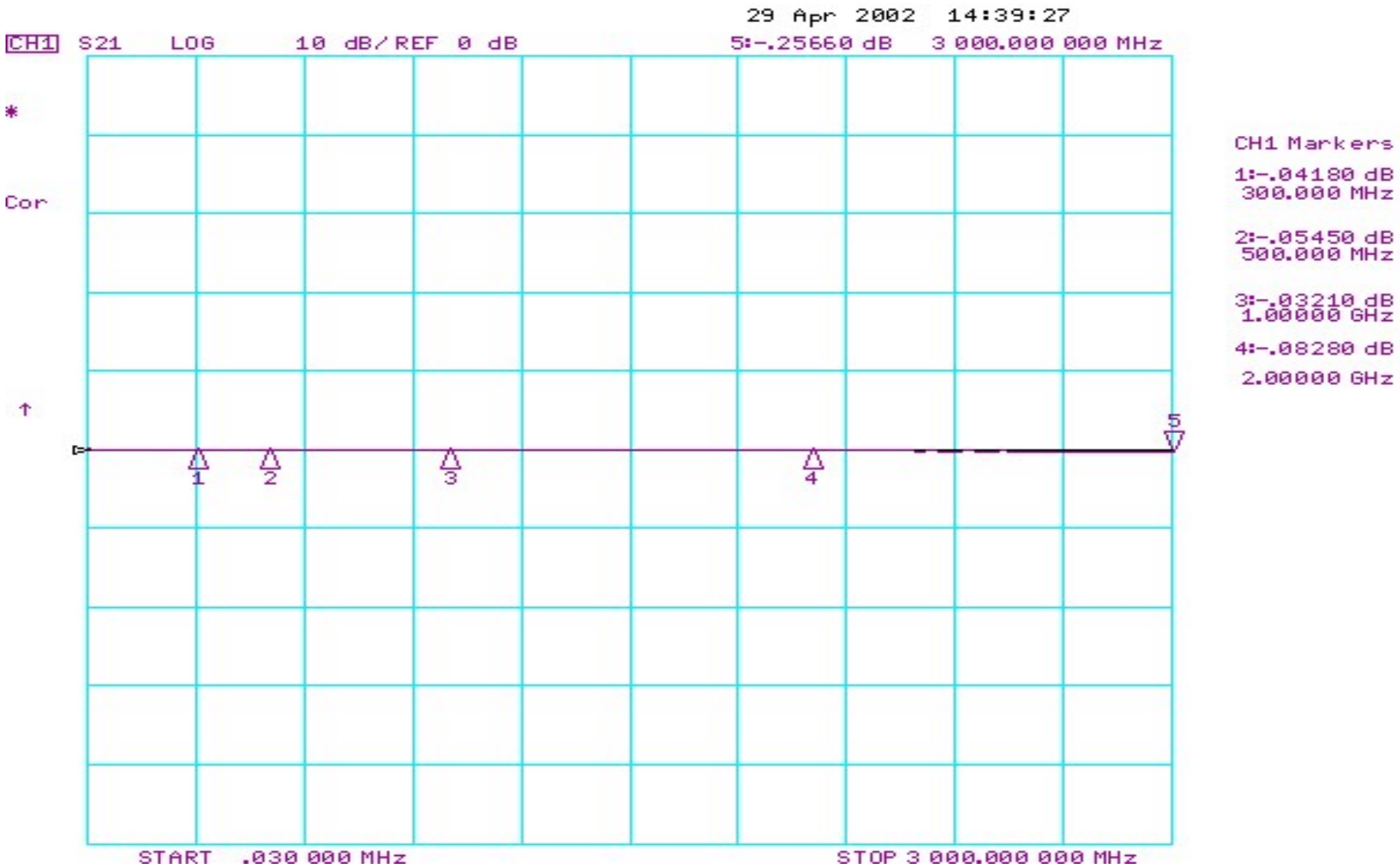
Electrical Characteristic – Impedance (1)



Electrical Characteristic – Return loss (2)



Electrical Characteristic – Insertion loss (3)



Specification:

Tip Dimesions	7~12 um
Probe Tip Height	75 um
Max. Probing area	4"
Min. Probing Pitch	90um/Array
Accuracy	+/- 1um
Planality	< 3 um
Max. Current	800 mA
Shear Force	100 g / pin
Major Material	Ni/Tip, Cu/trace
Path RES.	< 2 Ohm
Impedance Match	50 Ohm +/- 10%
Leakage	< 10nA @ 5V
1st Order L/T	5 weeks
Repeat Order L/T	< 2 weeks

Life time analysis

Subject: SCS MEMS VPC for 8” wafers(633 pins)
Tester/Prober: Agilent 93000/P600, P12/TEL
Clean sheet: Enhanced 3M type C(***type C + polish paper/pink type***)
Tool: Olympus microscope with micro meter
Reading: Check pin high twice(from ULTCC to tip) for average.

Result:

1. *The wear out rate is around 3~6um after 6000 times clean.*
2. *In the bumping probing simulation experiment, there is almost no wear out (pin height) after 250K insertions*

Before

After 15K times

After 120K times

After 250K times

In the real world:

production running

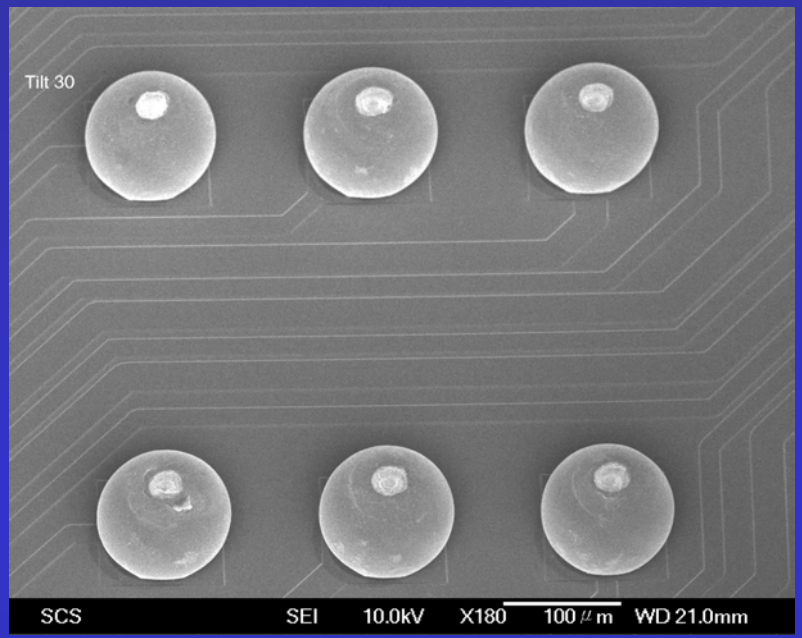
- ***Device:*** **Graphic Chip, 300mm wafers(1699 pins)**
- ***Facility:*** **Agilent 93000/P600 with TEL/P12**
- ***Production units:*** **15 lots(around 100K insertions)**
- ***Probing result:***

  - Yield is around 2 % better than conventional VPC.

  - 1st yield is almost equal to final yield.

  - Limited maintenance needed,brush cleaning only during the production.

In the real world:



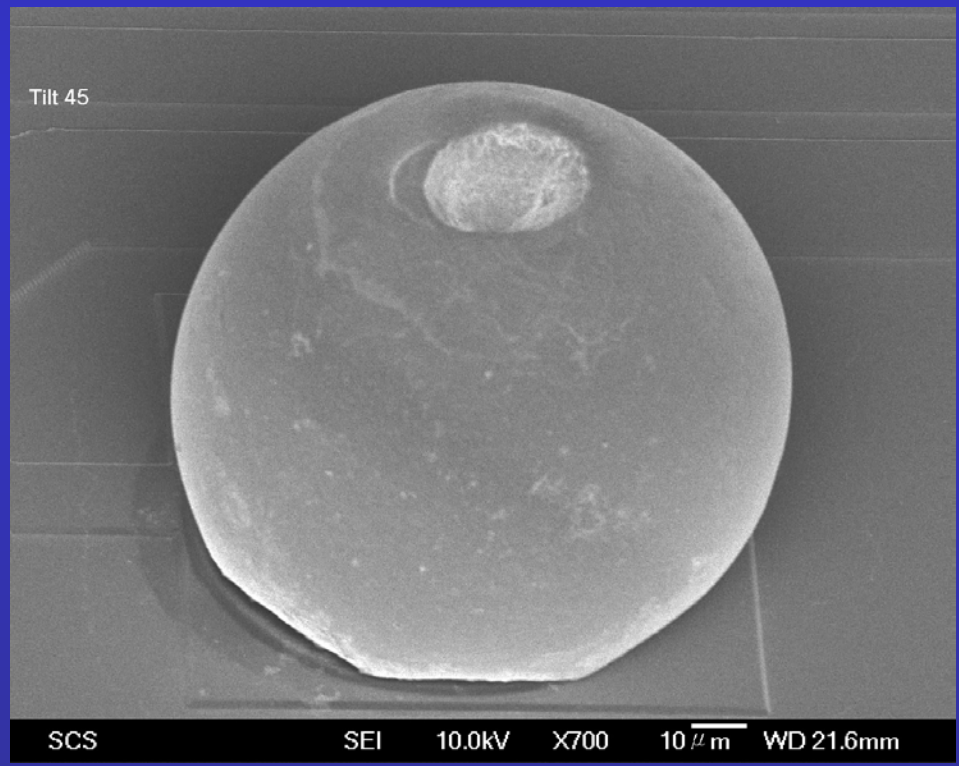
Probing set-up:

O/D: 90um

Dimple dimension: 30 um

Dimple depth: 20 um

 # Dimple size is around 1.2~1.6% of bump size.

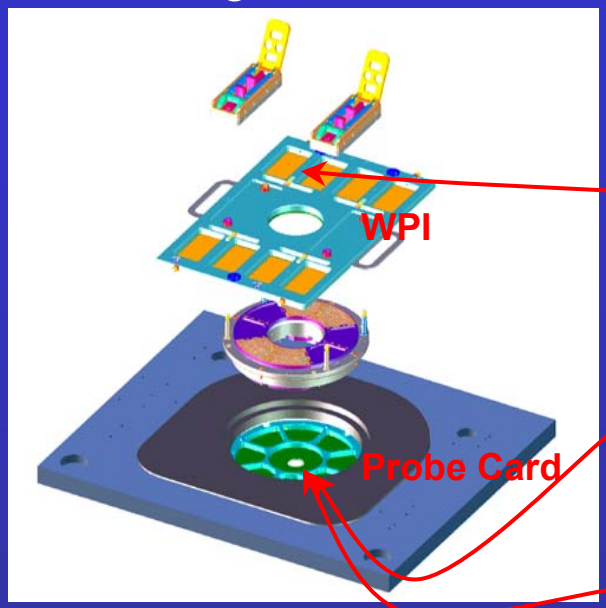


What's Next?

Speed sort in CP stage?

One of our customer set-up a project to simulate the possibility of speed testing in wafer sort stage, he simulate a signal in different frequency and measure this signal in different point of the test environment.

Tester: Agilent 93000/P600 and Network analyzer



Step 1

check at Pogo Pin

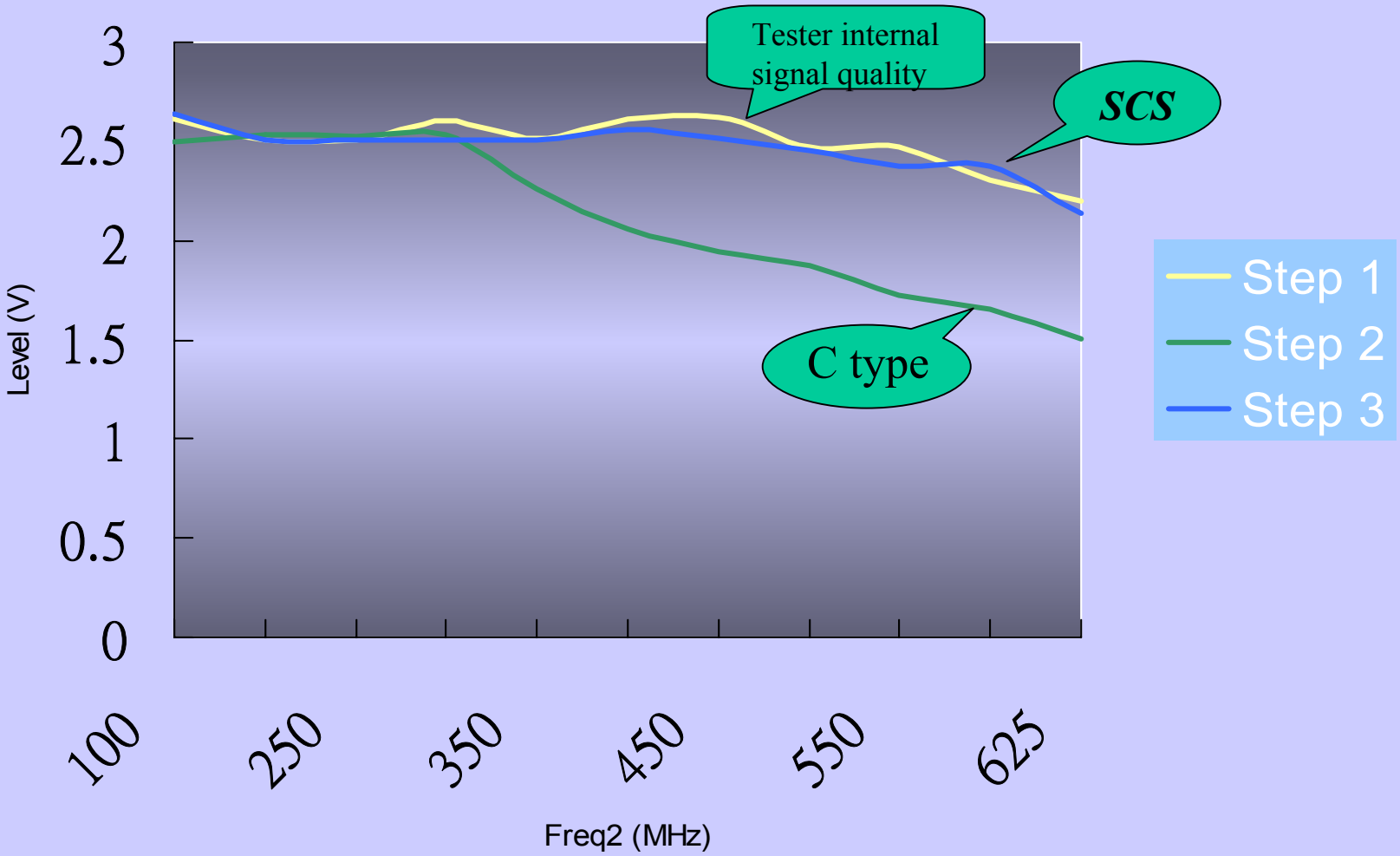
Step 2

Check/probe at Wired Type vertical probe card
(on the solider point)

Step 3

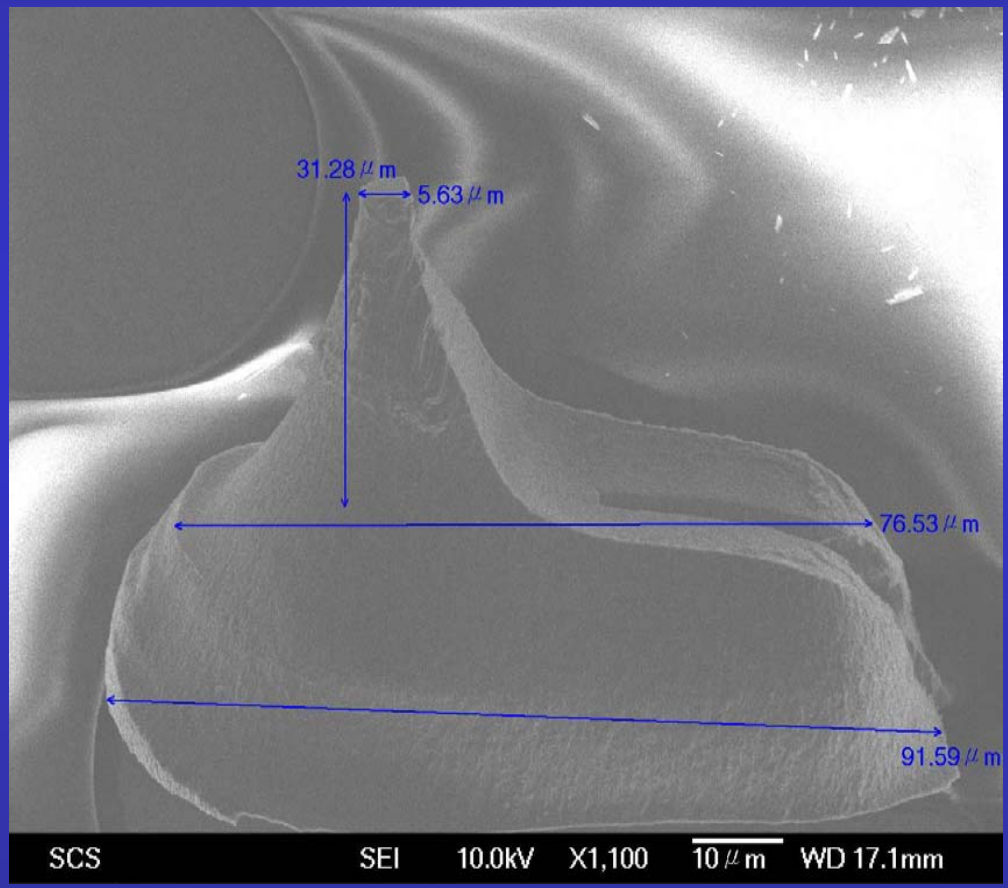
Check/probe at SCS Probe Card
5 → with SCS accipiter **(on the top of needle)**

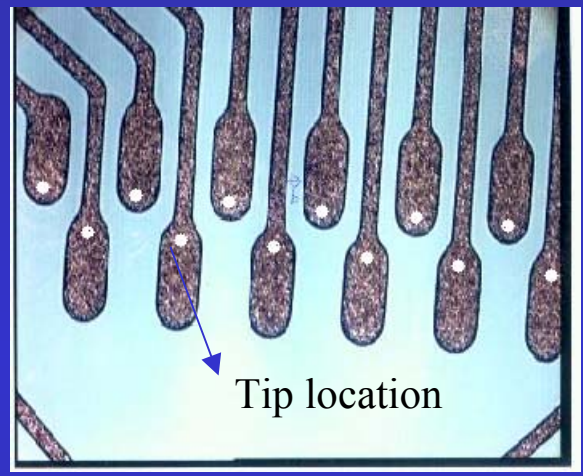
Speed sort in CP stage?



What's Next?

- 45um/linear bump pitch probing?





Object: LCD driver
Bump: Au bump
Bump size:17Hx32Wx65L
Bump pitch: 40um

Conclusion:

- Rigid tip design for VPC is a good design for wafer testing.
- Rigid tip design perform low maintenance needed and reduce the risk of probe card damage.
- As tester price getting higher and higher, utilization rate of VPC is a essential mark of profit.
- MEMs + LTCC technology should be able to apply in bare die B/I test for memory device.