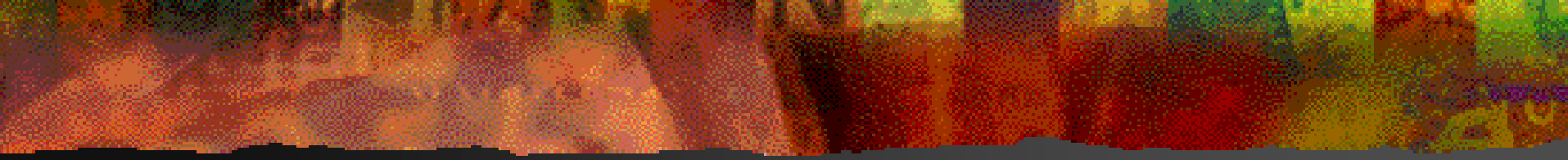

Future Trends
"One Mann's Opinion"

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Future Trends “One Mann’s Opinion”

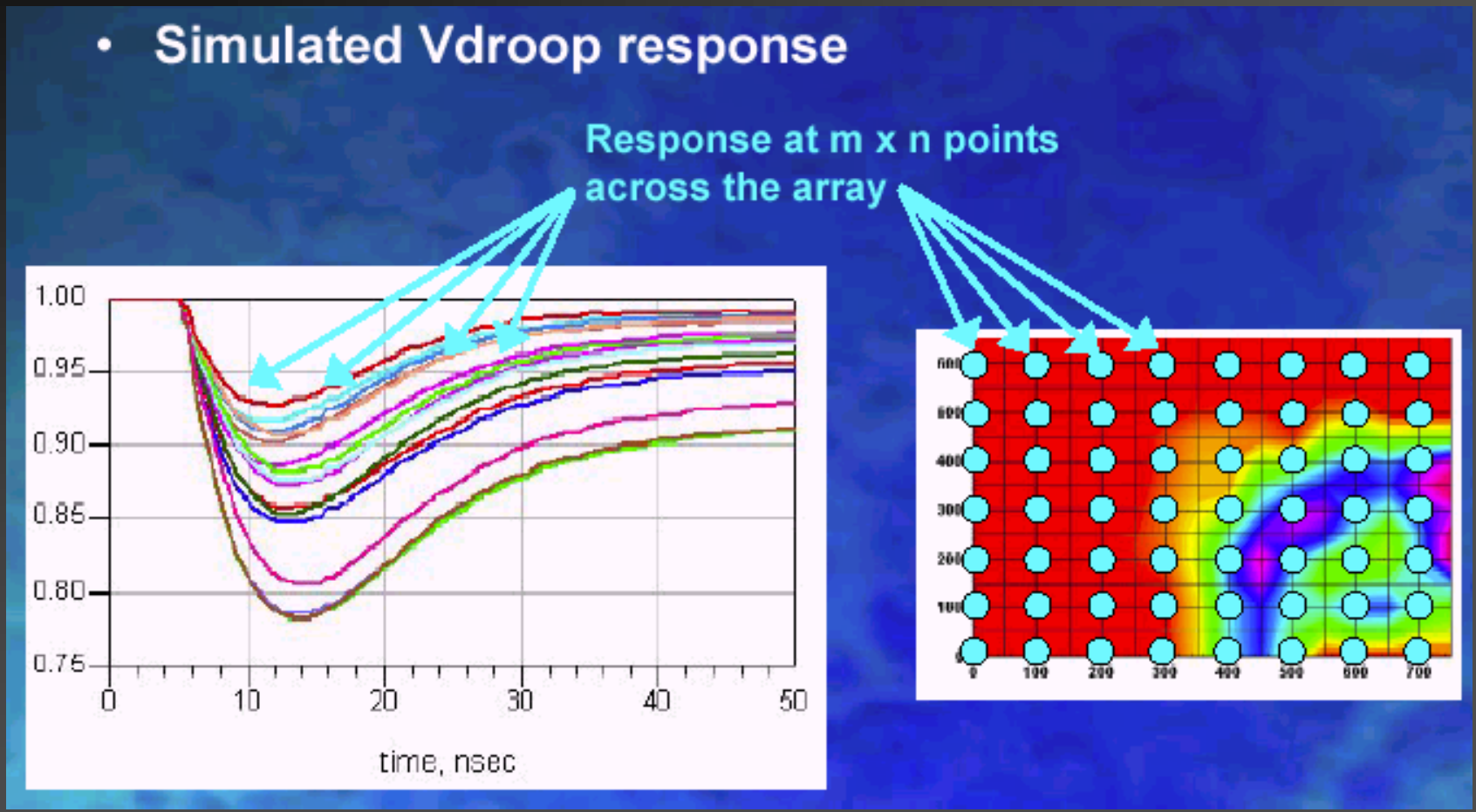
- Relative Reduction in Probe I/Os per die
- Feed Forward of Process Data
- Post Processing Probe Data
- Fully Integrated Probe Test Cell
- Alignment Fiducials
- Reliability Probe Screening
- General Predictions

Reduction In Number of I/O Pads Probed

- **Design For Test, Built In Self Test**
  - Input stimulus generated on-die
  - Output response compacted on-die
  - Chip outputs sampled by same I/O pad input
- **Selective contacts for power and grounds**
  - 10% power & grounds in the “good old days”
  - Now 50 % power & grounds on microprocessors
  - You don’t really need to connect them all
- **Don’t get too excited… Multi-die probing will drive the contacts per probe card up even higher than the ITRS predictions!**

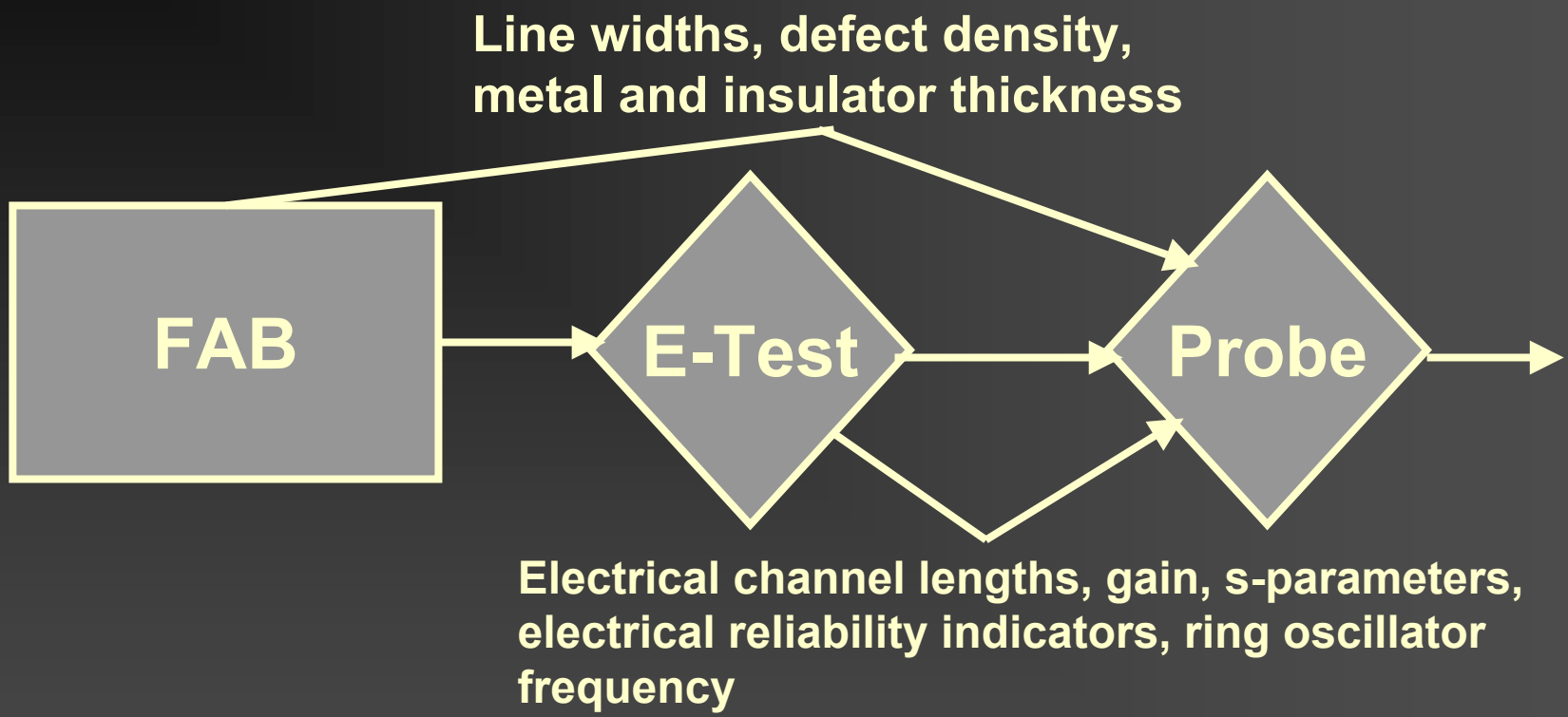
Intel's Selective Power & Grounds*

- Simulated Vdroop response



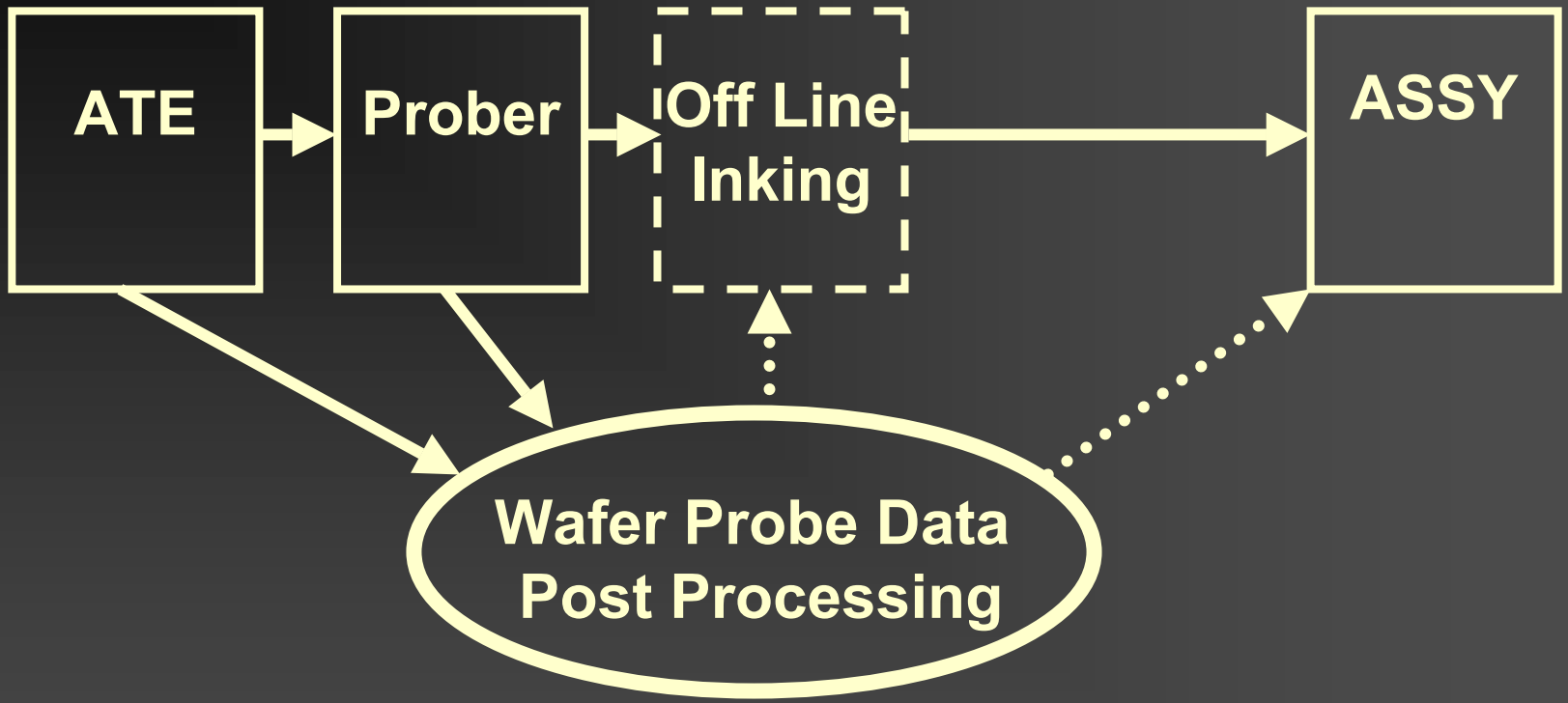
*Southwest Test Workshop, June 2002, web site

Feed Forward of Process Data



- Process & parametric data will effect probe test
- Speed sorting at probe
- Thoroughness of test (Known Good Die)

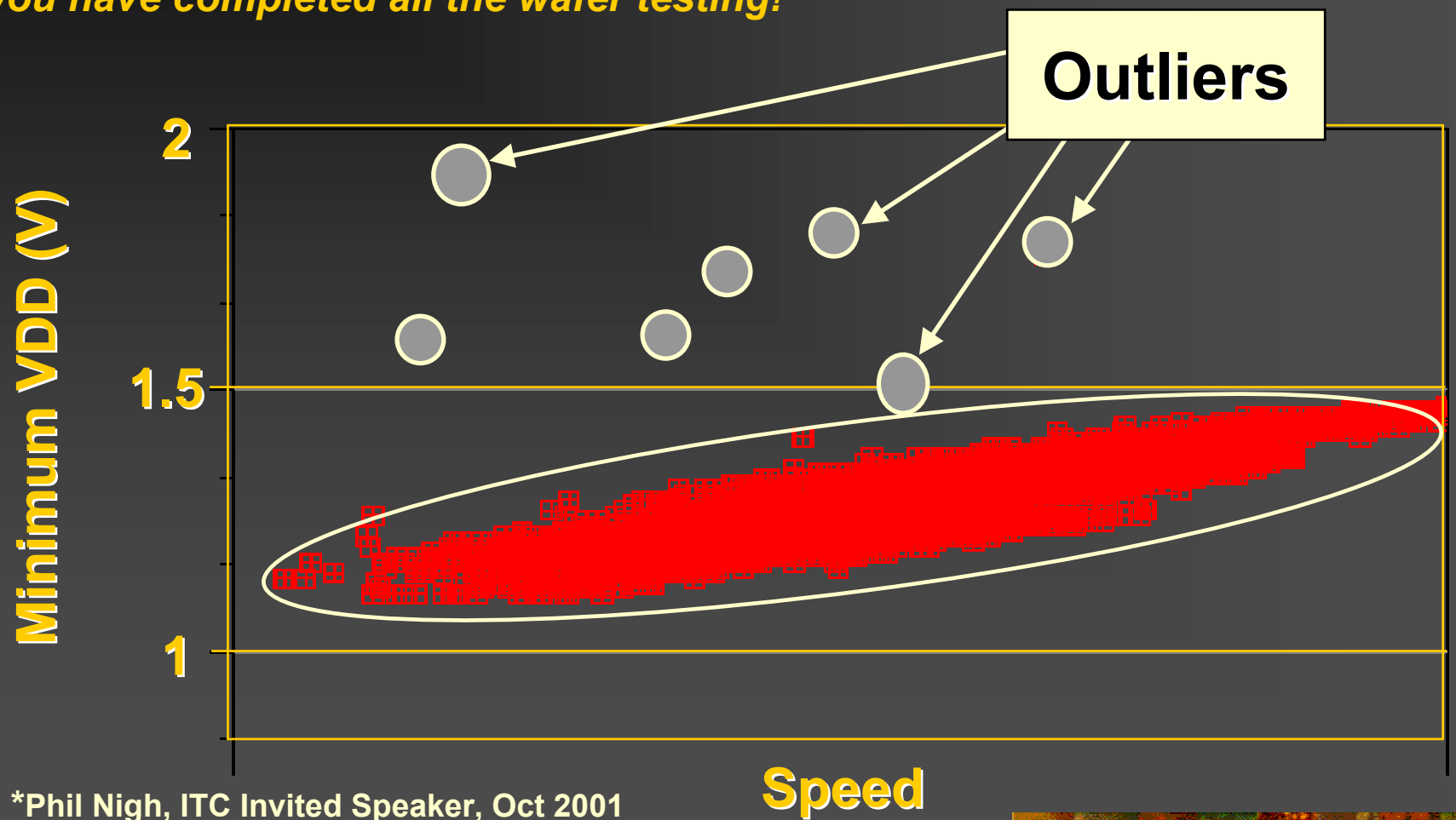
Post Processing of Probe Data



- Test for parametric outlier rejects
- Spacial (topographical) outlier rejects

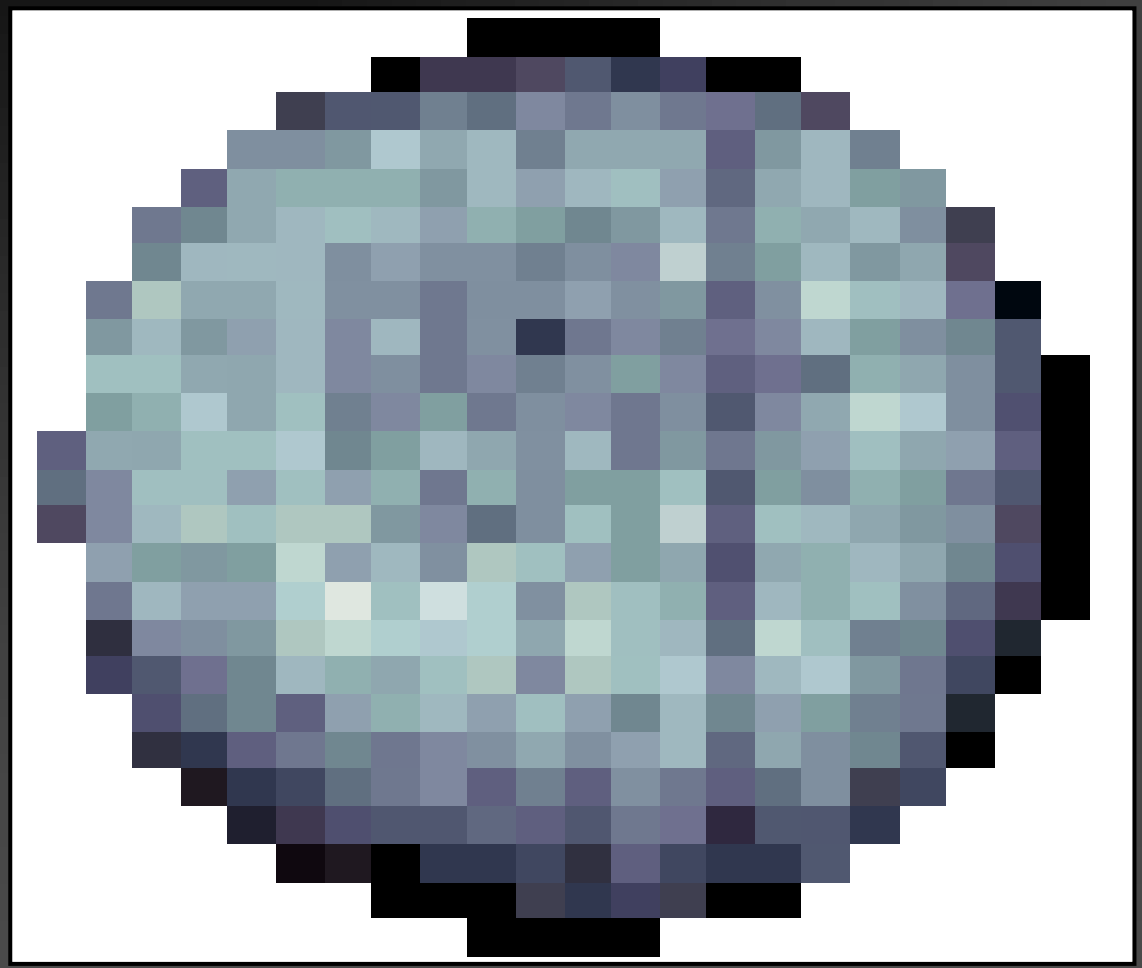
Minimum VDD Outliers*

Problem: You don't know the outliers until you have completed all the wafer testing!



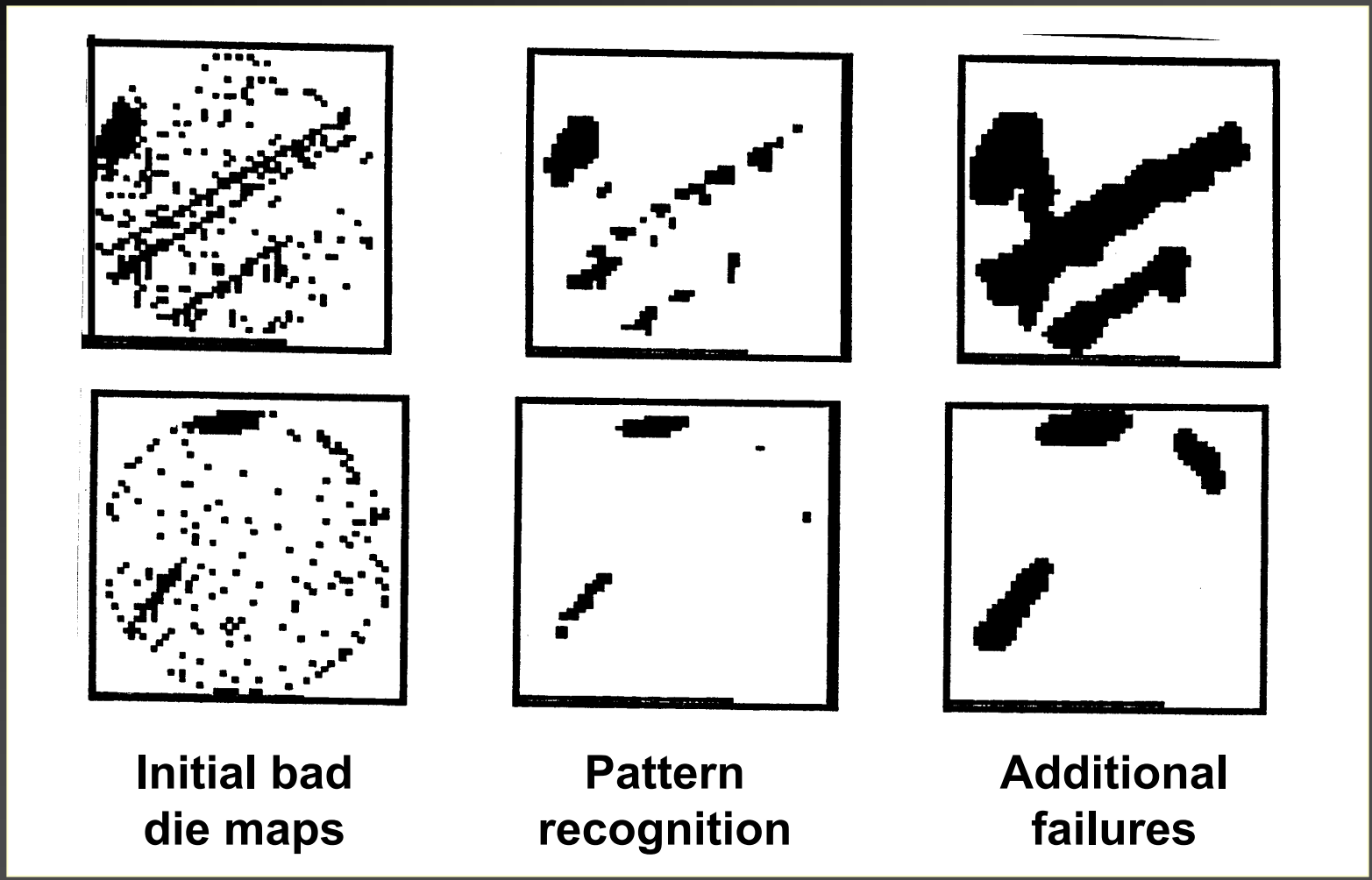
*Phil Nigh, ITC Invited Speaker, Oct 2001

Iddq Spatial Variation



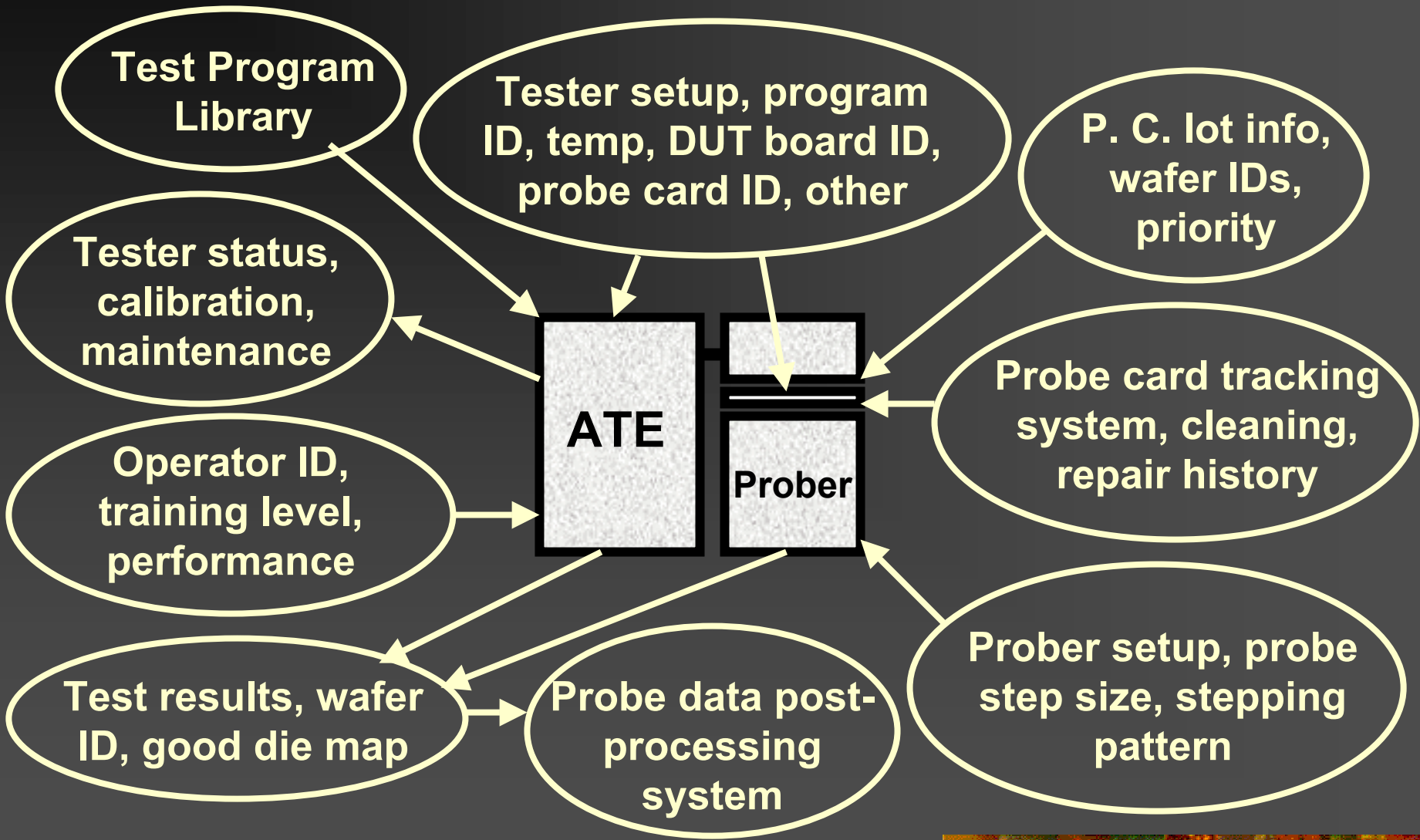
- Noticeable “donut pattern” for background Iddq value
- Where do you set the Iddq threshold?
- Iddq is more than random defect driven

Rejecting Die for an Optical Device (Phillips*)



*Design & Test Of Computers, March-April 2002, pp 44-48

Test Cell Integration



Integrated Probe Test Cell

- Wide variety of often independent data bases, programs, and platforms
- Multiple test cells, ATE types, and locations
- New equipments always being added
- Extensive operator training and retraining

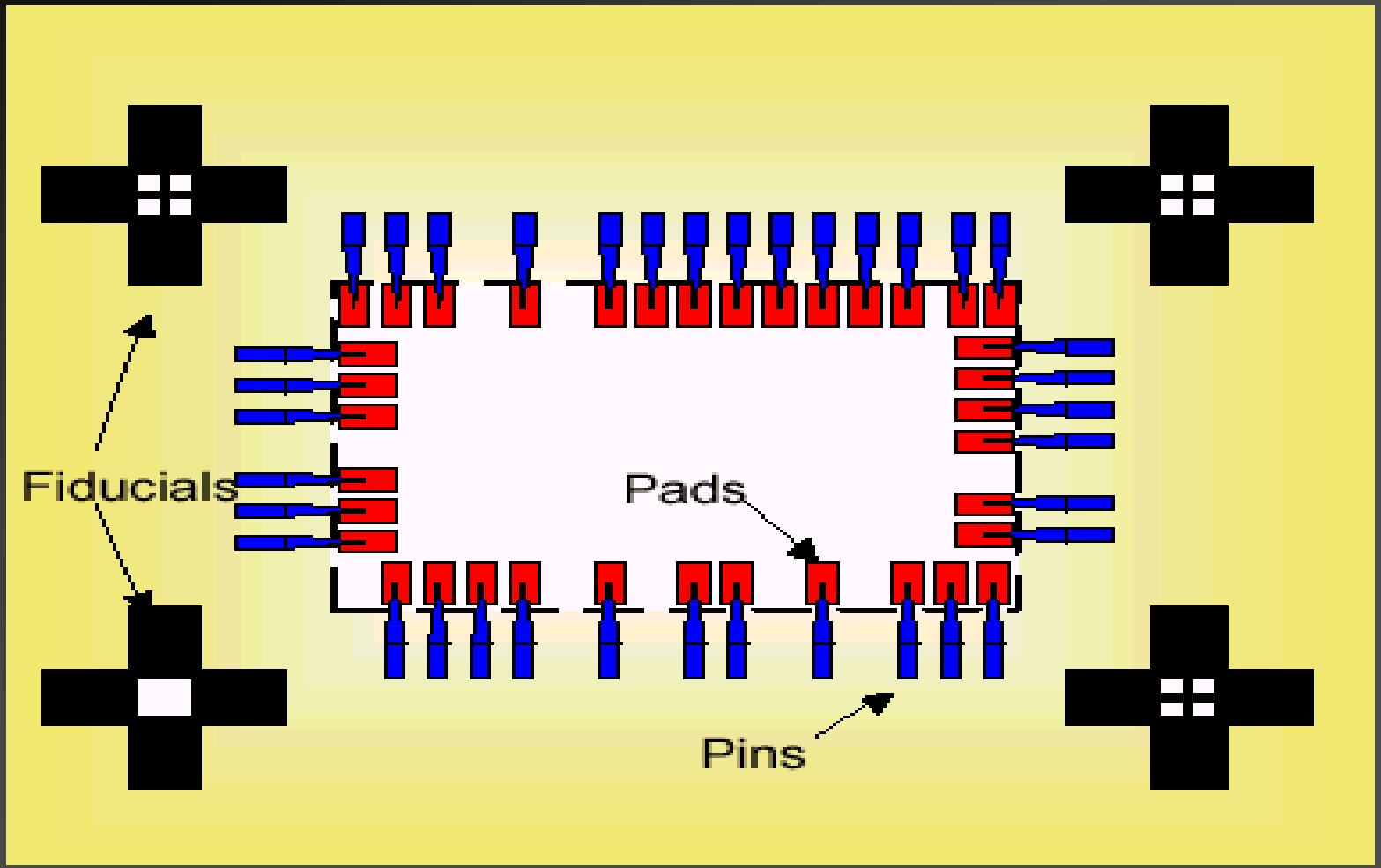
Someone will bring it all together

But who?

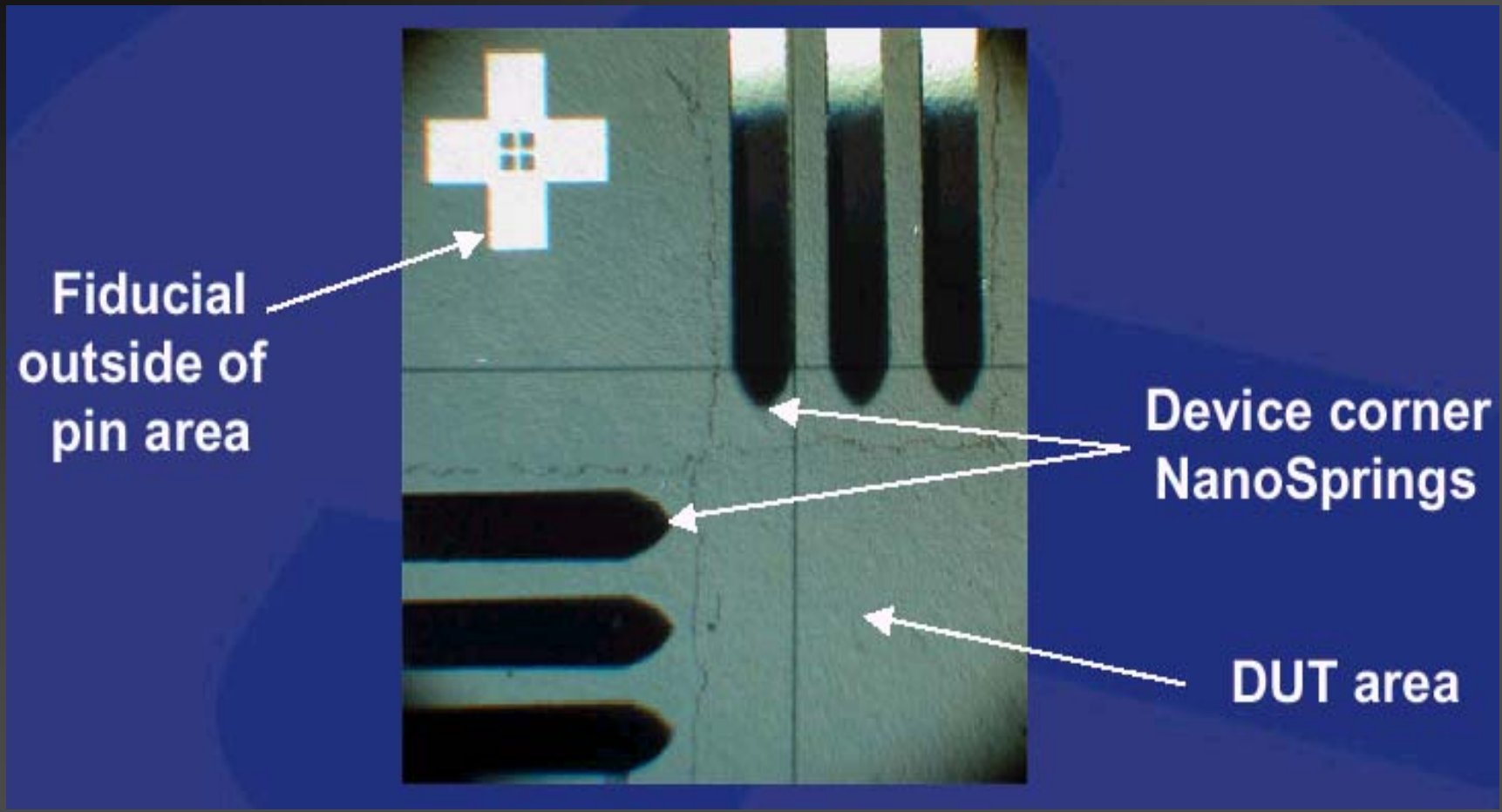
Alignment Fiducials

- Present methods uses prober cameras to align needles to I/O pads
- Some new technology contactors are not easy for the pattern recognition to see
- EG and NanoNexus developed alignment by targets (fiducials) on probe card
- Concept can reduce cost of prober optics and reduce alignment time
- Can be extended to fiducials on wafers

Alignment Fiducials



NanoNexus & Electroglas*

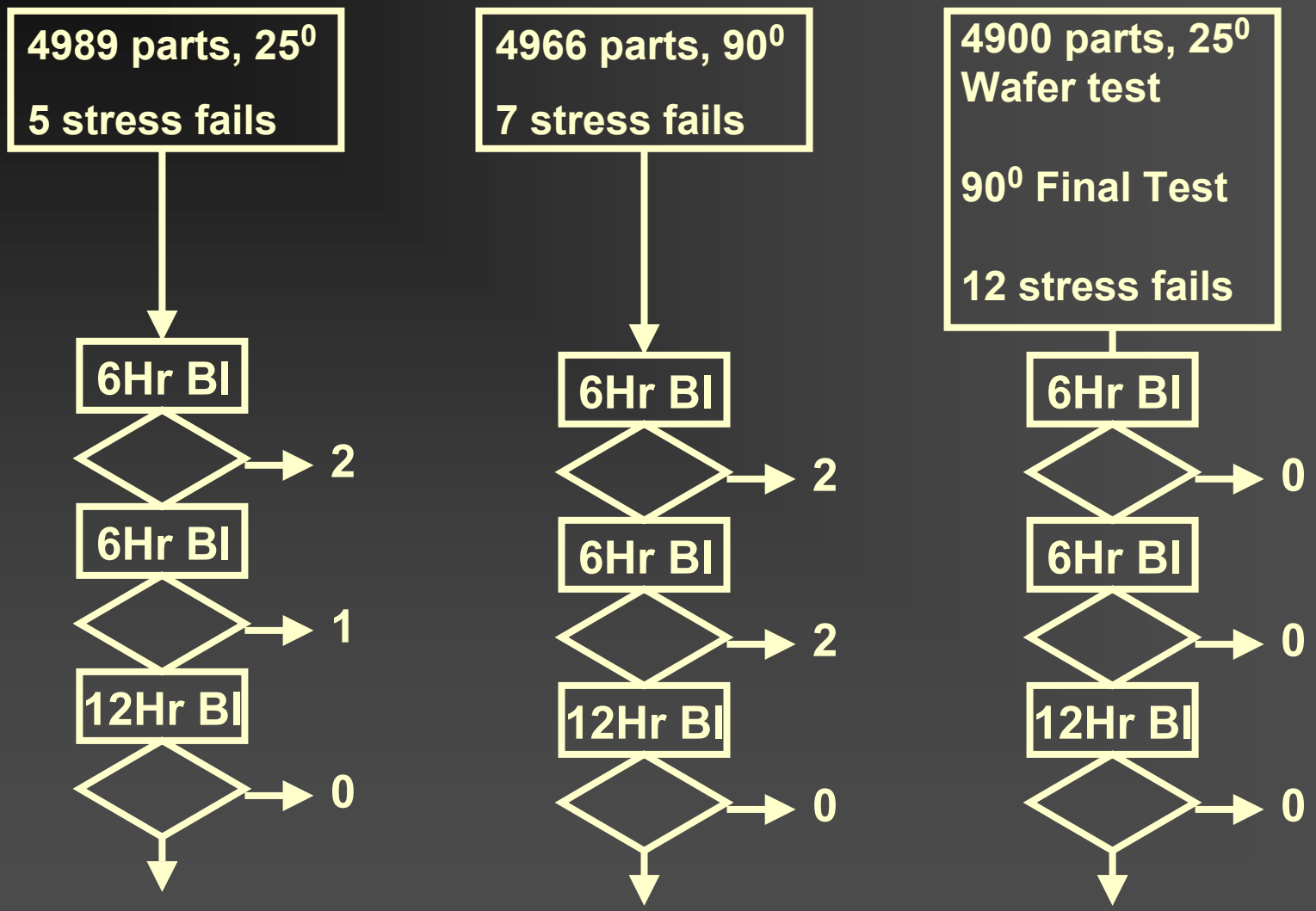


*Southwest Test Workshop, June 2002, web site

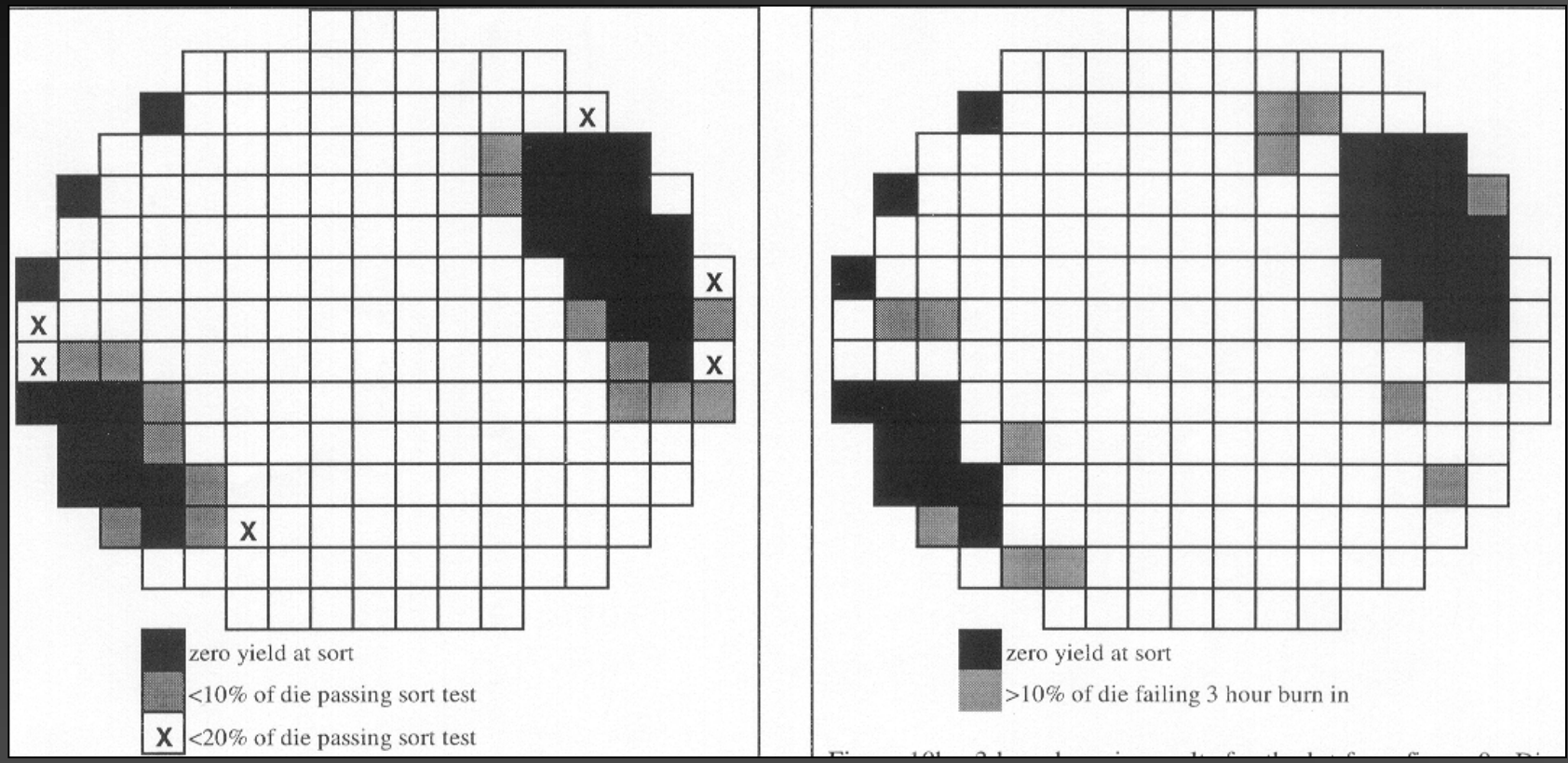
Reliability Screening at Probe

- Voltage stress followed by test
- Interesting experiment on .18 micron chip
- Early Failure Rate was 2000-3000 PPM
- Five lots, 112 wafers, were split three ways
- Tests of stress levels up to 1.6x for 1 sec
- Two splits evaluated stress temperature
- Last split demonstrated final flow
- Stress replaced 100% production Burn-In!

Voltage Stress Experiment



Intel* Probe Yield Vs Burn-In Fails

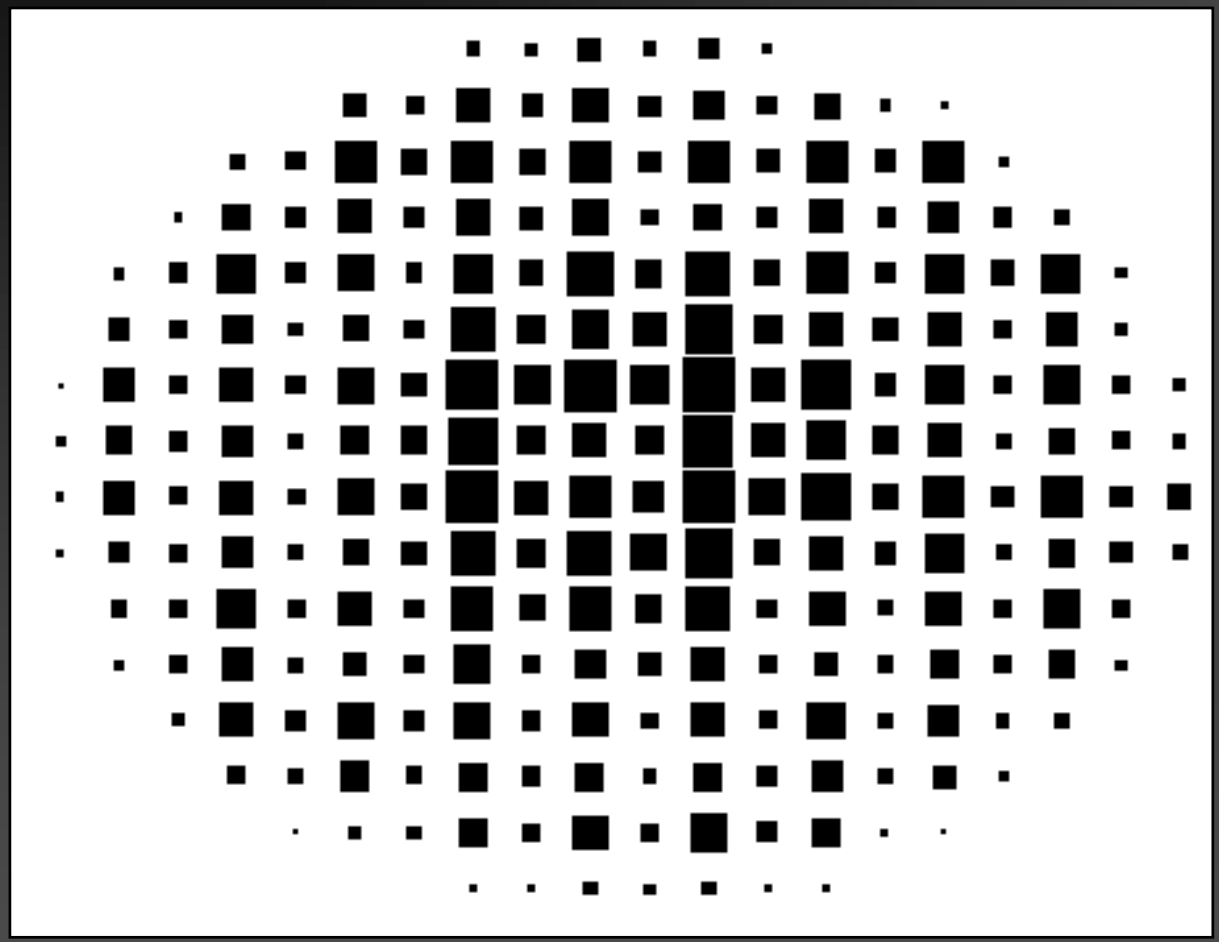


Probe map of zero and low yielding die locations

Map of low yielding locations after 3 hours of burn-in

*International Reliability and Physics Symposium, 1999

Intel's* Scrapped Unreliable Die



Die passing sort, rejected for reliability concerns (size of box is proportional to % rejected)

*International Test Conference, 2001, Paper 40.3

General Predictions

- Someone will invent a liquid/plasma I/O pad cleaner eliminating needle cleaning
- Bare die sales will be supported by suppliers with unique probe tests (+$NRE)
- I/O pad damage will transition from a minor packaging yield loss to a major reliability crisis
- Probe testing will be absorbed by packaging facilities (OMG!)
- Full Wafer Probing??? Just be patient…