

***A test-setup for probe card characterization
under „production-like“ operating conditions***

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A Test-Setup for Probe-Card Characterization

Outline

- Background / Motivation
- Test Concept Requirements
- Test Setup
- Probe-Card Measurement Results
- Summary

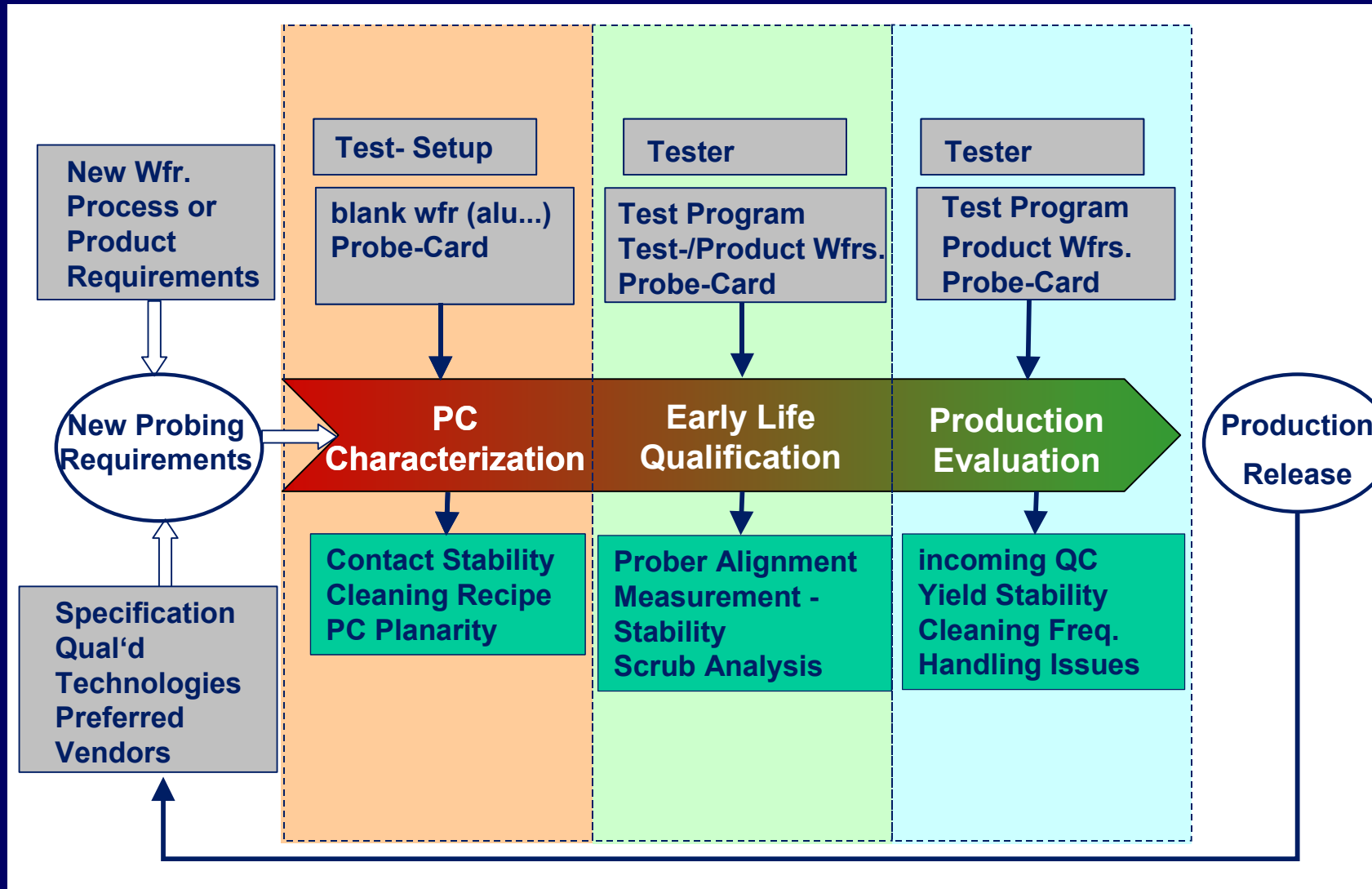
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Background

- strong need for probe card evaluation process for:
 - new probing technologies (pad arrangements, pitch, multi DUT)
 - new products: (materials, BEOL-stack)
- short „time-to-market“ prohibits iterative improvement process
 - evaluation process needs to start earlier
- missing links in the evaluation process:
 - reliable prediction of c_{res} performance
 - c_{res} stability under manufacturing conditions

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Probe-Card Evaluation - *IDEAL* flow



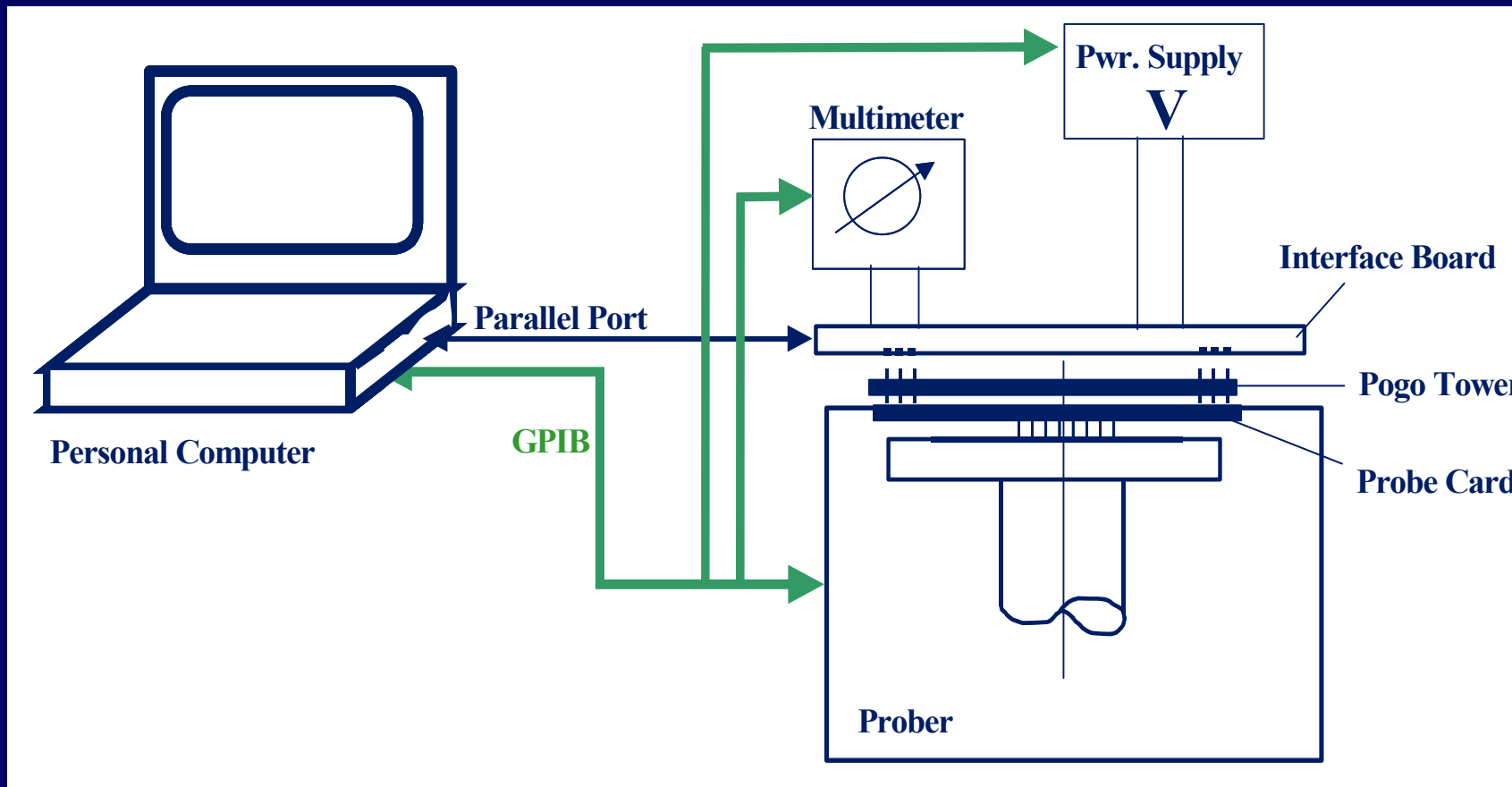
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Test Concept - Requirements

- test scenario as close as possible to real probing conditions
 - force current through contacts
 - probing parameter variation
 - temperature
 - overdrive
 - chuck-speed
 - high number of Touch-Downs
 - different contact materials
- Evaluation should be possible w/o specific product or test-chip
 - amount of test-chip and/or product wfrs limited
 - product schedule can be shifted
- low cost & flexible setup
 - use existing equipment & h/w (but no tester)
 - flexible channel assignment (Vcc, GND)

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Test Setup- Overview 1/2



A Test-Setup for Probe-Card Characterization

Test Setup- Overview 2/2



Interface Board



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Test-Setup Main Features

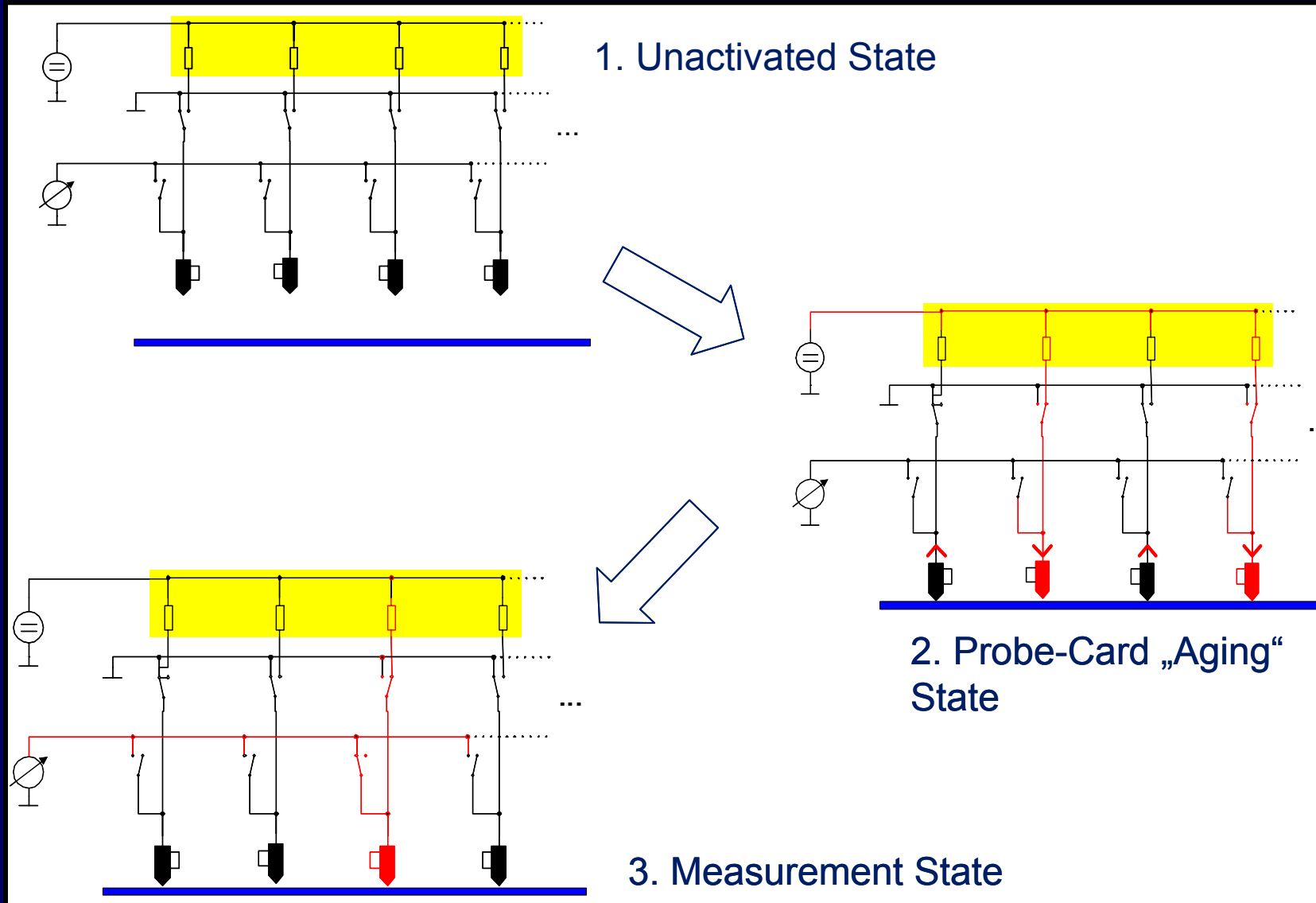
- Wafer handling: TSK APM 90 (available prober)
(w/ Prober-Interface Docking Unit)
- Nr. of measurement channels: 128
flexible channel assignment of probe contact to Vdd or Gnd via GUI
- Current per needle: 0,1-200 mA
- Repeatability (σ): ca. 1,4 m Ω
- Data Output: ASCII format

				number	1	2	3	4	5	6	7	
				channel	7	6	5	2	3	1	68	
				X-coordinate	0	0	0	0	0	0	0	
				Y-coordinate	7931	7611	7291	6971	6651	6171	3371	
				comment	DAIS'	DAIS'	DAIS'	DAIS'	DAIS'	DAIS'	DAIS'	
				VCC / GND	GND	VCC	GND	VCC	GND	VCC	GND	
touchdown	X	Y	X_abs	Y_abs								
	2	3	5	166.245	346.0482	1.27	4.86	1.64	1.02	0.91	2.38	30
	4	5	5	147.74	346.0482	1.35	4.55	1.92	0.91	0.78	2.54	30
	6	7	5	129.235	346.0482	1.27	4.79	2.04	0.87	0.9	2.02	30
	8	9	5	110.73	346.0482	1.32	4.82	2.09	0.92	0.96	2.18	30
	10	11	5	92.2248	346.0482	1.42	5.68	2.49	0.9	1.02	2.58	30
	12	14	4	64.4648	370.2382	1.19	5.37	1.8	0.89	0.83	1.76	30
	14	12	4	82.9698	370.2382	1.25	4.76	1.59	0.77	0.91	1.65	30
	16	10	4	101.475	370.2382	1.11	4.95	1.69	0.75	0.88	1.7	30
	18	9	4	110.73	370.2382	1.4	4.67	1.83	0.74	0.82	1.99	30

Example
Result File

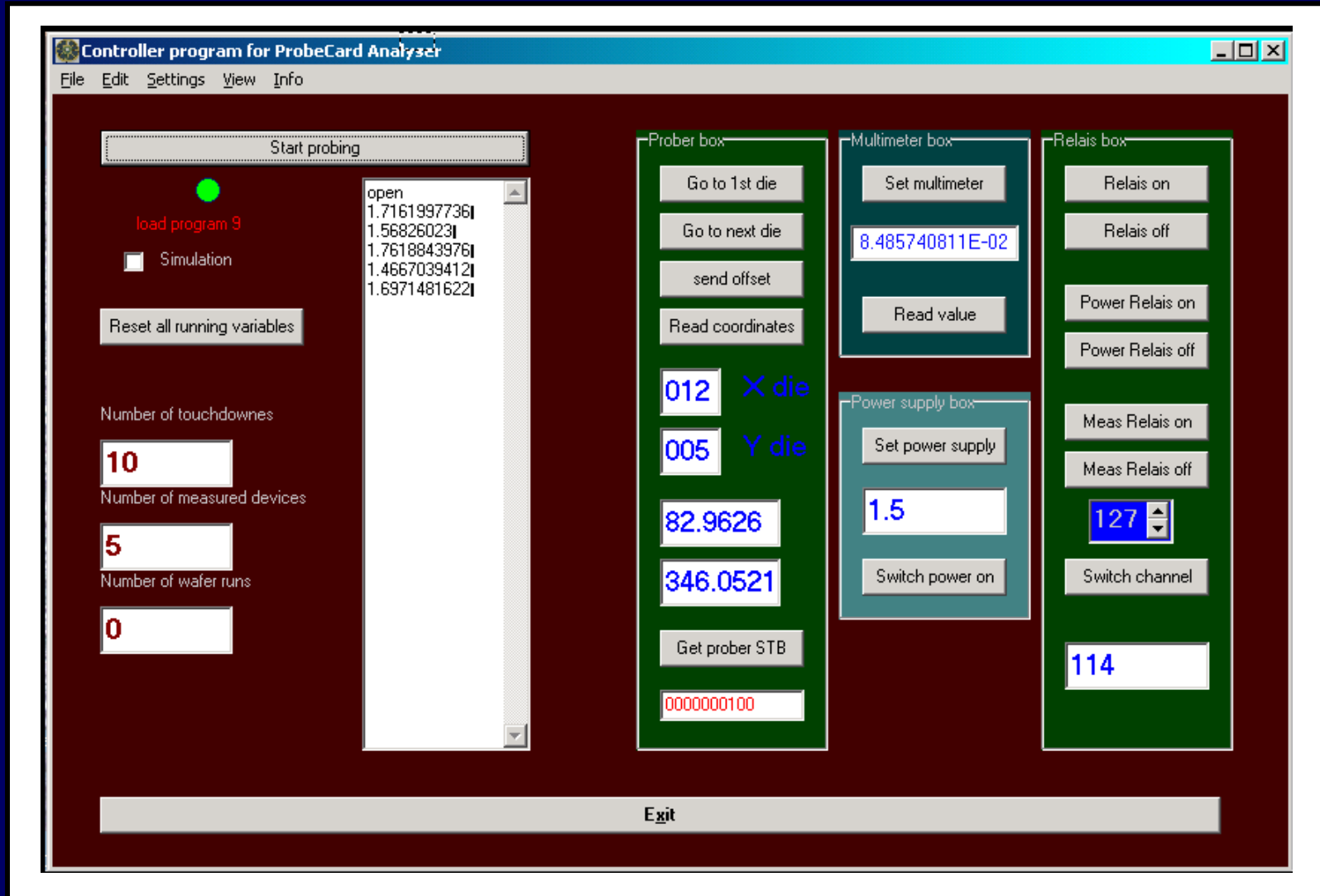
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Test Sequence 1/2



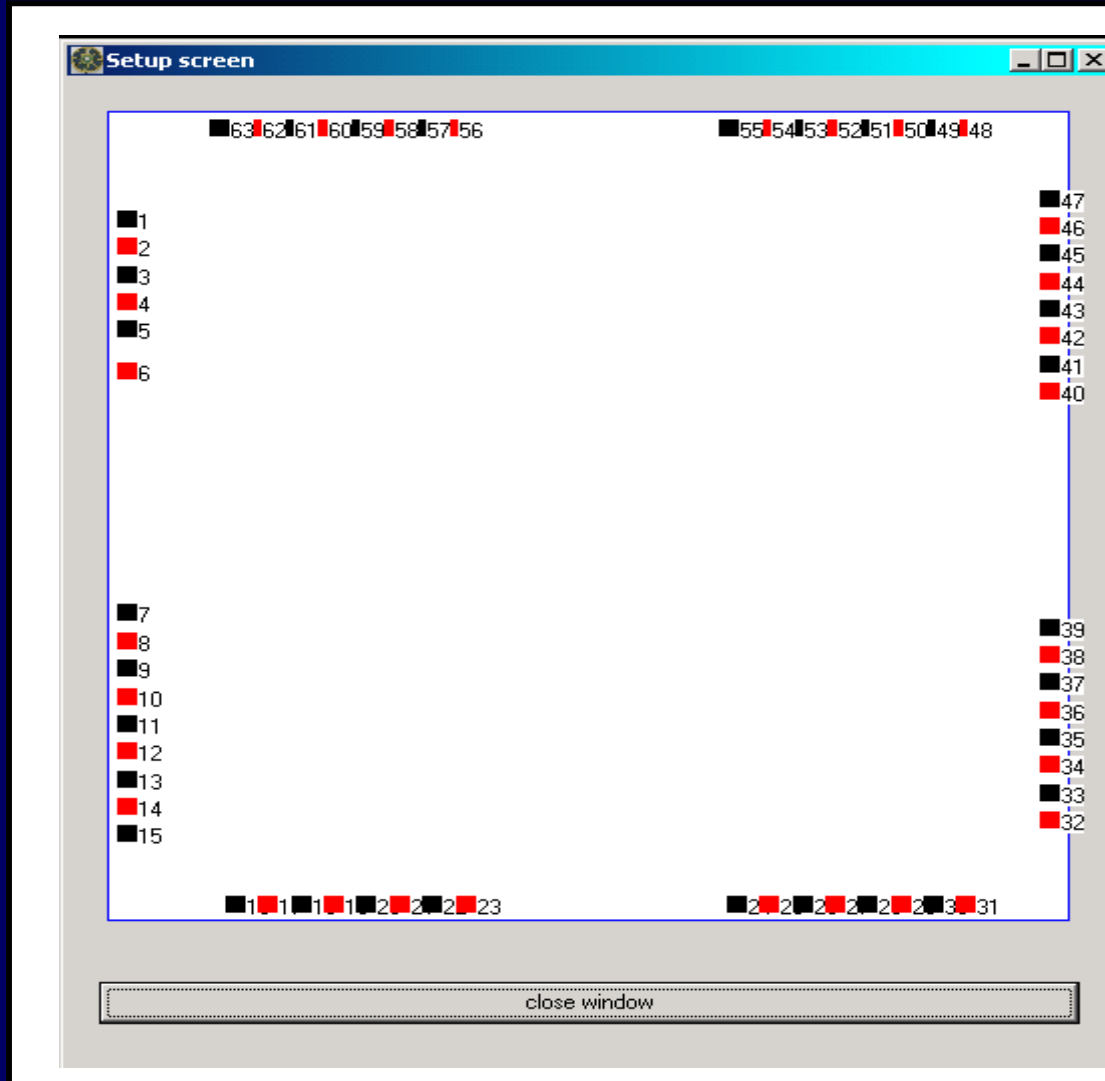
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Test Setup- User Interface 1/2



A Test-Setup for Probe-Card Characterization

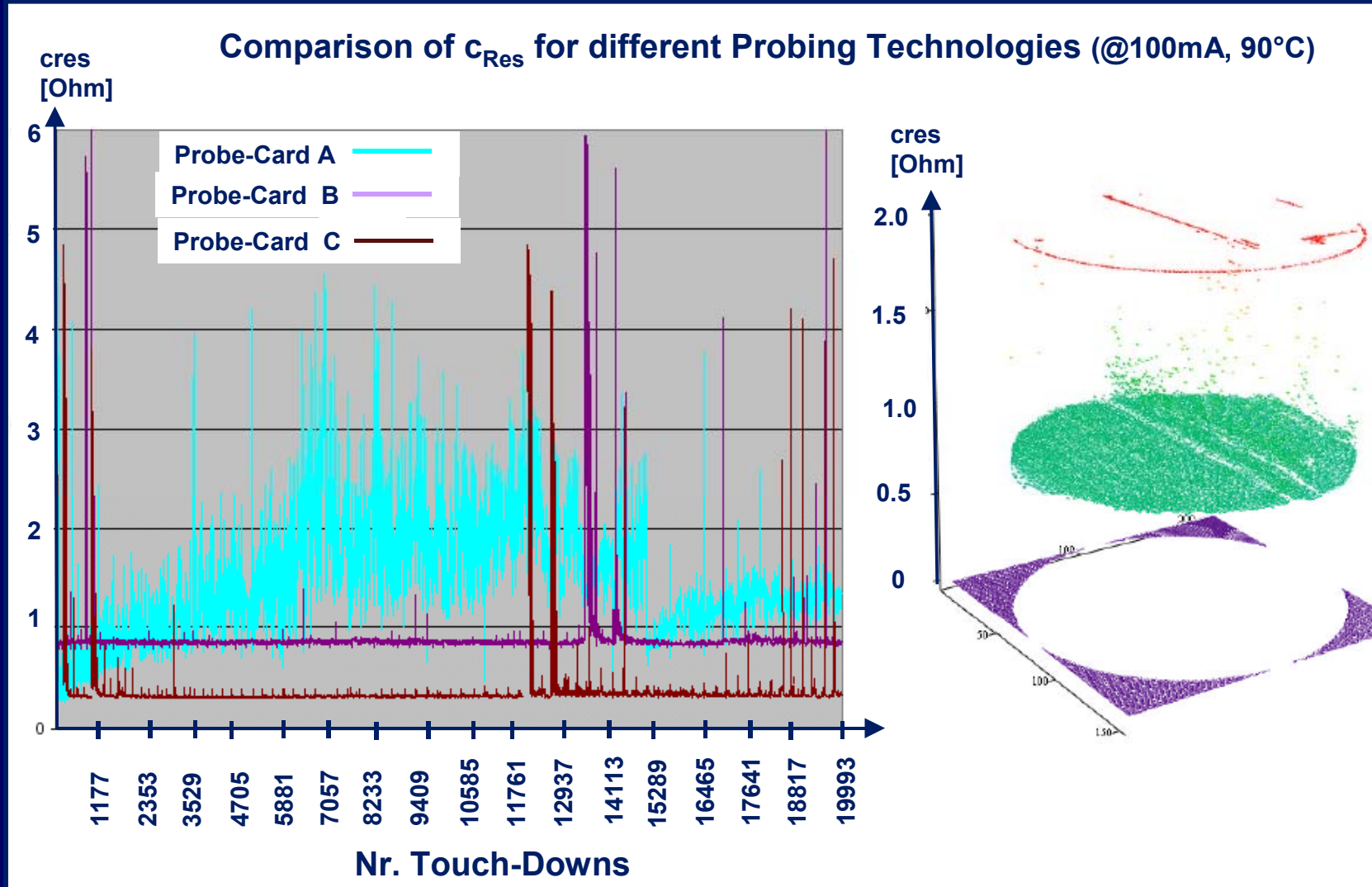
Test Setup- User Interface 2/2



**Mapping of Pins
to Vdd and Gnd**

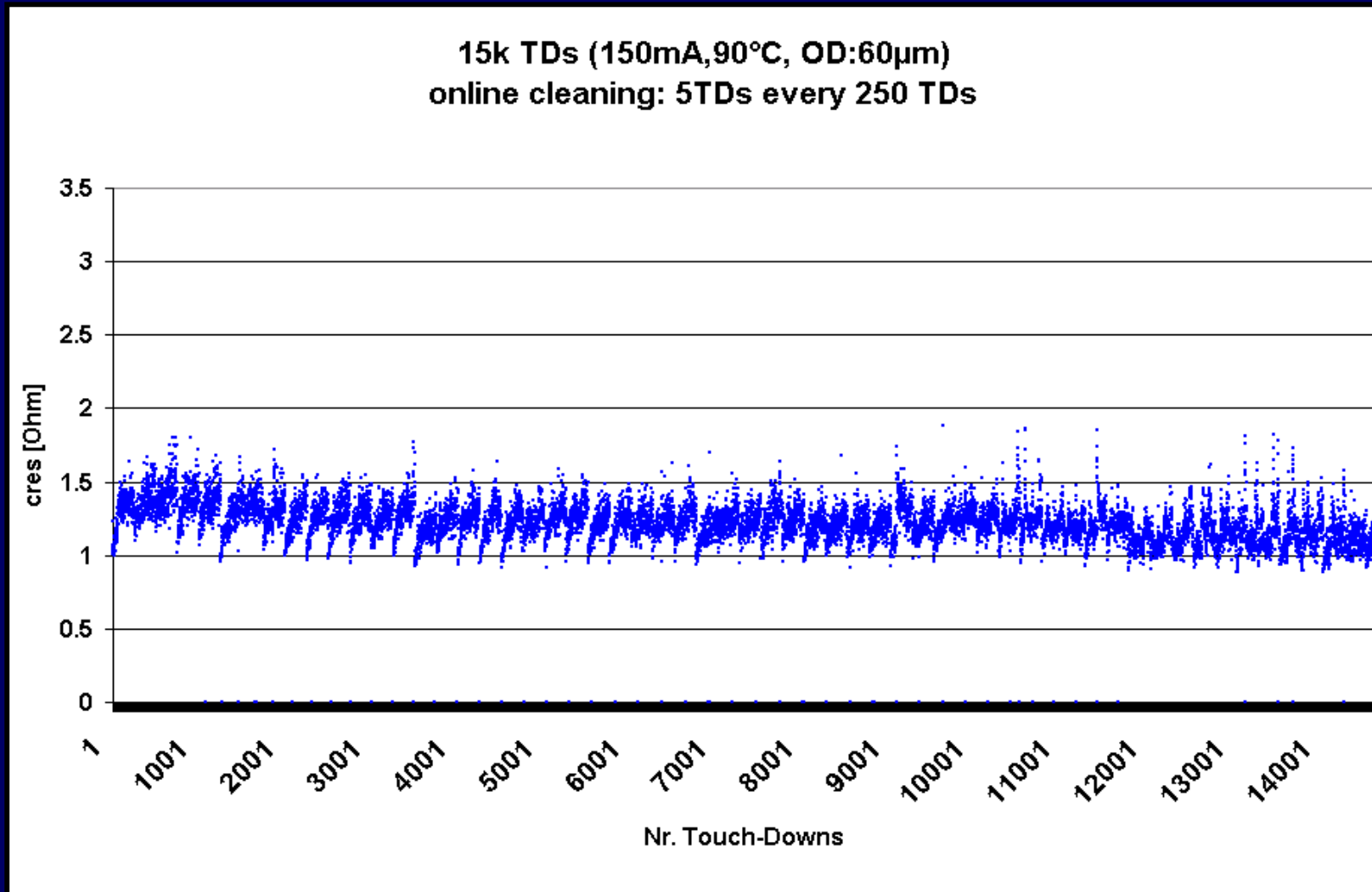
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Measurement Results 1/3



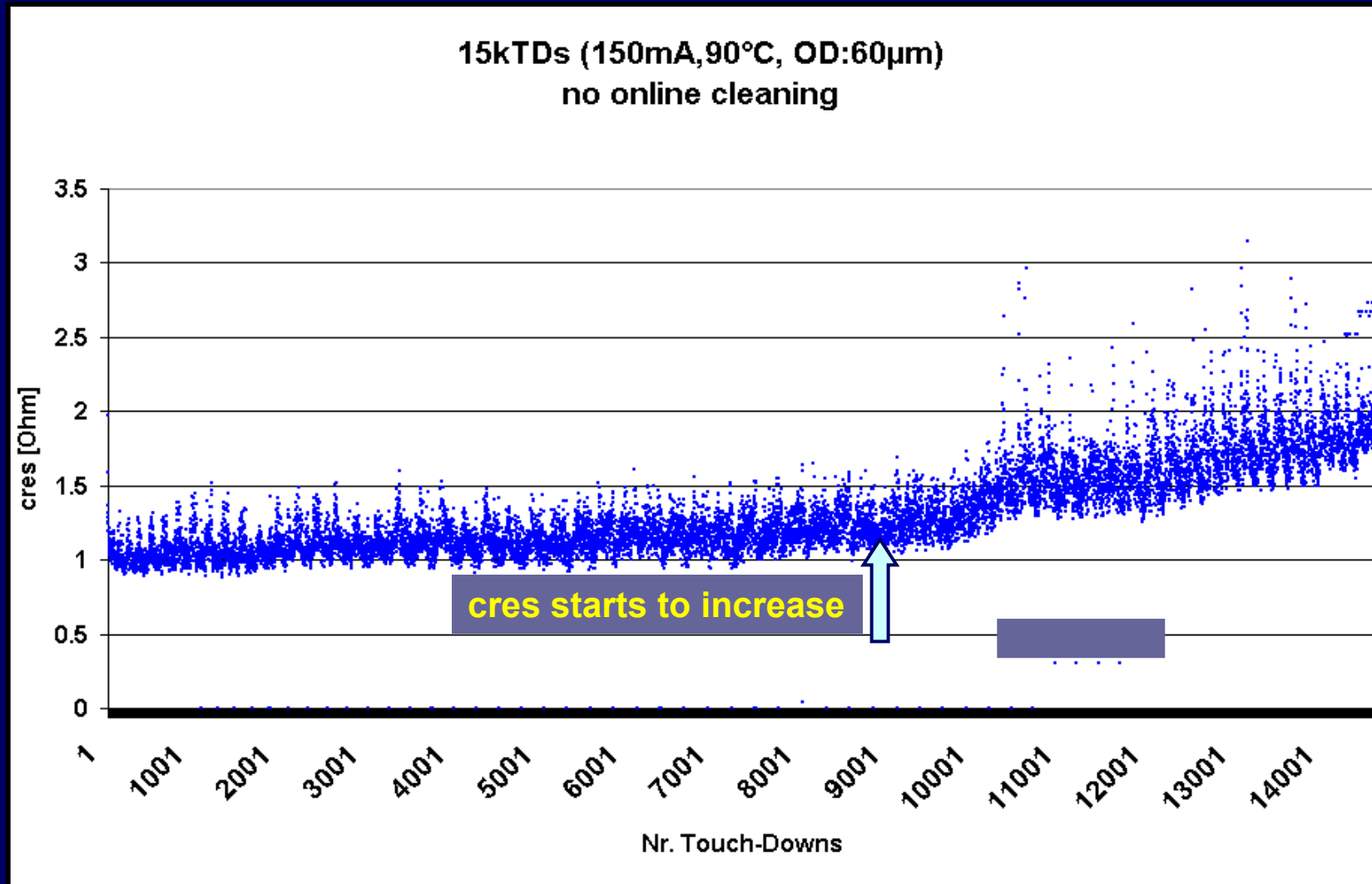
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Measurement Results 2/3



A Test-Setup for Probe-Card Characterization

Measurement Results 3/3



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Summary

- test-setup can identify contact-resistance issues better than using a product (no interpretation of test-data required)
- test setup enables us to assess performance trend of Probe-Cards in an early project phase
- less resources required during evaluation phase (ATE resources and test code development resources)