Celerity Research

Probe and Planarize™ -- Optimizing Bump Shape and Height at Probe

Vada Dean and Tom Nguyen
Southwest Test Workshop 2004

Celerity RESEARCH

Overview

- The Problem -- Flip Chip Device Reliability
- The Solution -- Probe and Planarize™
- Smart PnP Technology™

The Problem

Flip Chip Device Reliability

Flip Chip Device Reliability Issues

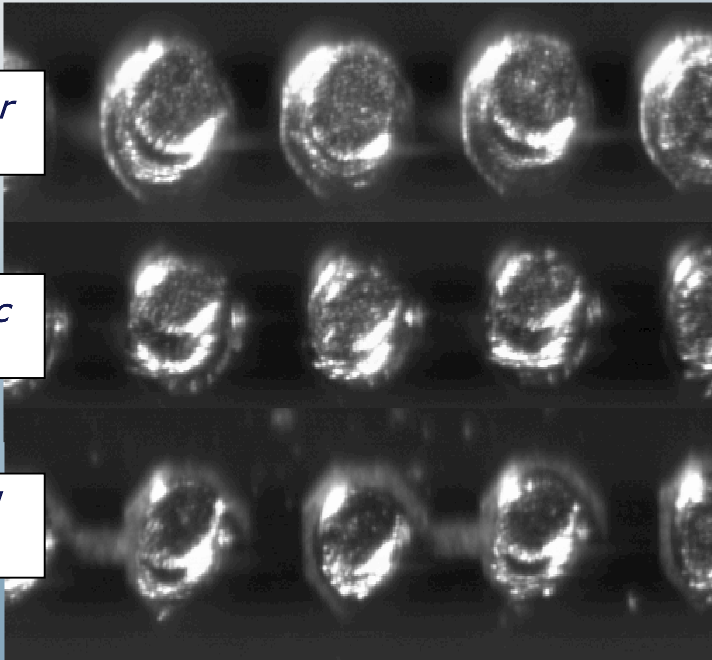
- Probe marks damage bumps on the wafer
- Scratched and penetrated bumps trap contamination and flux
- Bump reflow adds yield risk and cost
- Height variation of wafer bumps hinder interconnect formation

Bump Damage, Contamination and Reflow

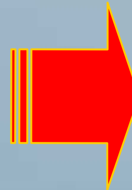
Cu Pillar
60 µ OT

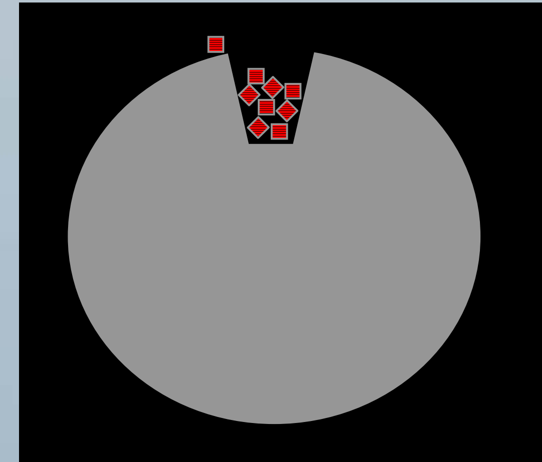
Eutectic
60 µ OT

Hi Lead
60 µ OT



- Trapped contaminants and flux weaken flip chip interconnect joints
- Increases variation of bump height





REFLOW WAFER TO ELIMINATE SOLDER DAMAGE (260°C)

Additional Temp Excursion causes:

- PMOS transistor damage
- Die Yield Loss
- Reduced Final Test Yield
- Additional $’s for wafer reflow process

Typical Bump Height Distribution

1124
1079
849
752
496
381
232
178
94
71
49
25
14
12
6
3
4
1
0
2
1
1
1
0
0
0
0
0
0
1

Chip

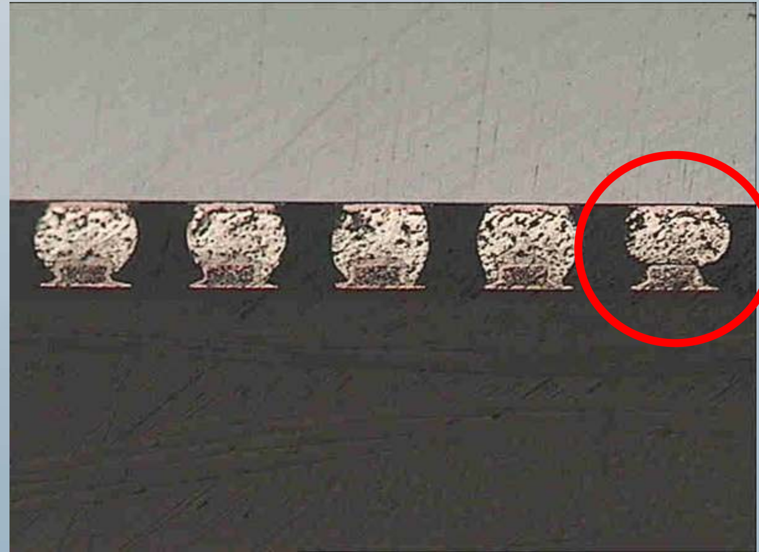
Substrate

113 115 117 119 121 123 125 127 128 131 133 135 137 139 141

Ball Height (microns)

Avg. = 118.77, Sigma = 2.10, Number Balls = 5376

Weak Flip Chip Interconnect



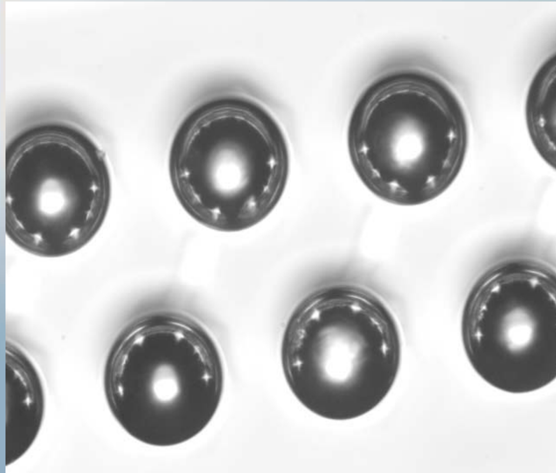
Inferior Interconnect and Lack of Wetting:

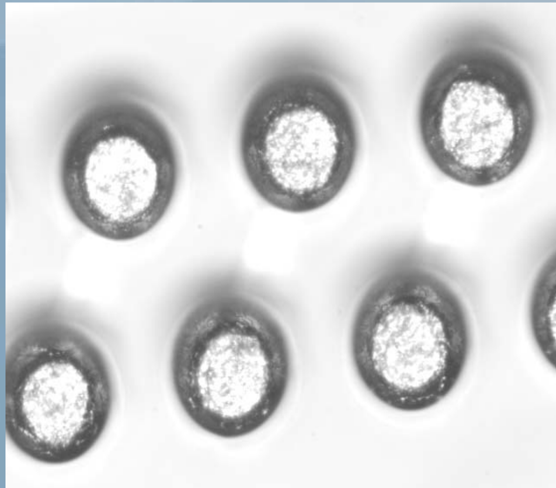
- Smaller ball with little or no contact after reflow
- Contamination interference

The Solution

Probe and Planarize™

Smart PnP Probe™ with Probe and Planarize™



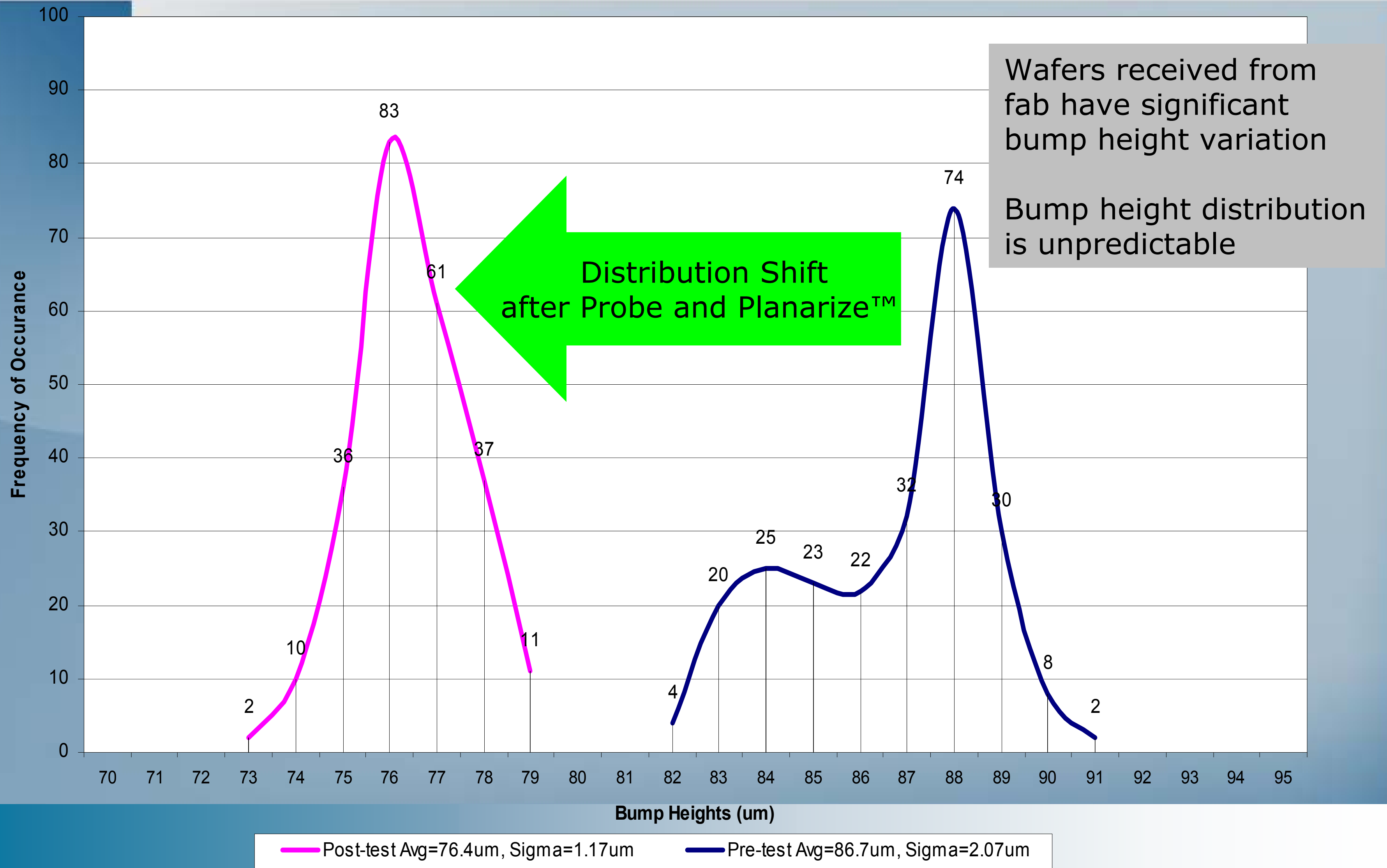


Advantages

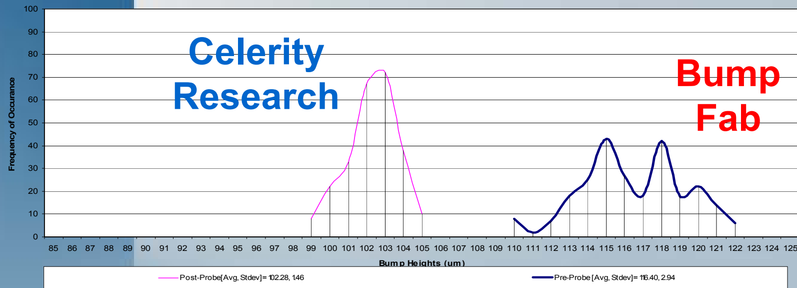
- Reduced variation of bump height enhances interconnect integrity
- Flat surface eliminates trapped contamination and flux
- Textured surface improves reflow and wetting

Probe and Planarize™ uniformly deforms bumps across the wafer

Smart PnP Probe™ Improves Bump Height Distribution



Probe & Planarize™ Results



Vendor A

Lot # 2

High Pb

Before

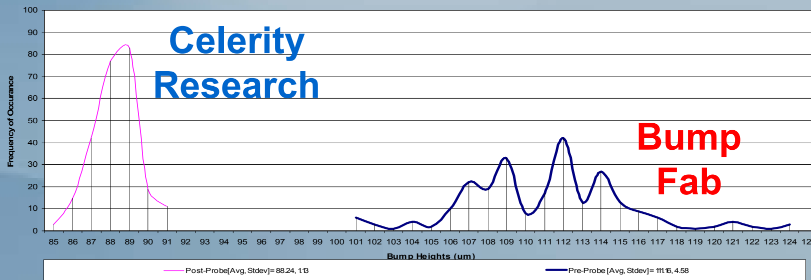
Avg. Bump Ht. = 116.40

Std. Dev. = 2.94

After Probe & Planarize™

Avg. Bump Ht. = 102.28

Std. Dev. = 1.46



Vendor A

Lot # 3

High Pb

Before

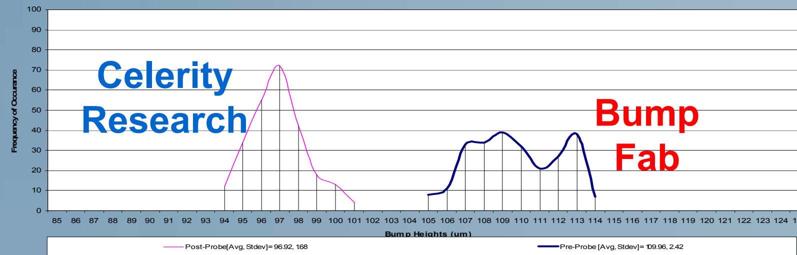
Avg. Bump Ht. = 111.16

Std. Dev. = 4.58

After Probe & Planarize™

Avg. Bump Ht. = 88.24

Std. Dev. = 1.13



Vendor A

Lot # 4

High Pb

Before

Avg. Bump Ht. = 109.96

Std. Dev. = 2.42

After Probe & Planarize™

Avg. Bump Ht. = 99.92

Std. Dev. = 1.68

Probe and Planarize™ Improves Reliability

Non-Planarized
Bump Structure

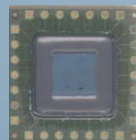
Weak flip chip interconnect joint. Will result in reliability failure of device.

Probe and Planarize™
Bump Structure

Preferred flip chip interconnect joint structure.

Smart PnP Probes™ Reliability Study

	Cu Pillar		Eutectic		High Pb	
	PnP	Control	PnP	Control	PnP	Control
MSL L3	0/600	0/600	0/600	0/600	0/600	0/600
TC-B 4500 cycles	0/100	11/100	0/100	57/100	0/100	52/100
TC-B 3000 cycles	0/250	8/250	0/250	19/250	0/250	11/250
UB-Hast 96 hrs	0/150	0/150	0/150	0/150	0/150	0/150
UB-Hast 168 hrs	0/50	0/50	0/50	0/50	0/50	0/50
HTS 165C 500 hrs	0/50	0/50	0/50	0/50	0/50	0/50

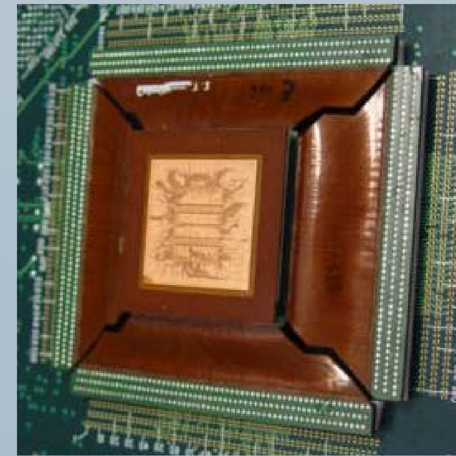


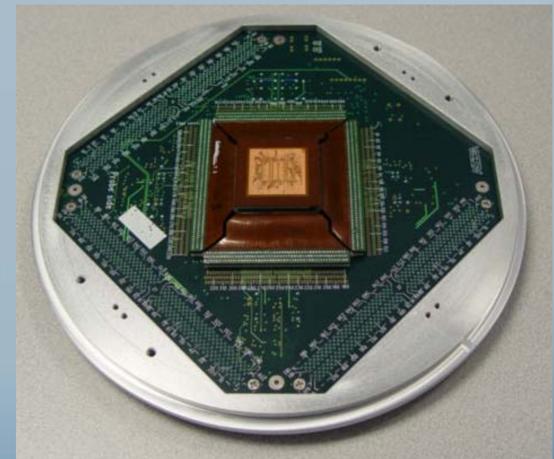
MTBS Daisy Chain (15 x 15 mm die size, Var. pitch 125–240μ)
TF-Polyimide 31 x 31 mm FC-BGA Package
ASE-M / MTBS FC-BGA Assembly Process

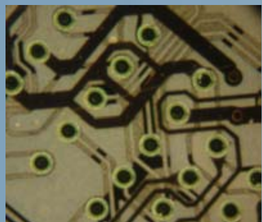
Smart PnP Technology™

Celerity Research Smart PnP Probe™

- Smart PnP Probe™ with unique Probe and Planarize™ technology:
  - High density capability (up to 10000 pins)
  - Fine pitch (60 micron or less)
  - Massively parallel
  - Superior electrical performance
  - The only probe technology that improves the integrity of the flip chip joint interconnect

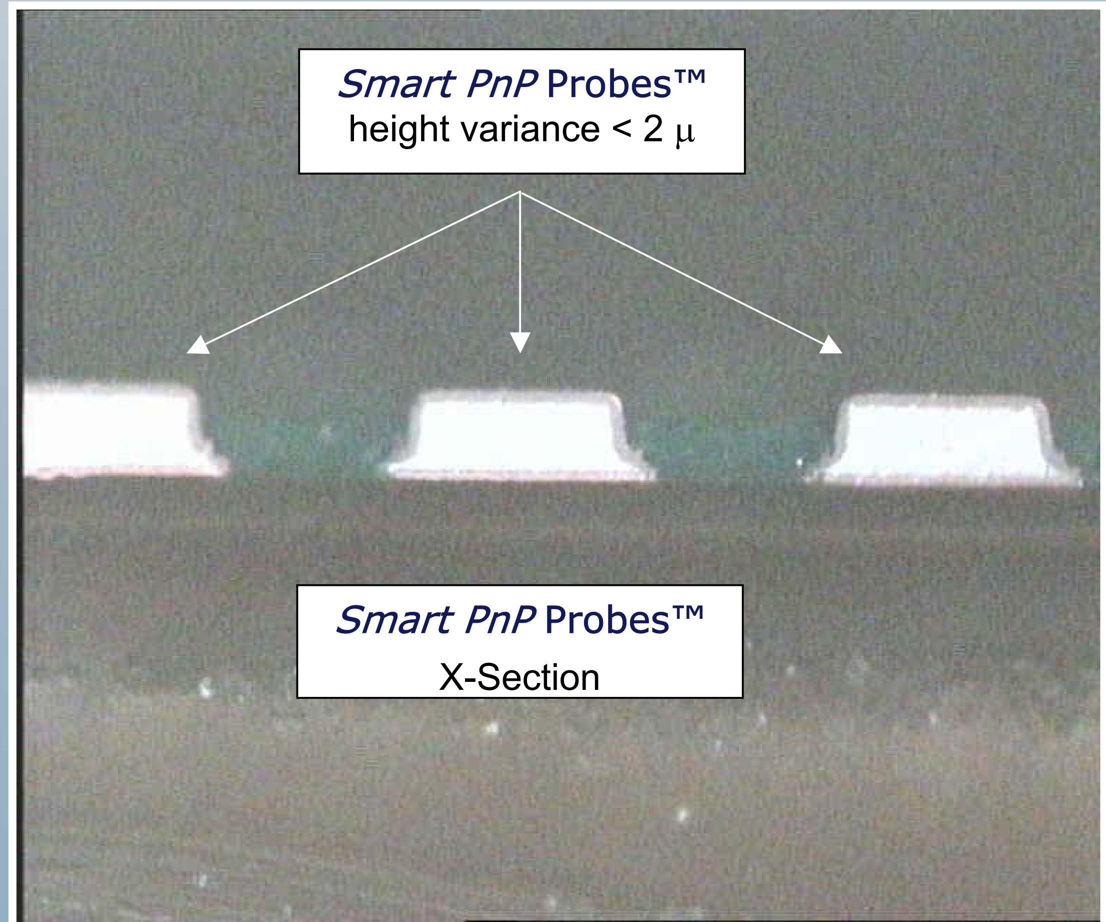






Smart PnP Probes™

- Coplanarity <+/- 2μ.
- Rigid and durable probes



Smart PnP Probe™ Planarity

Coplanarity

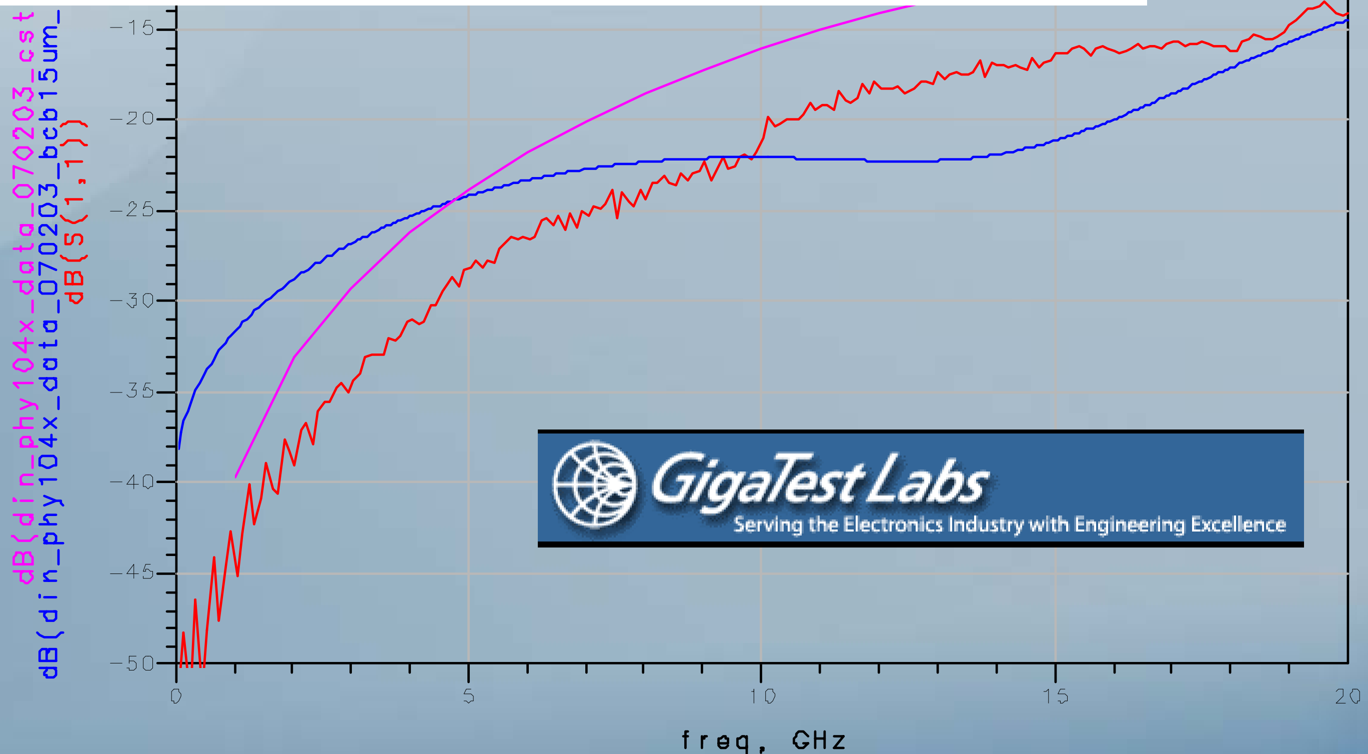
240 Probes Monitored -- Camtek Falcon

Planarity (um): 0.0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5

Touchdowns: 0, 0.5k, 1k, 5k, 10k, 50k, 100k, 500k

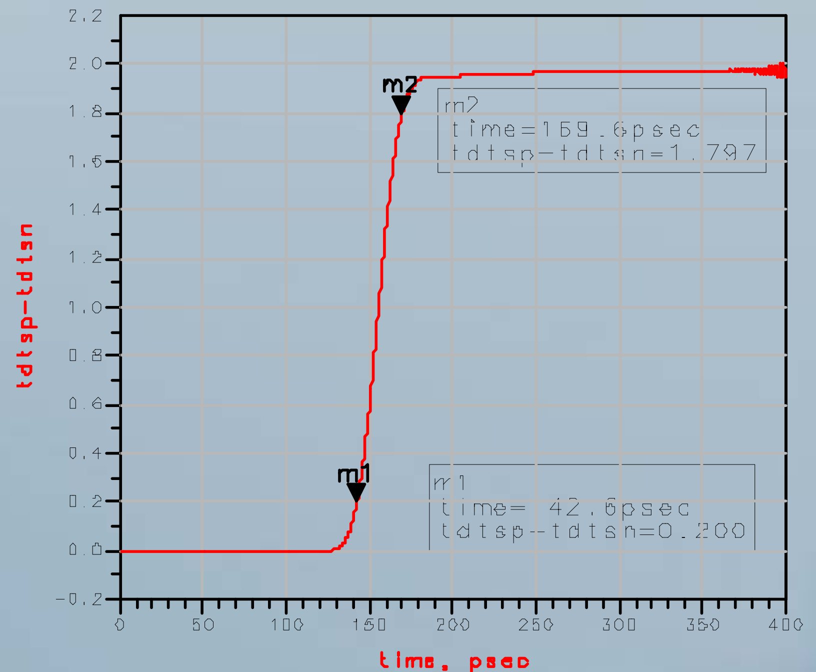
Smart Probe Technology™ Utilizes Advanced Design and Simulation

- Electrical parasitics well defined and modeled with EDA tools and simulators
- Lumped elements can be designed into the *Smart PnP Probe™*



PnP Probe™ TDR/TDT

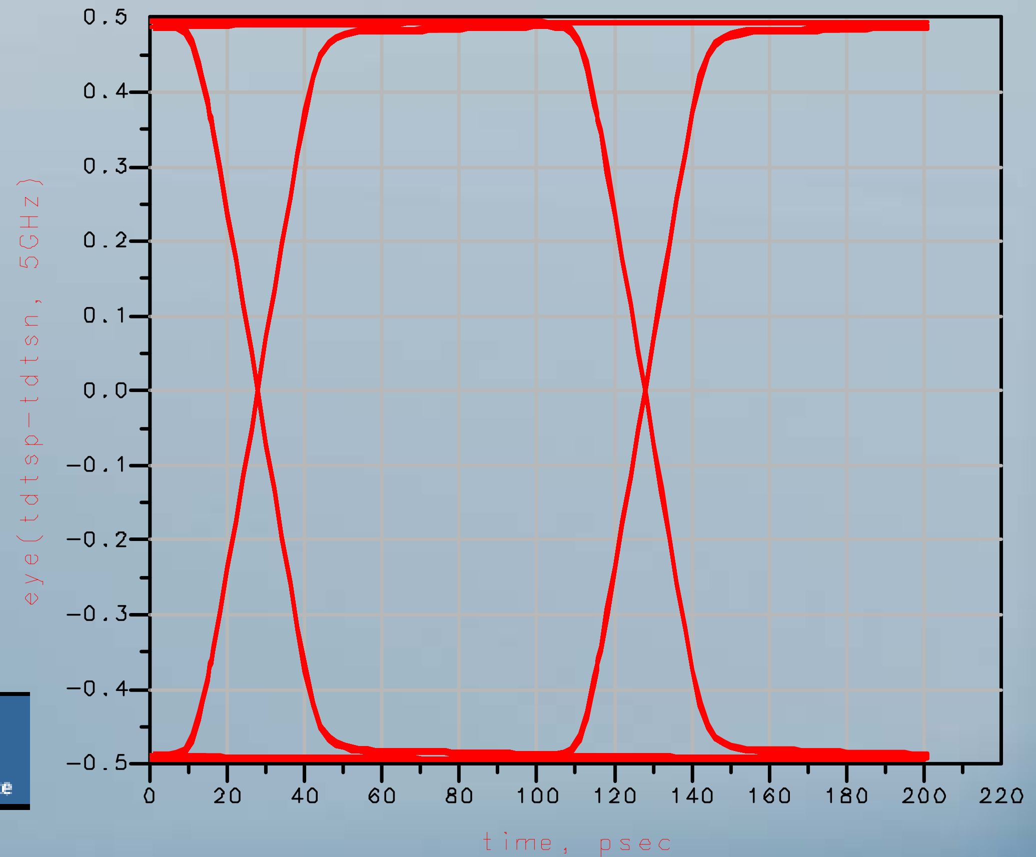
DataIn Pins - Diff TDR/TDT response for 25ps input



Output risetime is 27ps
Skew is less than 0.25ps

Smart PnP Probe™ Eye Diagram

- DataIn Pins
  Eye-diagram at 10 Gb/sec
- Jitter is less than 1ps
- Eye-closure is 6%
  (measured 30ps after zero crossing)



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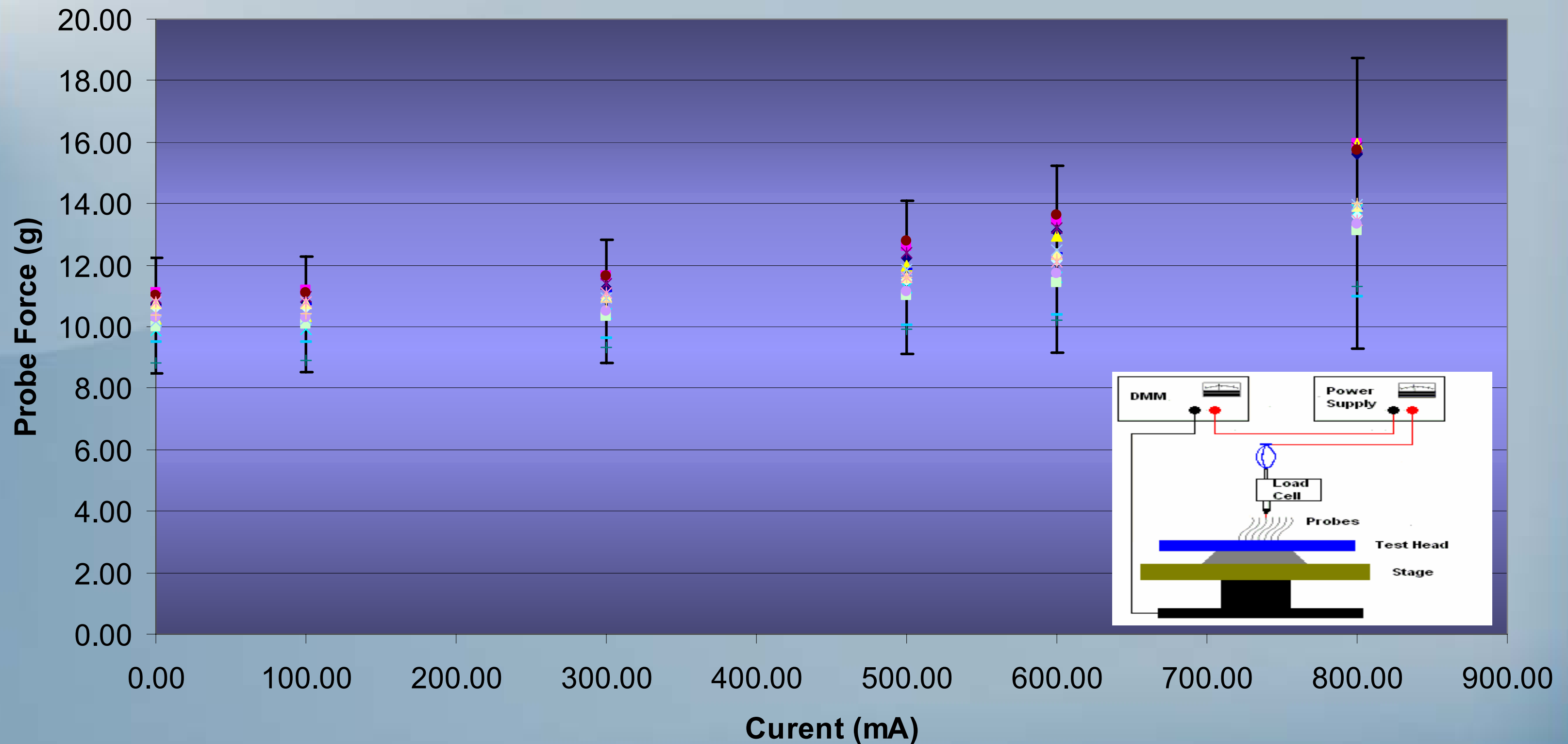
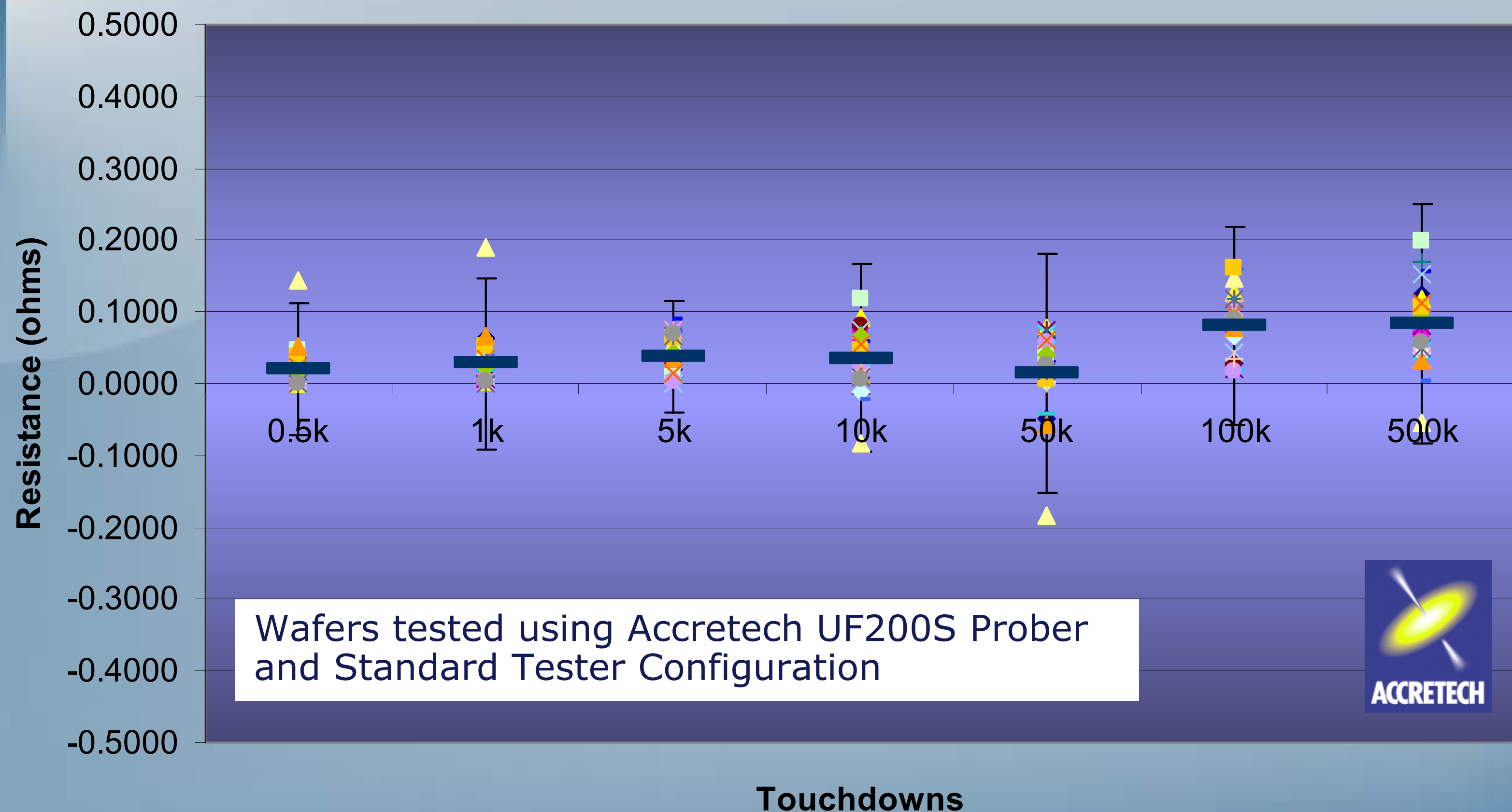
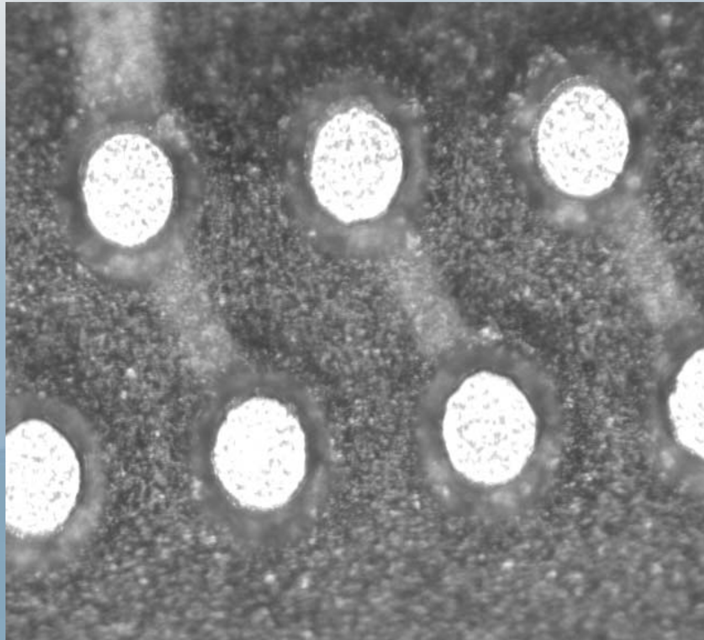
Smart PnP Probe™ Current Capacity



Contact Resistance Performance

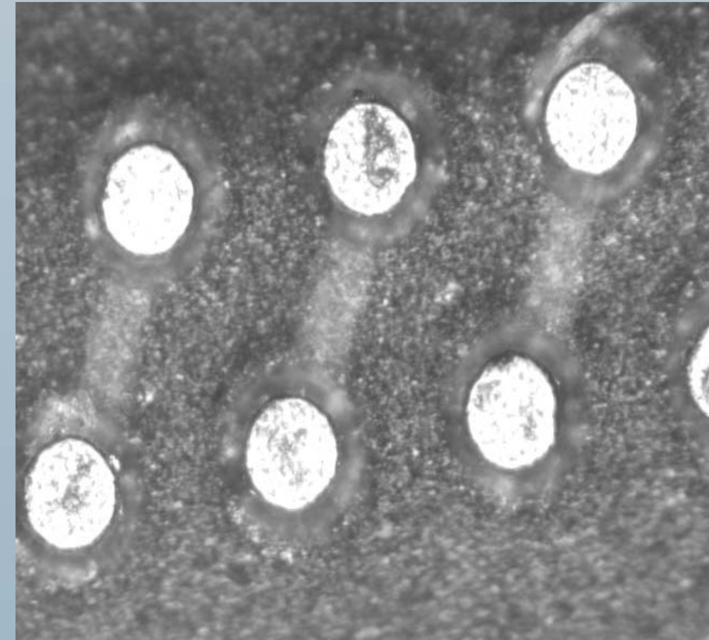


Smart PnP Probe™
Probes After 500k Touchdowns (no clean)



Smart PnP Probe™

Before Touchdown



Smart PnP Probe™

After 500K Touchdowns

Conclusions

- Probe and Planarize™
  - Optimizes Bump Shape and Height at Probe
  - Improves Flip-Chip Device Reliability

- *Smart PnP Technology™*
  - Provides superior coplanarity
  - Maintains advanced electrical performance throughout life of probe card
  - Provides reproducible low C_{res}
  - Enables fine pitch and massive parallel testing

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