SCANIMETRICS Inc.

We measure the heartbeat of computer chips

Wireless Wafer Probe

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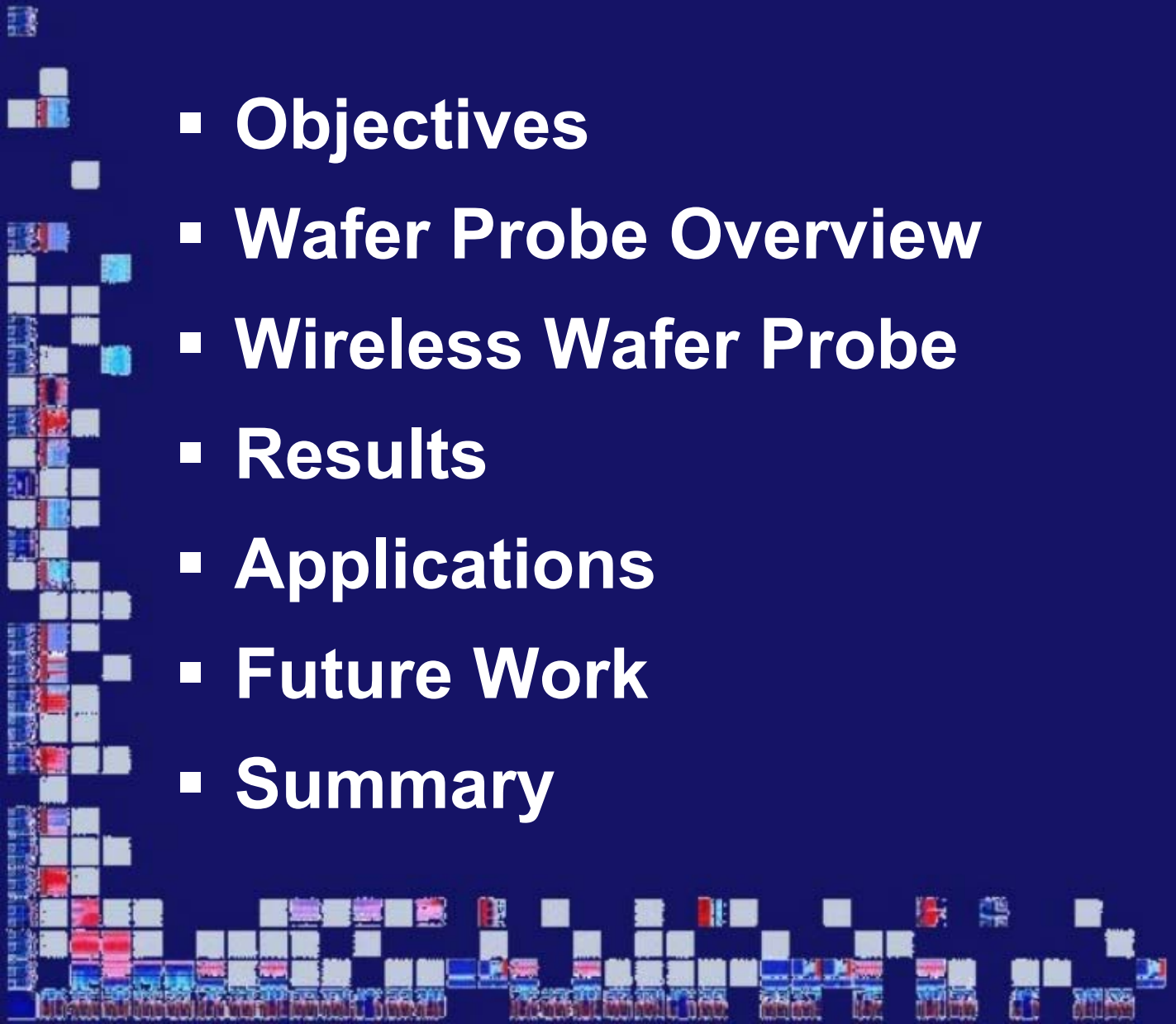
SOUTHWEST TEST WORKSHOP

Outline

- Objectives
- Wafer Probe Overview
- Wireless Wafer Probe
- Results
- Applications
- Future Work
- Summary



Objectives

- Non-contact wafer probing
  - Eliminate scrubbing issues
  - Increase reliability, reduce maintenance
  - Increase yield (front-end and back-end)
- High speeds (Gbps) with high pin counts
- Maintain signal integrity
- Improve price/performance
- Maintain compatibility with existing equipment and processes
- Enable transition to full wafer probing
- Hybrid approach for high power devices

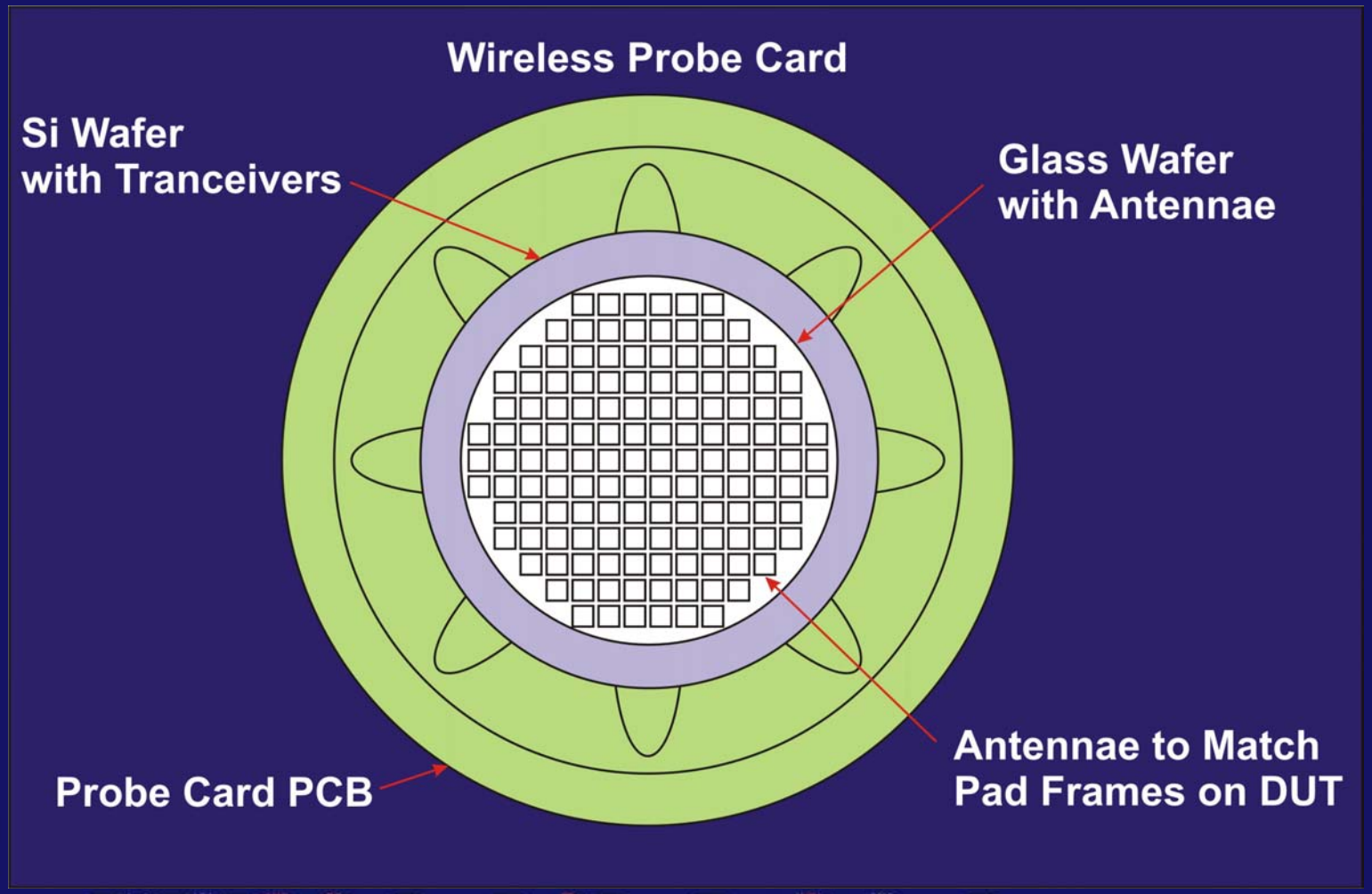
Wafer Probe Overview

- Limitations
  - Support for increased parallelism
  - High contact forces reduce yield
  - High frequency testing at high pin counts
  - Reliability (up to 10% retest)
  - Automated manufacturability (manual assembly required)
  - Maintenance and cleaning of probe cards
  - Probing chips made with new materials (e.g. low-k dielectrics)
  - Scaling as pad pitch and size decreases

Wireless Wafer Probe

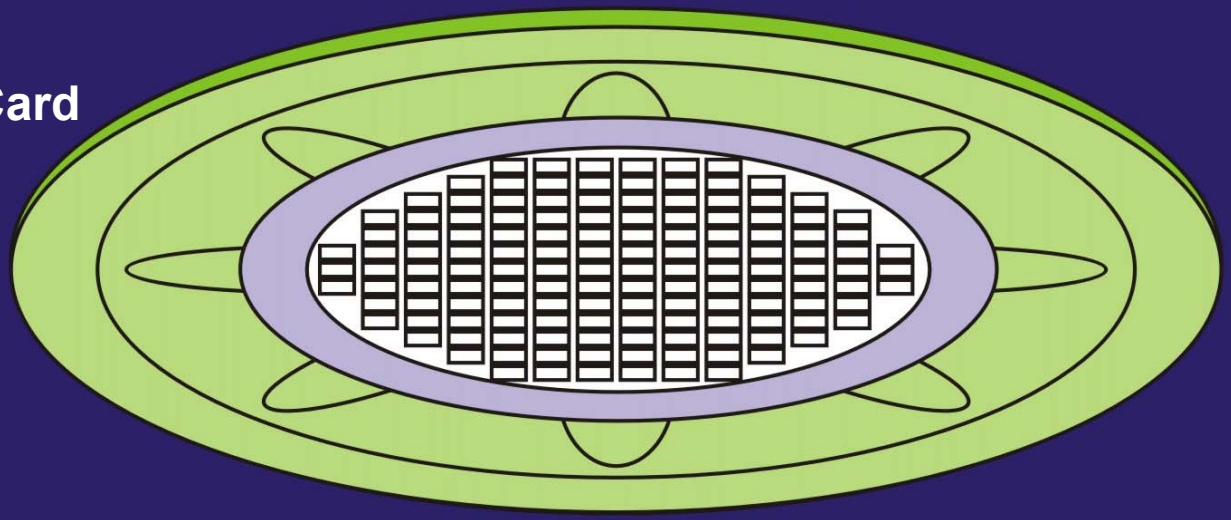
- Eliminates contact force and scrubbing issues
- Increased test speeds (Gbps) at high pin counts
- Good signal integrity
- Enables increased parallelism up to full wafer probing
- Automatic alignment capability with less alignment accuracy requirements
- Significantly reduces need for re-test
- Supports internal test points with no ESD protection requirements (less chip real estate usage)
- Compatible with existing equipment and processes
- Capability to work with new materials (low-k dielectrics)

Wireless Probe Card

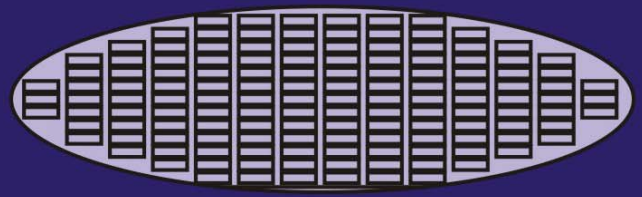


Wireless Wafer Probe

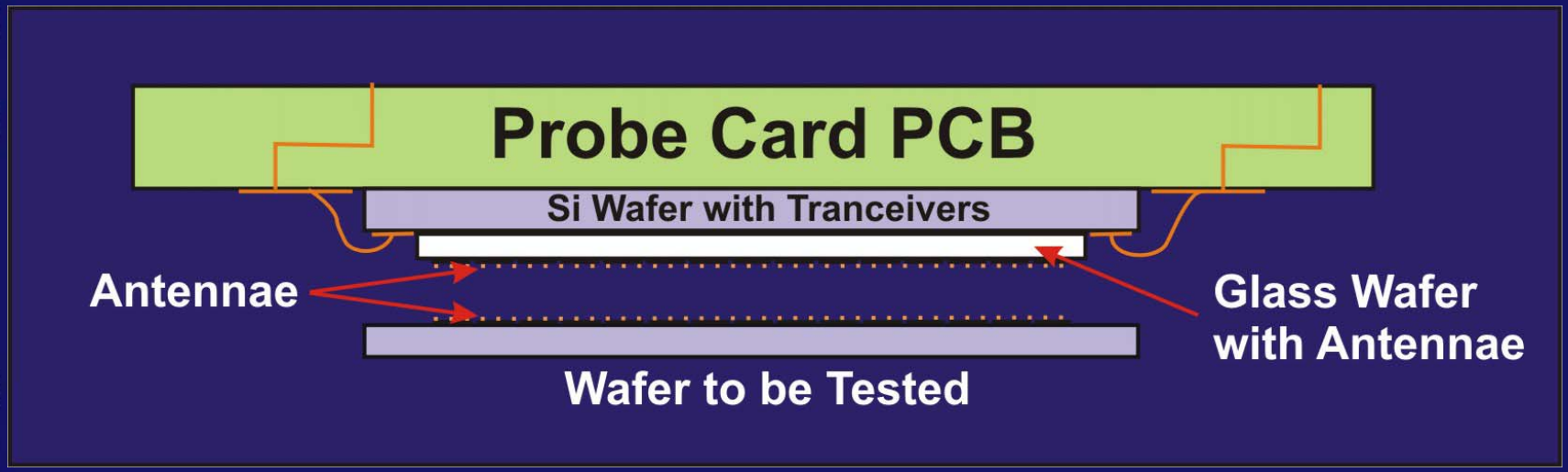
Wireless Probe Card



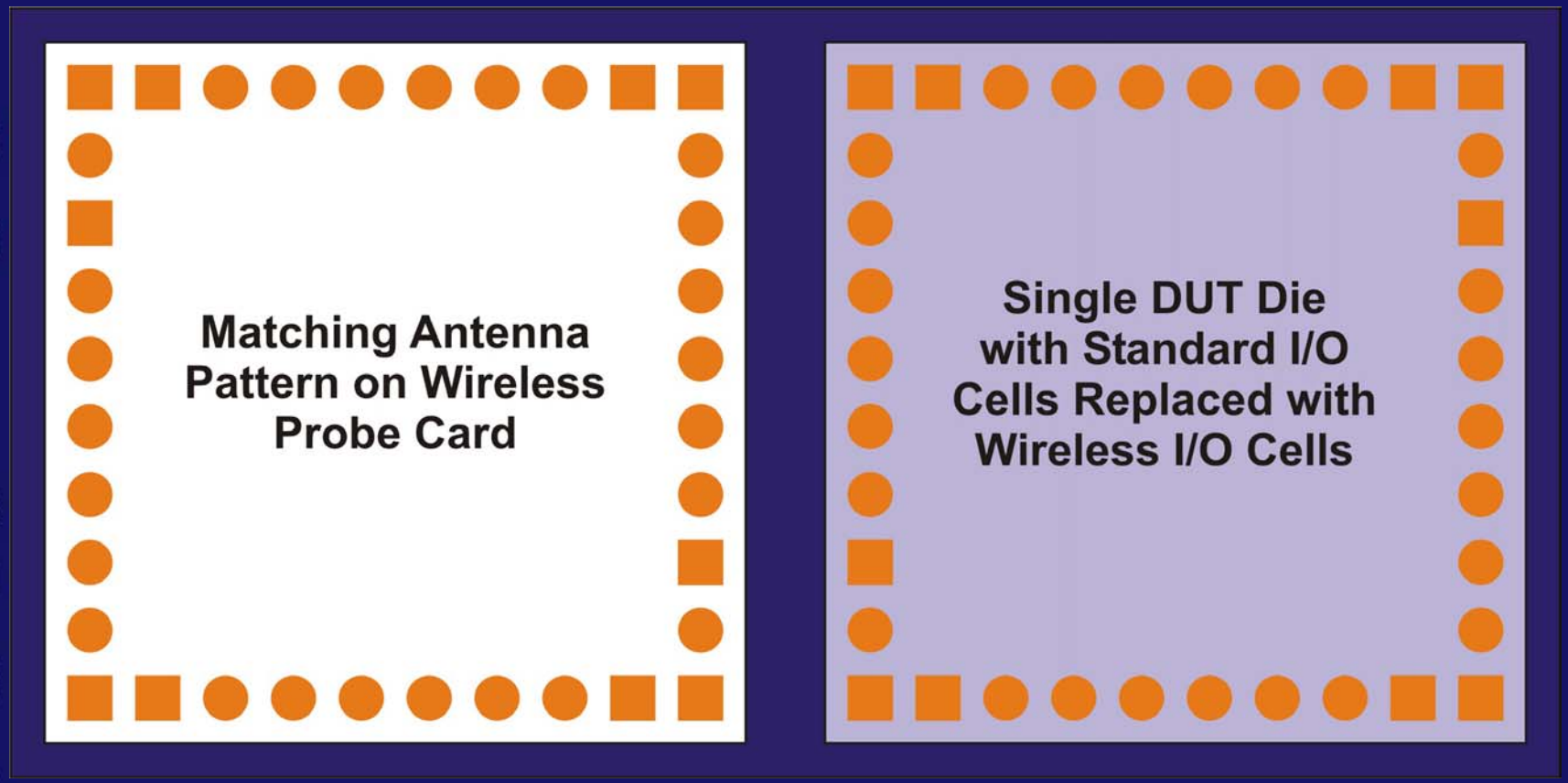
Wafer to be Tested



Wireless Probe Card



Wireless Probe Card

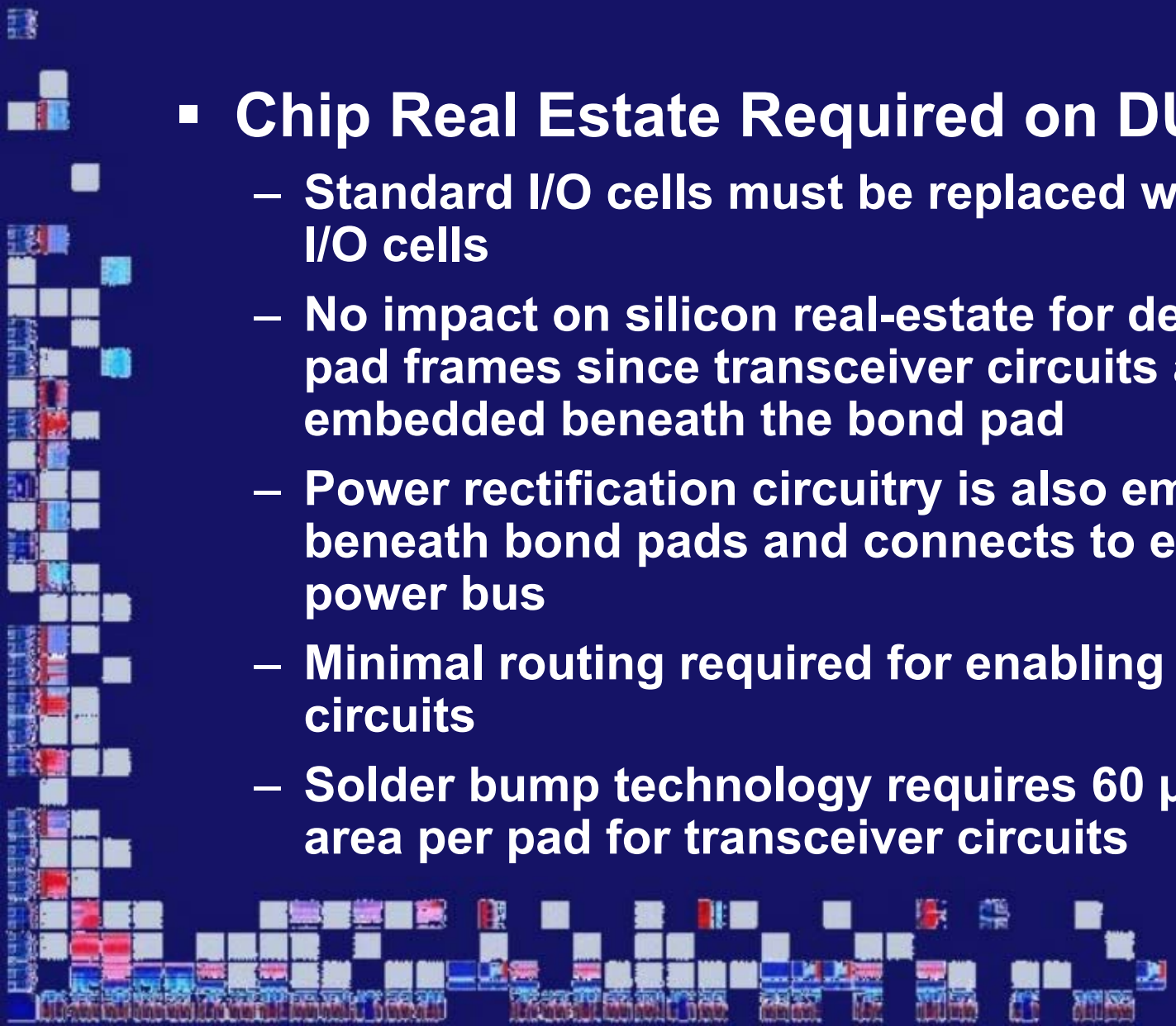


Wireless Probe Card

- Specifications
  - Probe separation distance < 100 µm
  - Antennae for data communications
  - Separate antennae for power transfer
  - Bi-directional communication at Gbps
  - Power delivery of few hundred mW per pin
  - Probe pitch scales down to 35 µm
- Performance Impact
  - Power to transceivers disabled after test
  - Single transistor loading per I/O site

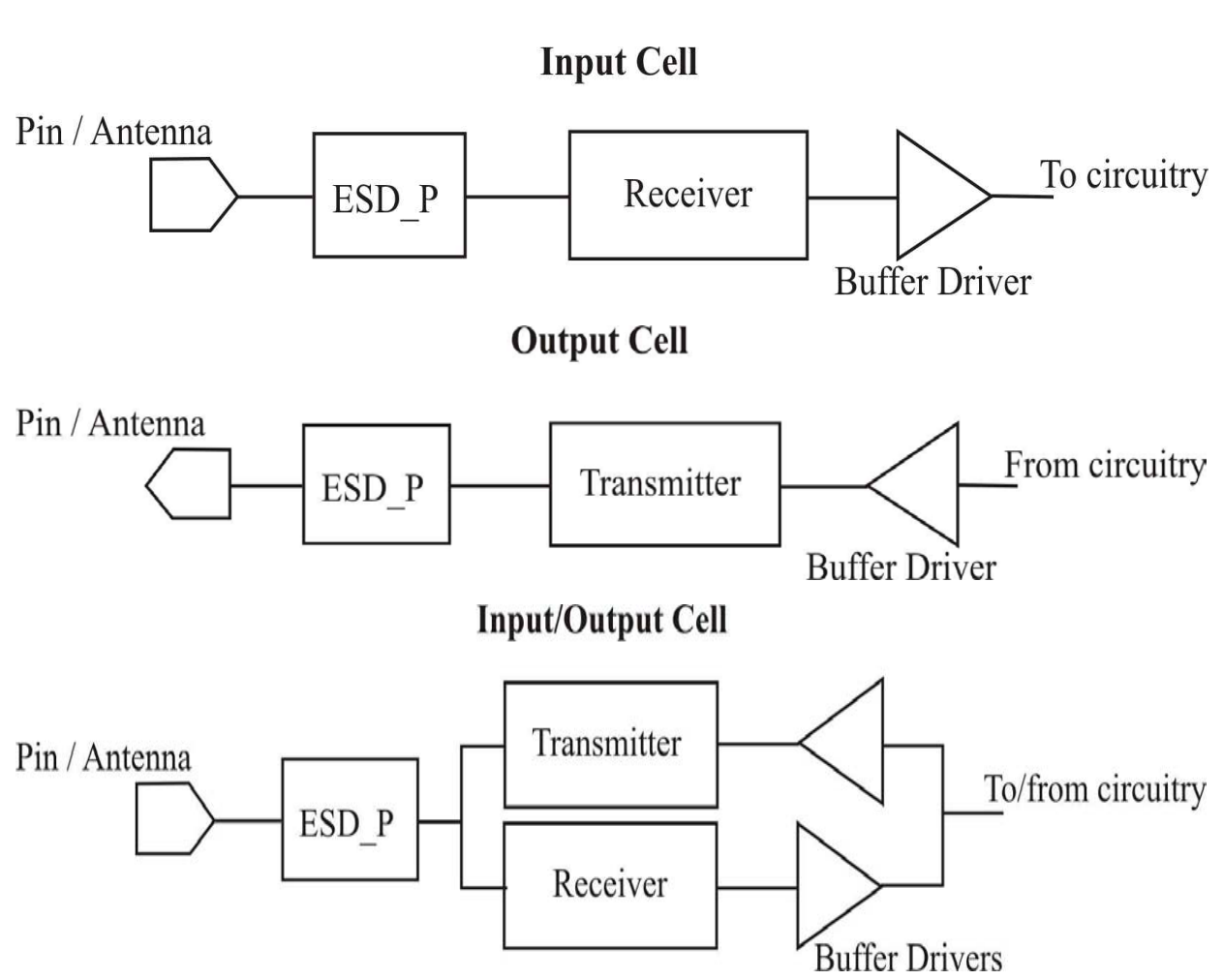
Wireless Probe Card

- Chip Real Estate Required on DUT
  - Standard I/O cells must be replaced with wireless I/O cells
  - No impact on silicon real-estate for devices with pad frames since transceiver circuits are embedded beneath the bond pad
  - Power rectification circuitry is also embedded beneath bond pads and connects to existing power bus
  - Minimal routing required for enabling transceiver circuits
  - Solder bump technology requires 60 µm x 60 µm area per pad for transceiver circuits



Wireless Wafer Probe

- ESD_P is electro-static discharge protection
- Clocked transmission gates are not shown
- Minimal real estate for the transmitter and receiver circuitry

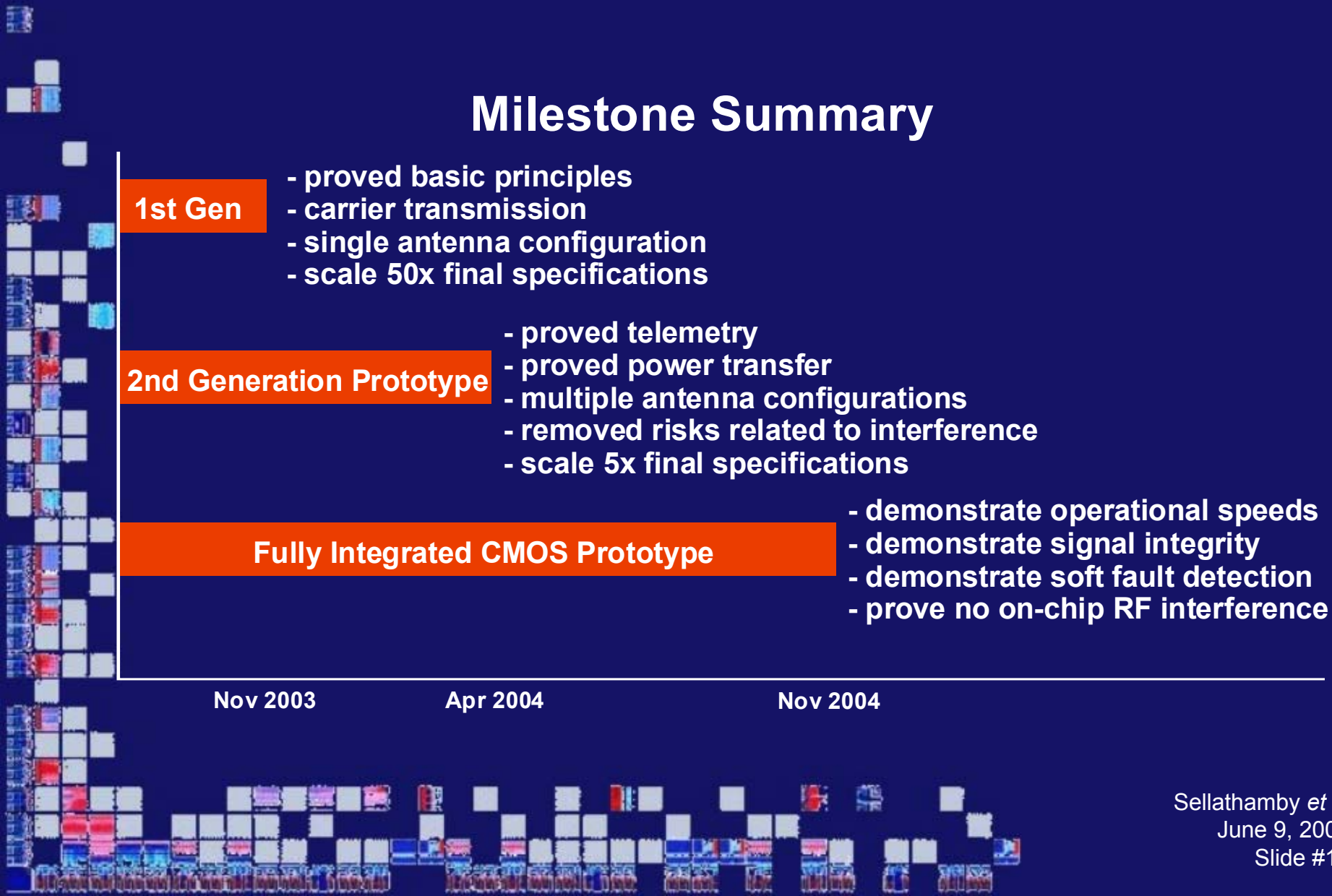


Wireless Wafer Probe

- Hybrid Solution for High Power Devices
  - Contact probes for power
  - Wireless probes for data
  - Redundancy of power pins in hybrid solution eliminates need for multiple touchdowns
  - Hybrid approach uses silicon micromachined probes

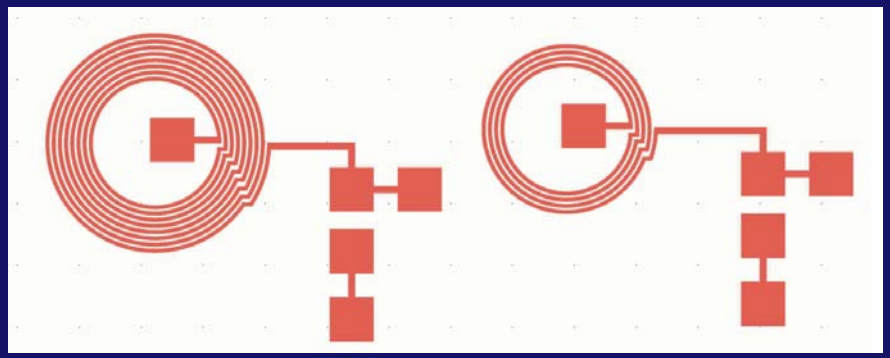
Wireless Wafer Probe

Milestone Summary



Results – First Generation

- 50 µm features
- Frequencies in the range 0.5 – 1 GHz
- Near-field coupling
- Power delivery through antenna
- Powered up electronics on DUT
- Transmitted sideband signals to probe
- CMOS compatible



Aluminum 0.53µm

Borosilicate glass substrate

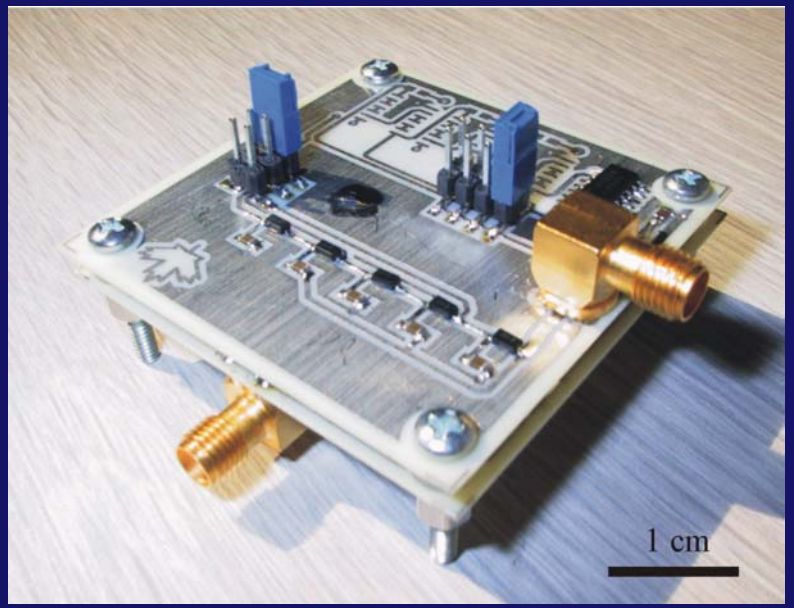
Aluminum 0.53µm

Thermal Silicon dioxide (1.6 µm)

Silicon substrate

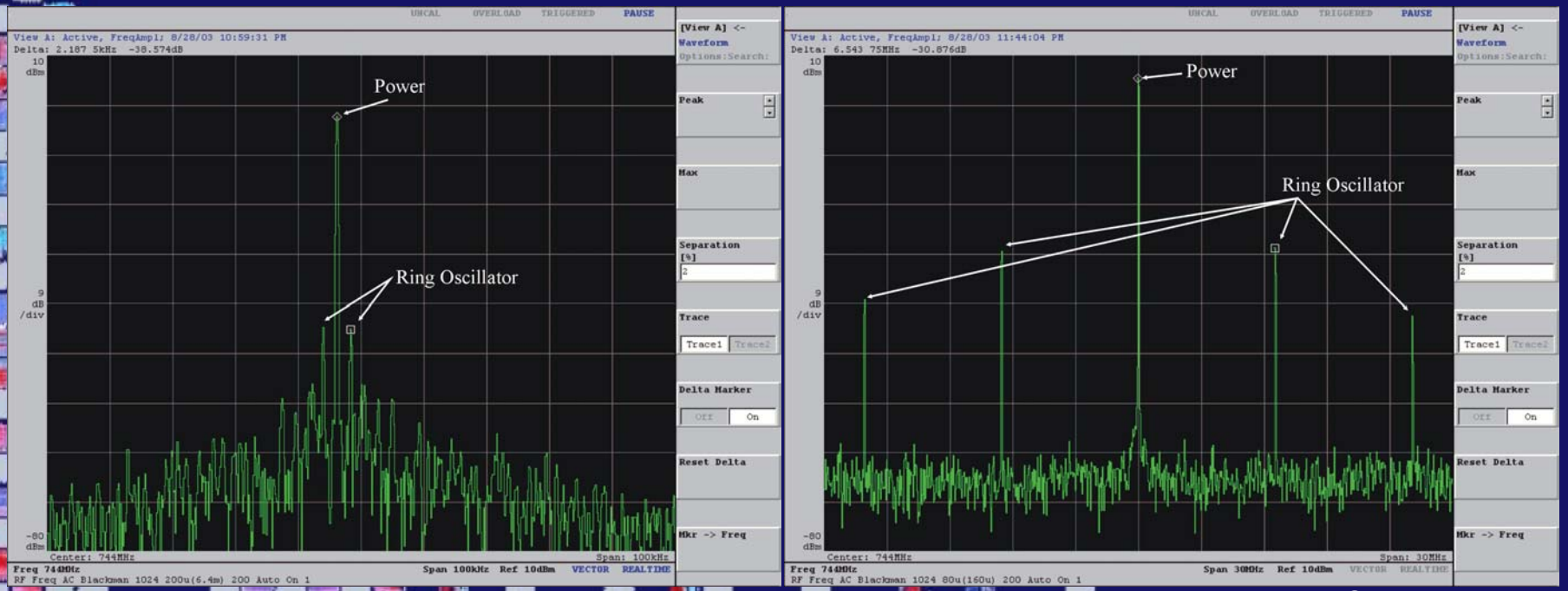
Results – First Generation

- Overall antenna dimensions: ~2800 to 3500 µm
- P_{in} (min) is 12.7 dBm or 1.15 V_{CC}
- Antenna die mounted on RF PCB
- 3.3V CMOS components on PCB



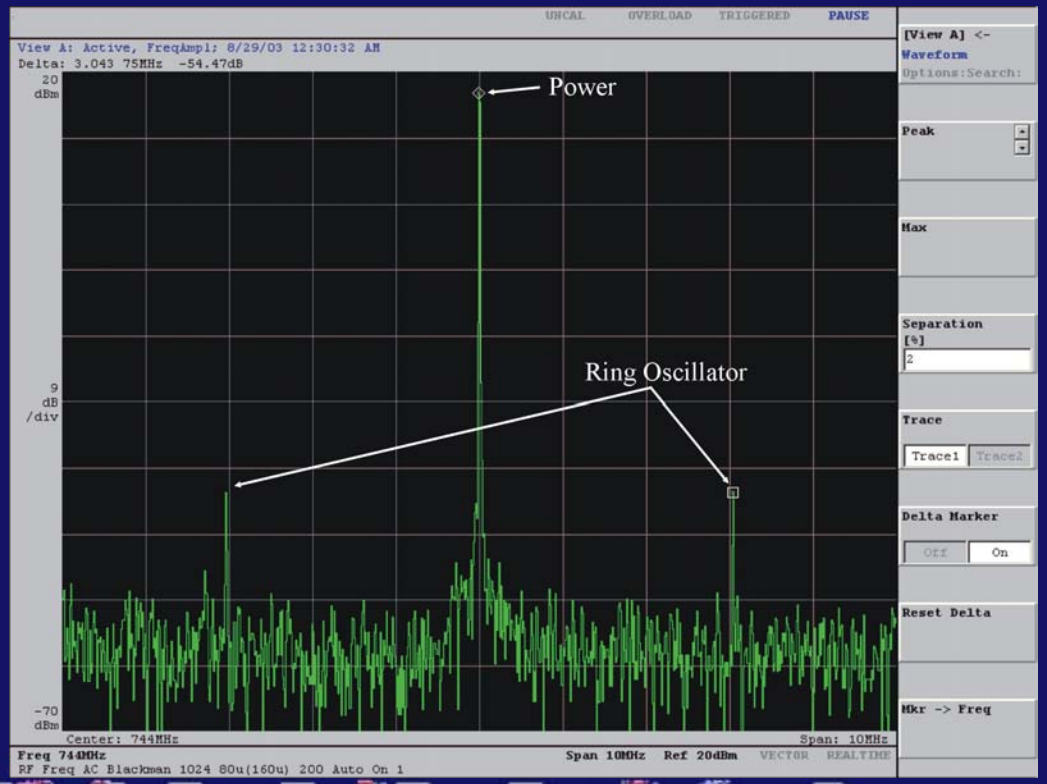
Results – First Generation

- Left figure: turn on of ring oscillator (12.7 dBm)
- Right figure: ring oscillator at full operation (20.0 dBm)
- Ring oscillator frequency proportional to VCC
- Centre freq = 744 MHz, Sidebands at +/- 3.0 MHz



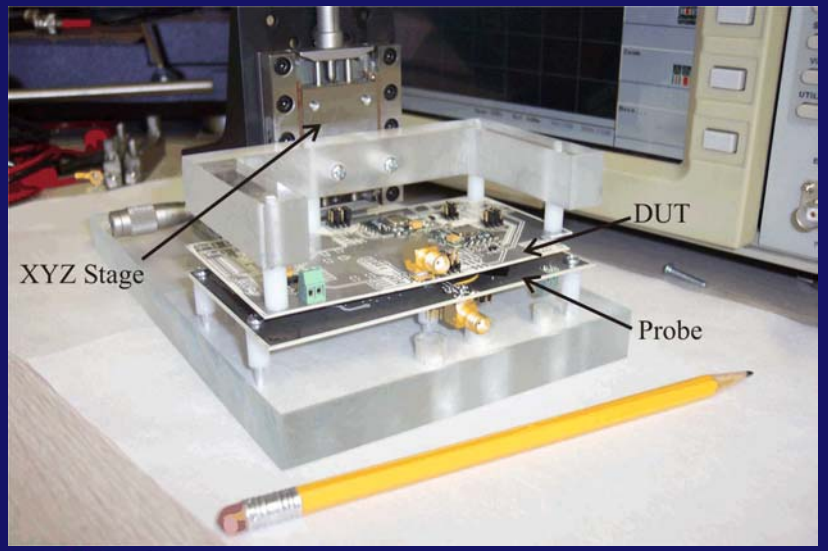
Results – First Generation

- Ring oscillator signal transmitted back to probe
- Sidebands 15 - 20 dB above ambient

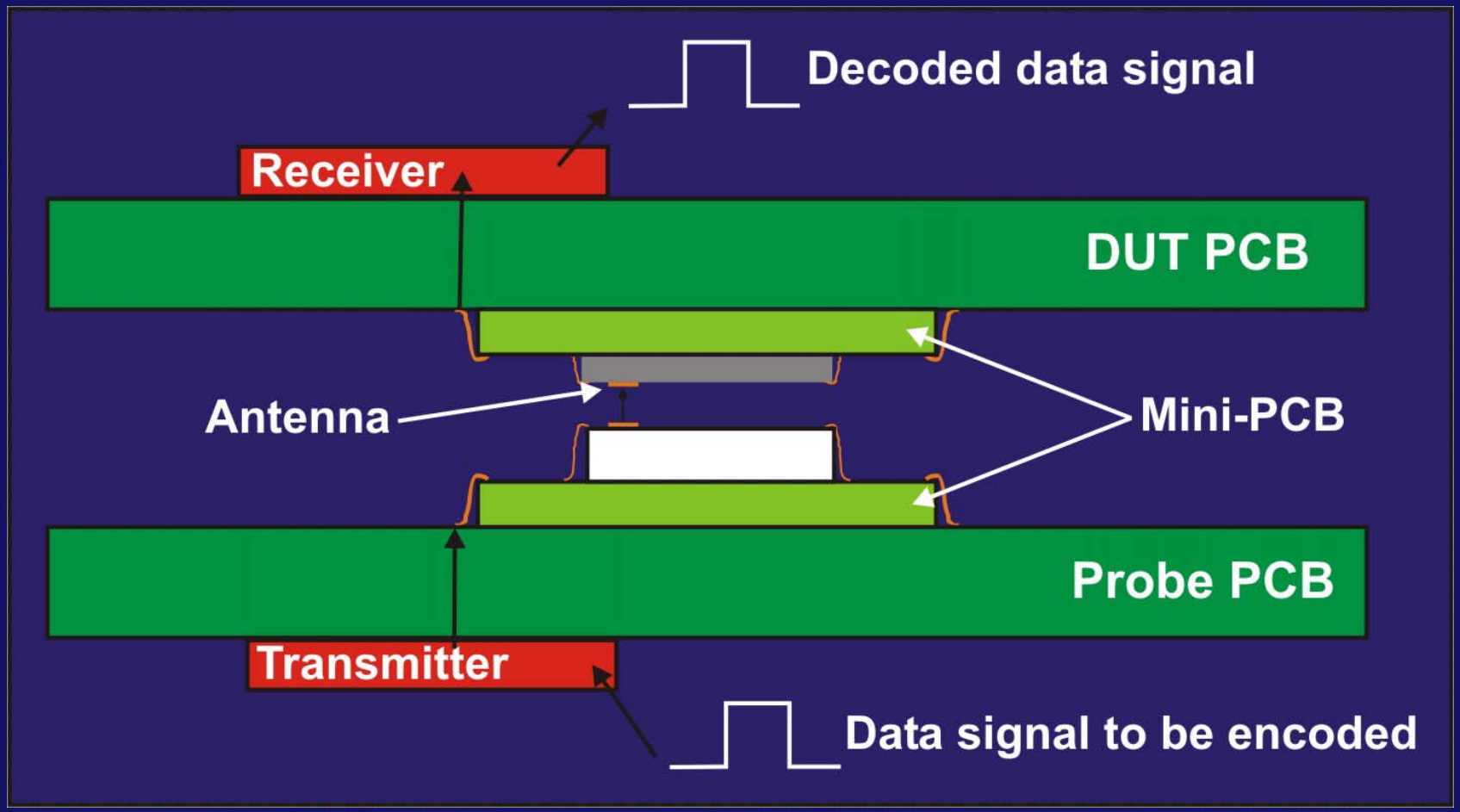


Results – Second Generation

- Reduced antenna size by up to 28x
  - Antenna feature sizes of 5 µm
  - Antenna dimensions of 100 – 1000 µm
- Demonstrated that technology can be scaled
- Created elementary I, O, and I/O cells for demonstration
- Demonstrated bi-directional data communication with multiple antennae
- Demonstrated power transfer to DUT
- Proved that cell-to-cell interference is not an issue
- Demonstrated that there is no interference with nearby electronic circuitry

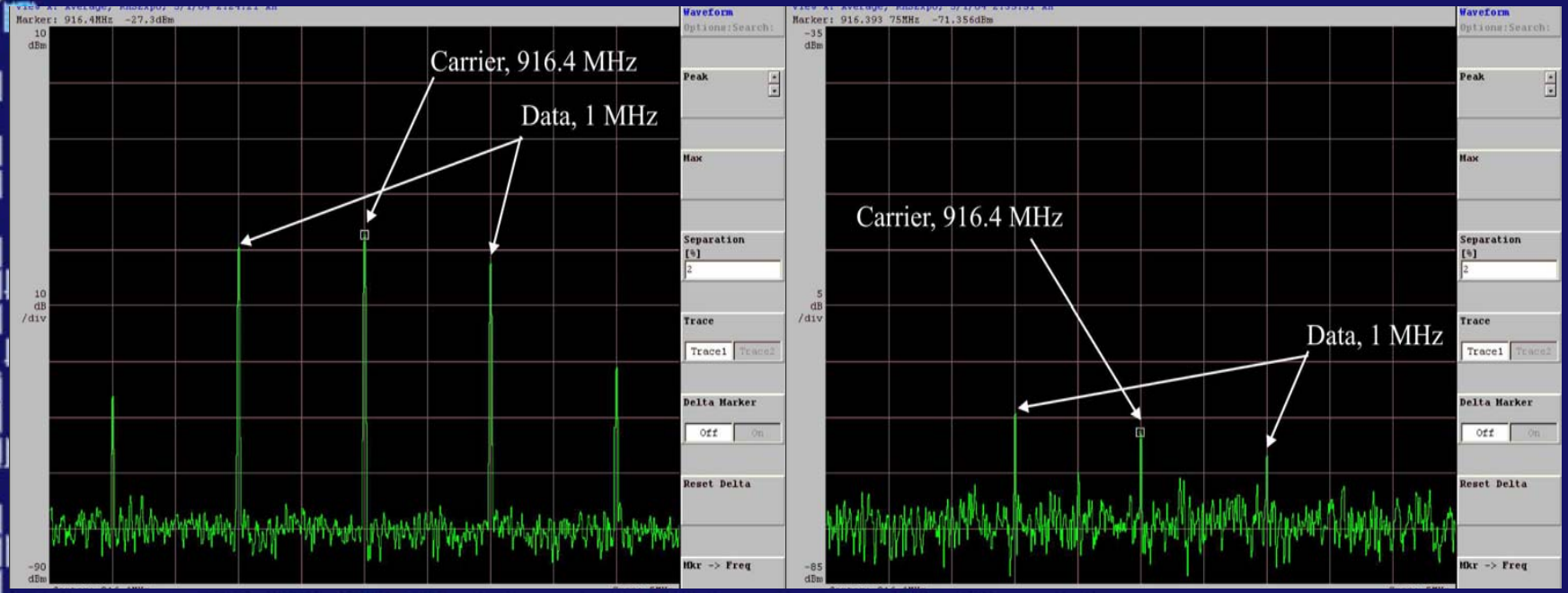


Results – Second Generation



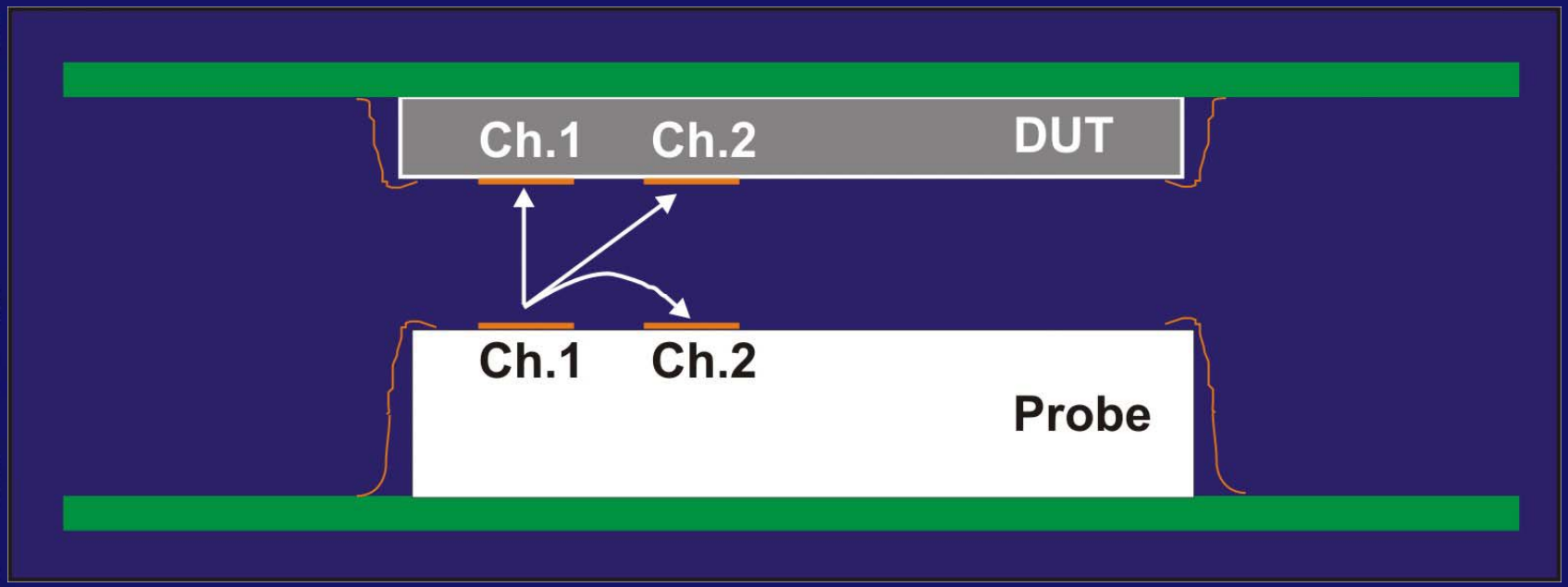
Results – Second Generation

- Amplitude modulated: 916 MHz carrier, 1 MHz data
- Left figure: transmitted spectrum from probe
- Right figure: received spectrum at DUT



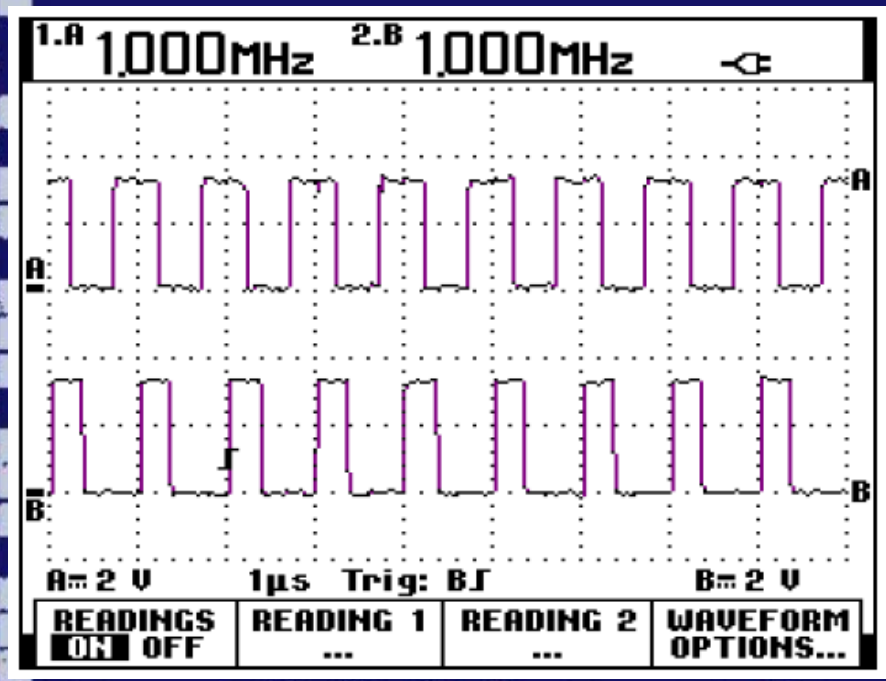
Results – Second Generation

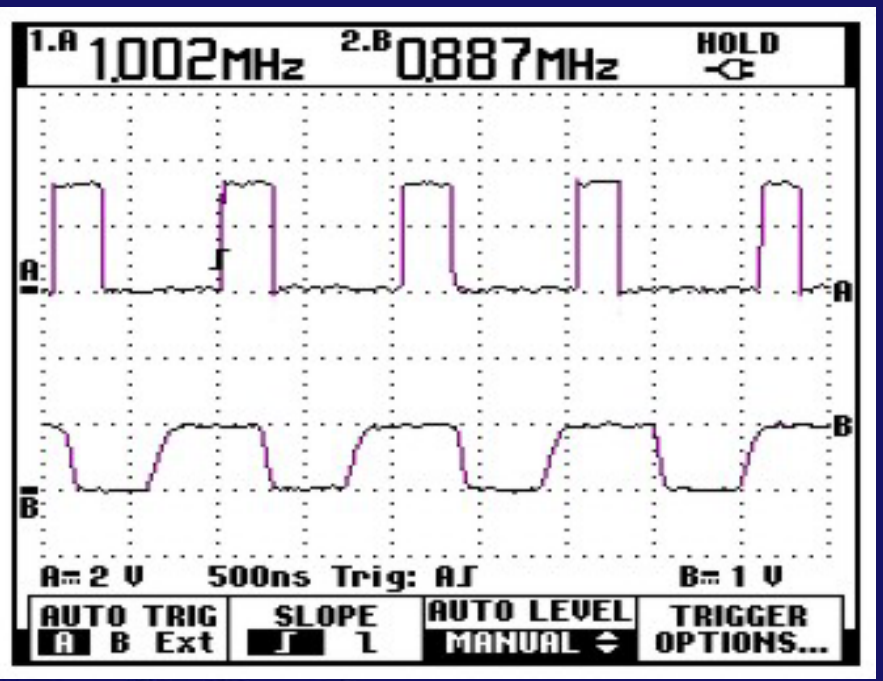
- Initially multiple receivers detected single transmitter
- Interference eliminated by:
  - Reducing transmit power to 1 μW for data channels
  - Reducing receiver sensitivity



Results – Second Generation

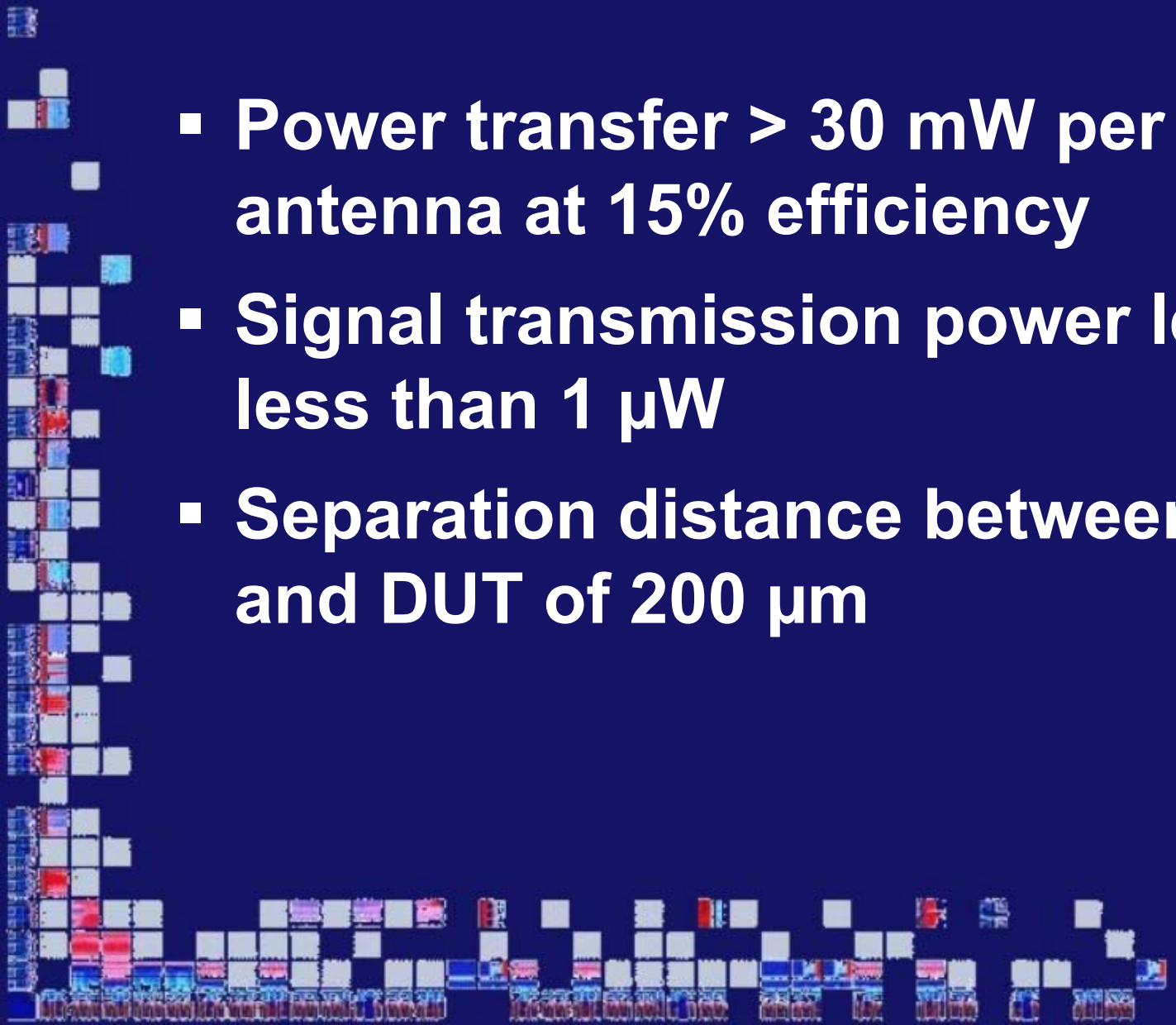
- Simultaneous data Tx, Rx, and power with four separate antennae
- Top left waveform: 1 MHz data signal before modulation and transmit
- Bottom left & top right waveform: 1 MHz demodulated signal at DUT
- Bottom right waveform: ring oscillator on DUT wirelessly powered





Results – Second Generation

- Power transfer > 30 mW per antenna at 15% efficiency
- Signal transmission power levels less than 1 μW
- Separation distance between probe and DUT of 200 μm



Wireless Wafer Probe

- **Technology Risks Addressed**
  - **Scaling risk:**
    - **Proved signal I/O down to 100 µm**
    - **Extrapolation of results confirm scaling to 35 µm pads**
  - **Real estate:**
    - **Simulated transmitter circuits in 0.18 µm (30 µm x 30 µm)**
    - **Designing receiver circuits in 0.18 µm (30 µm x 60 µm)**
    - **Simulated performance of 1 Gbps data rates**
  - **Power delivery:**
    - **Proved power delivery using 300 µm antennae**
  - **RF interference:**
    - **Proved pad to pad interference is minimal & manageable**
    - **Data transmit power reduced to microwatts eliminating radiation effects on circuit function and performance**

Wireless Wafer Probe

- Technology Risks Being Addressed
  - Signal integrity
  - Clock delivery and/or recovery
  - Soft fault detection (parametrics)
  - Effects of the wireless I/O cells after wafer probe (loading effects)
  - Performance of contact probes in a hybrid solution used for high power devices

Applications

- Wafer probe / Functional Test
- PCM / E-Test / Parametric Test
- Chip-Scale Communications
  - Inter-die communication
  - Intra-die communication
  - Die-to-PCB communication
- Wireless Buses
- Probing of Mixed Signal Systems

Future Work

- Third Generation Prototype
  - Timeframe: November 2004
  - Fully integrated CMOS design (TSMC 0.18 µm)
  - Reduce antenna size by an additional 2x
    - Antenna feature sizes of 1 µm
    - Antenna dimensions of 50 – 100 µm
  - Demonstrate that the technology can be integrated into an existing CMOS IC I/O cell
  - Prove that RF signals do no effect on-chip performance
  - Demonstrate that signal integrity at test speeds is maintained
  - Demonstrate soft fault detection techniques

Summary

- Fundamentally new technology for wafer probe and other applications
- First two prototypes have proved and verified technology
- Design of fully integrated CMOS prototype is underway
- Enables full wafer probing
- Significant benefits contributing to increased throughput and increased yield

Acknowledgements

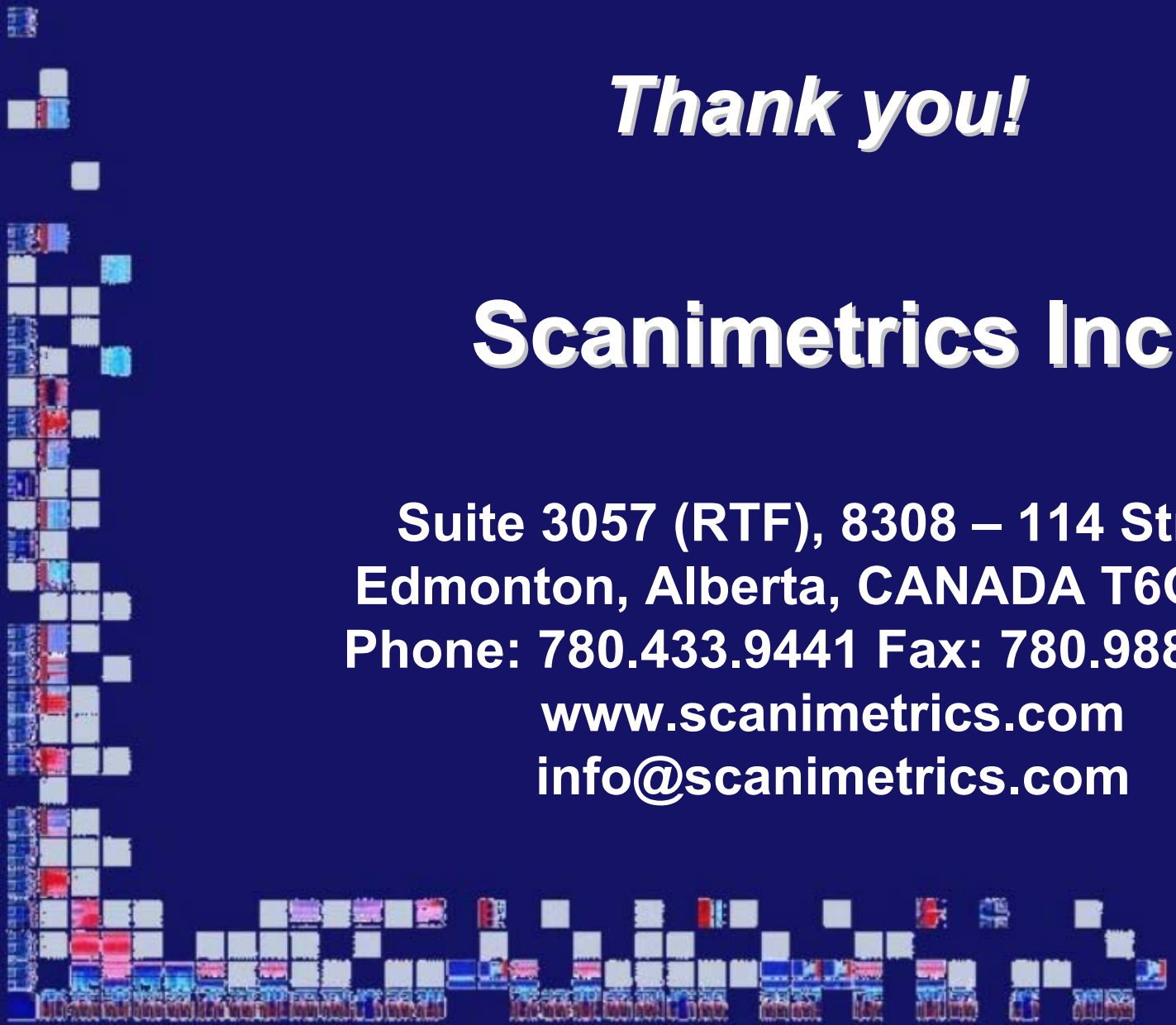
- University of Alberta

- National Research Council
  - Industrial Research Assistance Program

IRAP · PARI

- Alberta Ingenuity Fund

Alberta INGENUITY Fund



Thank you!

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