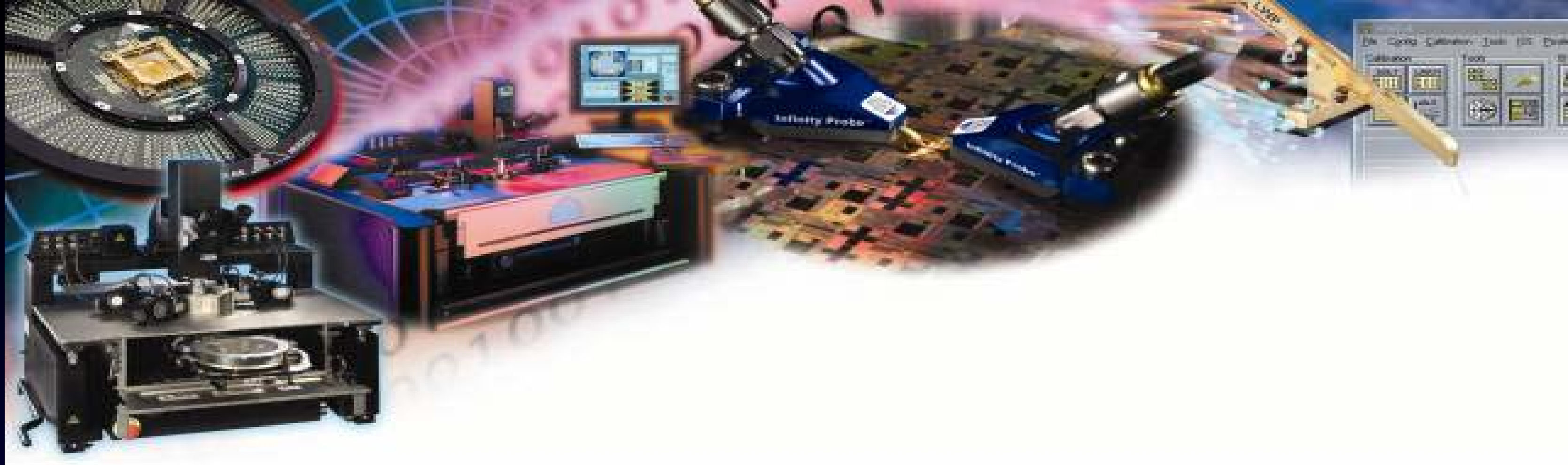
Innovating Test Technologies



"Challenges and More Challenges" SW Test Workshop June 9, 2004

Cascade Microtech
Pyramid Probe Division
Ken Smith
Dean Gahagan

Challenges and More Challenges

- Probe card requirements are getting more challenging everyday from every direction
- Identify the 5 most challenging areas
- Discuss some issues regarding each area
  - With some examples and some approaches that either give methodology to assess or that solve some of these challenges
  - And some comparisons of different technologies
- Summary

International Technology Roadmap For Semiconductors

2003 Edition

“Probe Cards

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“Challenges”

- Higher frequency response (bandwidth)
- Increasing switching currents (di/dt)
- Alternative pad/bump metallurgies
- Rising pin counts across tighter pitches and smaller pads/bumps
- Increasing test parallelism

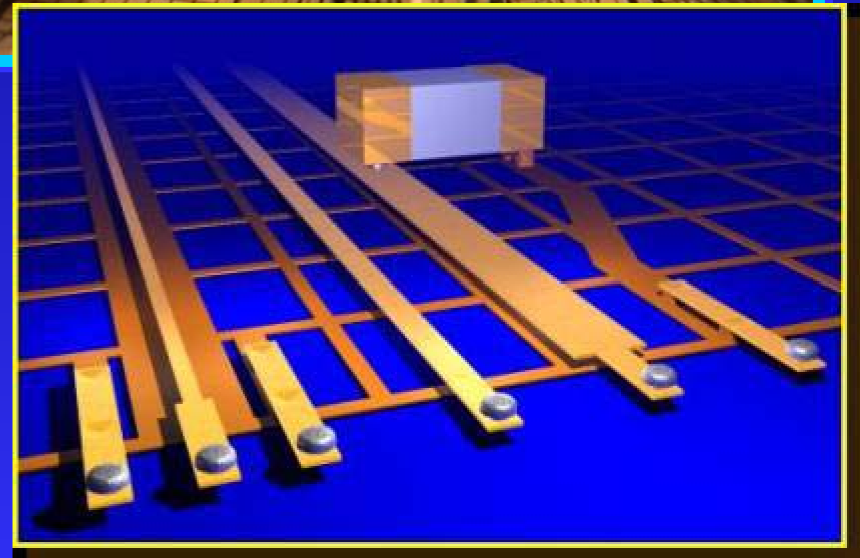
1) Higher Frequency (Bandwidth)

Probe card technologies require the following to functionally test higher frequency devices

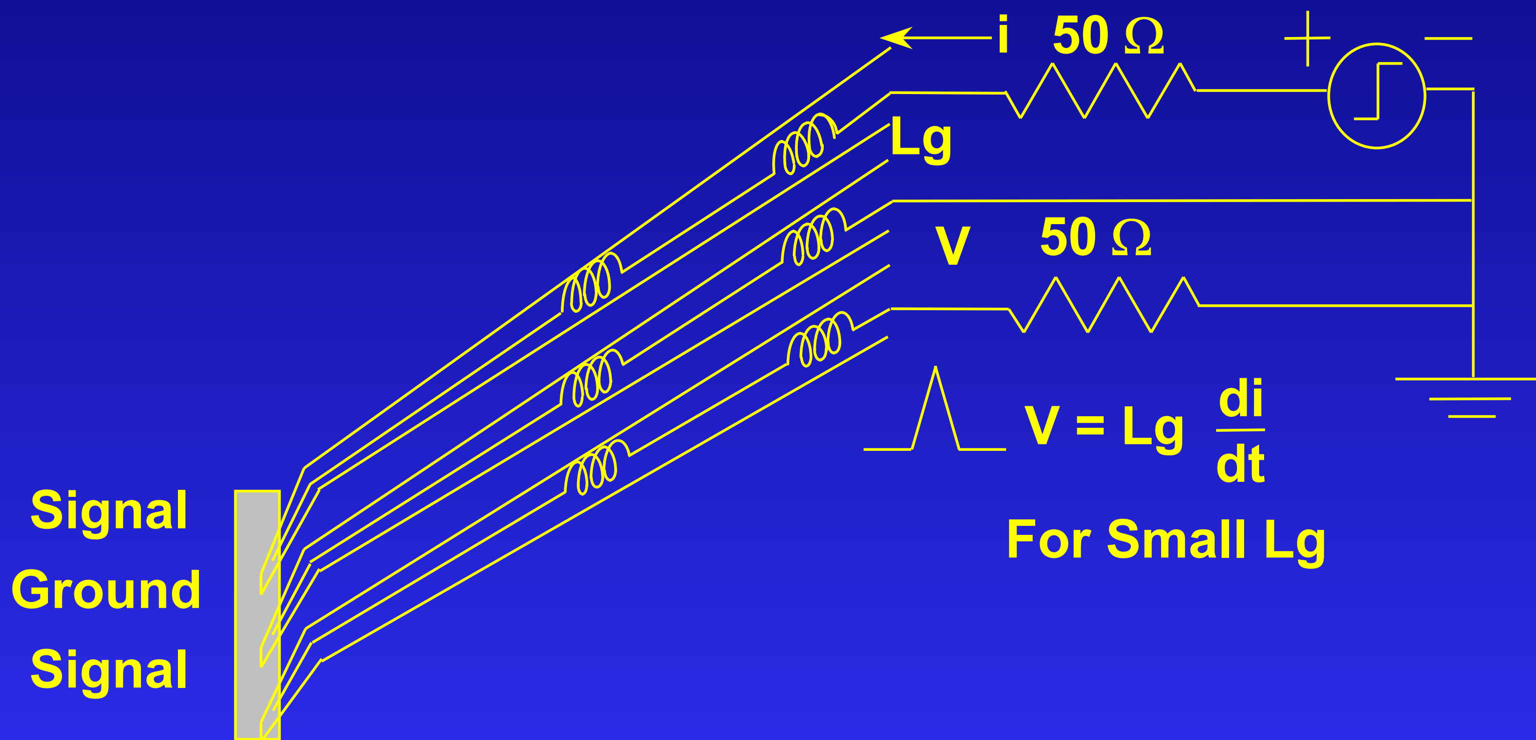
- Low inductance power and grounds
  - short probe lengths to power and ground)
- Short low loss signal lines with controlled impedance
  - short probe lengths with ground)
- Low impedance bypass capacitors
  - short probe lengths to the bypass cap)
- Low Contact Resistance
  - contact resistance affects 50 Ω lines dramatically

Probe requirements for power, ground and signal lines for higher frequency

- Probe card ground close to the DUT
- Ground inductance values < 0.5 nH
- No design constraint on ground pads
- Bypass capacitors within 50 psec of DUT
- Power lines require a low impedance path to the bypass cap and ground
- Able to power sense at the DUT to remove series resistance
- Controlled impedance lines with low return loss to enable calibration

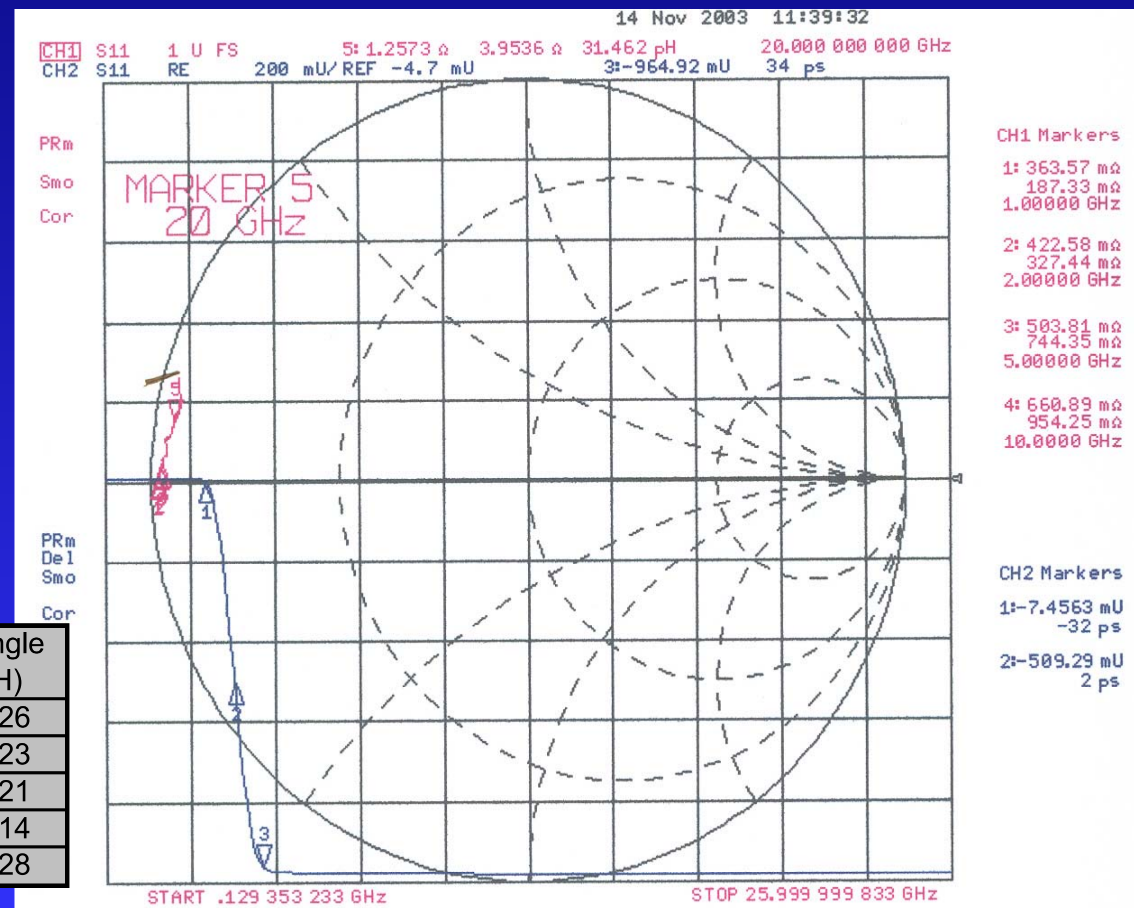


Measurement of Ground or Power Inductance



Inductance Measurement of Probe Path

- Test setup: Single probe tip with very low inductance space transformer and 8 parallel tips to ground (250 um pitch)
- L = 0.028 nH
  - (@ 20 GHz)
  - No resonance
- < 30 ps electrical length



Frequency (GHz)	X l total (ohms)	L total (nH)	L single (nH)
1	0.187	0.030	0.026
2	0.327	0.026	0.023
5	0.744	0.024	0.021
10	0.954	0.015	0.014
20	3.954	0.031	0.028

Estimating L and C Parasitics

$$Zo = \sqrt{\frac{l}{c}} \quad \textbf{and} \quad t = \sqrt{lc}$$

Where **Zo** = characteristic impedance of the line

l = inductance per unit length

c = capacitance per unit length

t = delay per unit length

L = T Zo

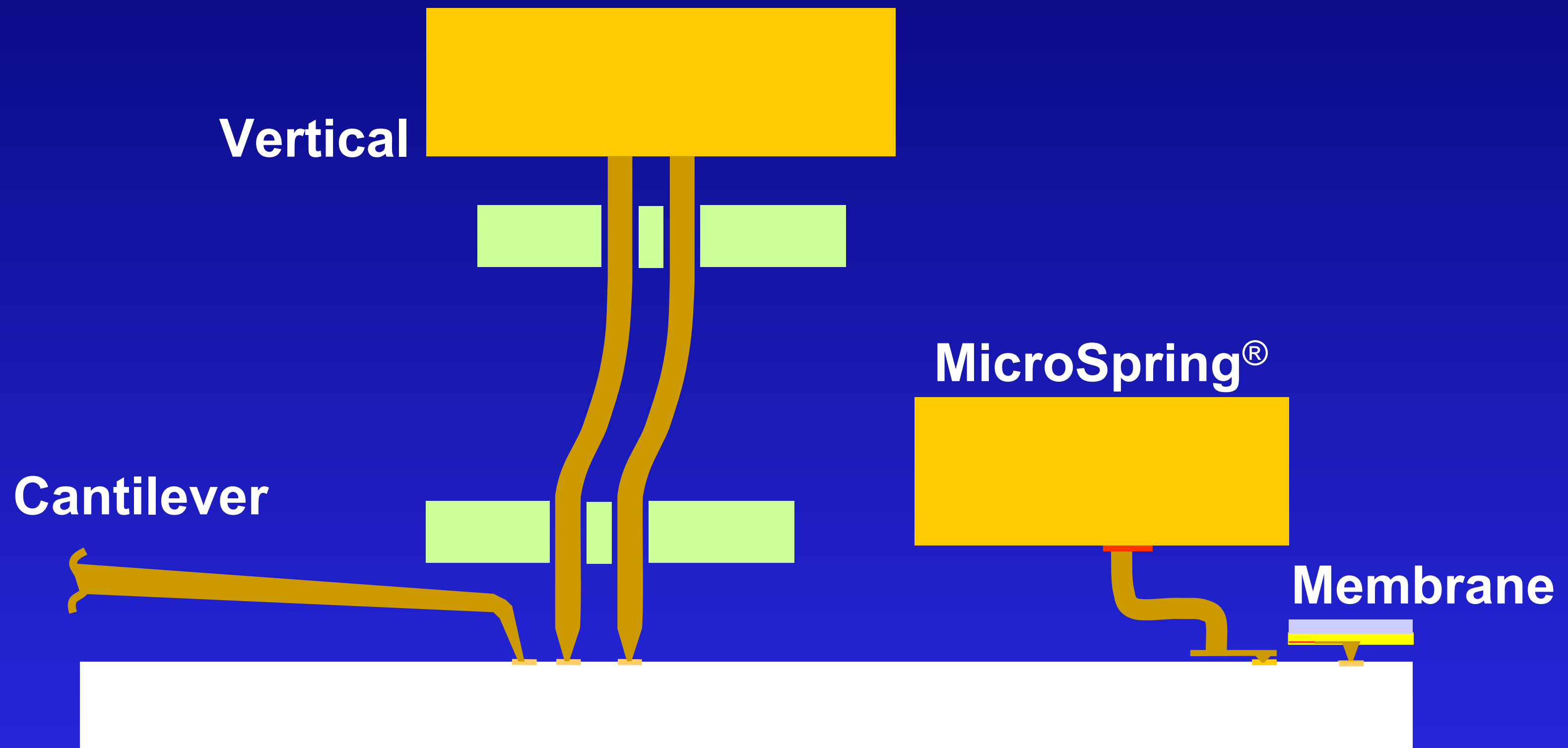
C = T/Zo

Where L = total inductance

C = total capacitance

T = total delay

Shorter Length Probe Tips Required for Lower Inductance



Contact Resistance Probing Copper Pads with Cantilever and Pyramid

3370A12_* Trend Gtest = RS_POLY1 [Ohm] between 06-DEC-03 and 21-DEC-03

SPC+CTL

TARGET

AVG

SPC--CTL--

+7.75E+00
+7.00E+00
+6.25E+00
+5.50E+00
+4.75E+00
+4.00E+00
+3.25E+00
+2.50E+00
+1.75E+00
+1.00E+00
+2.50E-01

AVG/STD

MIN/MAX

STD

production start with Cascade membrane card

[73 valid Lots from 73]

- Variance of cantilever = 1.5 ohms
- Variance Pyramid = 0.20 ohms

2)Increased switching currents

- Power supply bounce is a function of inductance and rise time
  - Delta voltage = Inductance * Delta current over Rise time
  - $dV = L * (di / dt)$
- Some typical test requirements

Typical rise times	(ns)
50 - 100 MHz (ASICs/uProc)	2
100 - 200 MHz	1
DDRAM-(BUS) (at speed)	0.2
Telecom / some SOC	0.1

Power Supply "Bounce" Calculator

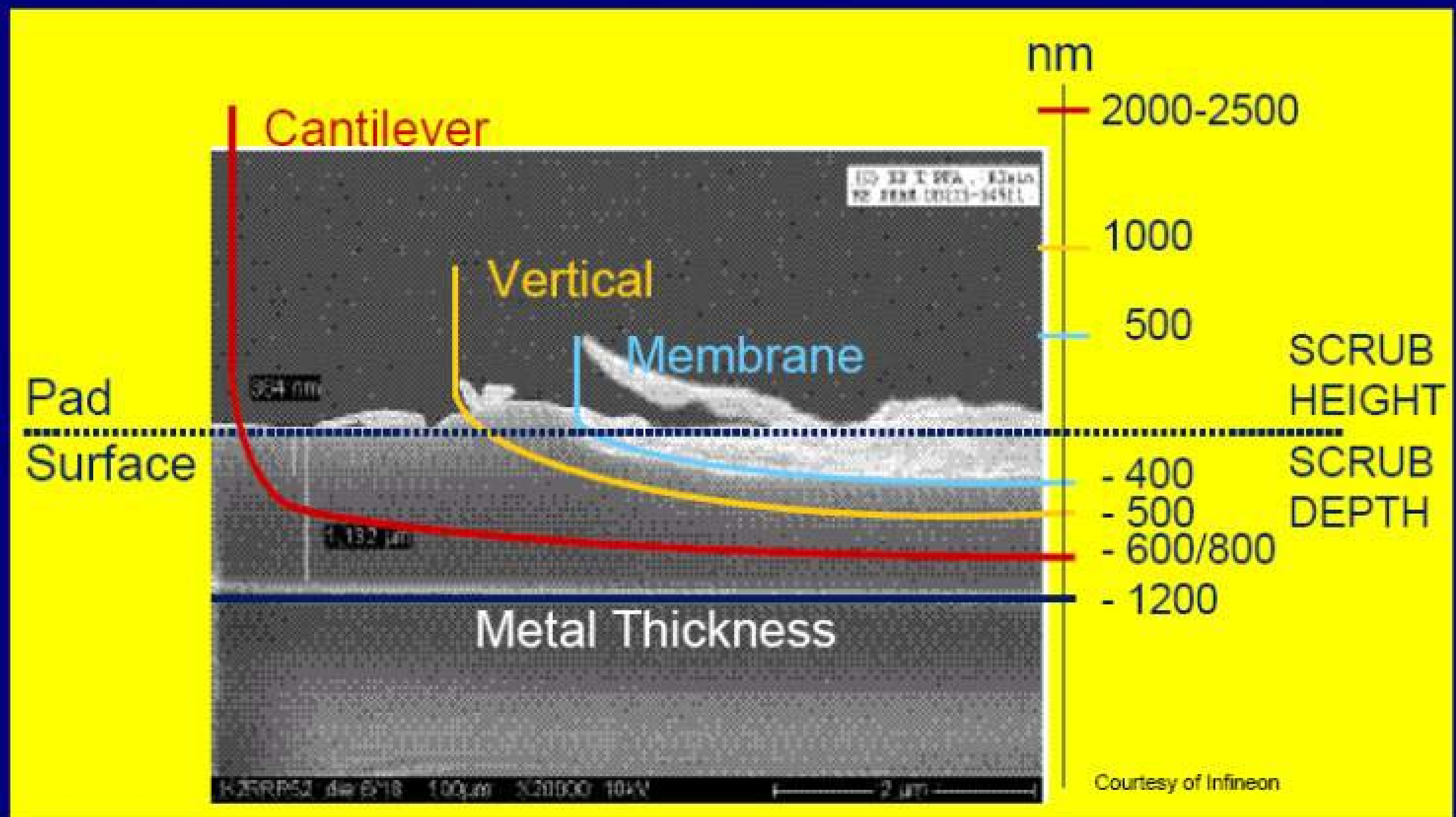
Inductance per probe>	L	Rise time	dv / dt	di / dt	Power probes /	dv
	(nH)	(ns)	(volts / ns)	(amps / ns)	I/O probes	(volts)
Cantilever	20	2	0.65	0.01	2	0.13
	20	1	1.30	0.03	2	0.26
	20	1	1.30	0.03	1	0.52
	20	0.5	2.60	0.05	7	0.15
Vertical (w ST)	10	1	1.30	0.03	2	0.13
	10	0.5	2.60	0.05	3	0.17
	10	0.5	2.60	0.05	1	0.52
Microspring (w ST)	7	1	1.30	0.03	2	0.09
	7	0.2	6.50	0.13	2	0.46
	3	0.2	6.50	0.13	2	0.20
Membrane	0.2	1	1.30	0.03	1	0.01
	0.2	0.1	13.00	0.26	1	0.05
	0.2	0.03	43.33	0.87	1	0.17
Note: Hard to find published inductance for space transformers (very design dependent)						
Input fields						
Driver impedance (ohms)	50		dv = L * (di / dt)			
Logic level (volts)	1.3		dv< 10% Logic level		< 20%	>20%

3) Alternate Pad/Bump Metallurgies

Challenges for good electrical contact with minimal pad/bump damage

- **Aluminum pads (of course)**
  - Oxide, thinner metal (0.5 micron), bondability vs pad damage
- **Gold pads and bumps**
  - Organic contamination, damage vs ACF bonding
- **Copper pads and bumps**
  - Requires a non-oxidizing probe tip
- **Al clad copper**
  - Damage to the barrier metal
- **Solder balls**; C4, Eutectic , lead free (Sn+____),
  - Probe tip damage, bump damage, voids, cleaning

Pad Damage of Probe Technologies



*slide complements of Fred Tabor of IBM and Infineon

Probing Low-K Dielectric

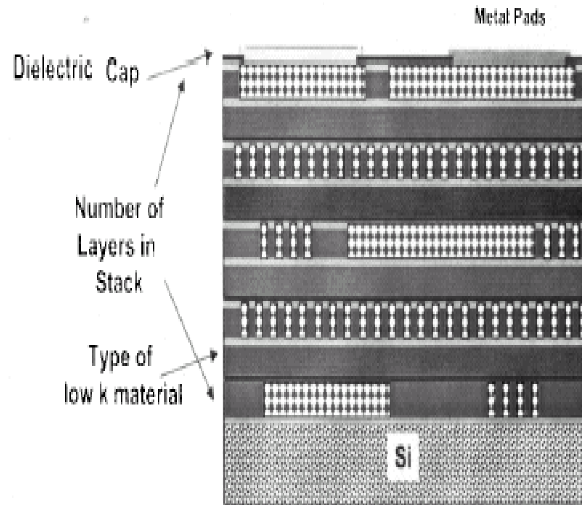
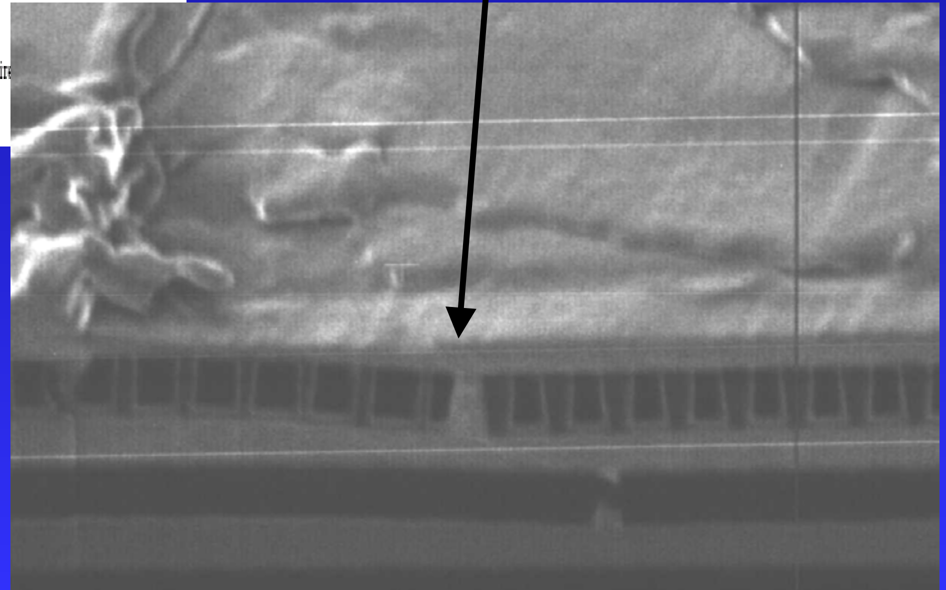


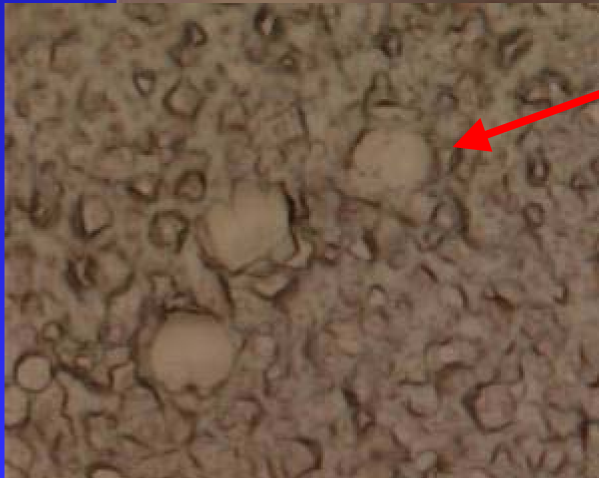
Fig. 2. Copper–damascene/LoK metal/dielectric stack, which indicates the complex structures that must be accommodated for wir
separated by thin barriers. Figure permission of ISMT.

New stack-ups pose serious challenges

Cracking can occur and is a function of the amount of force, pressure, and scrub



Probing Copper Posts

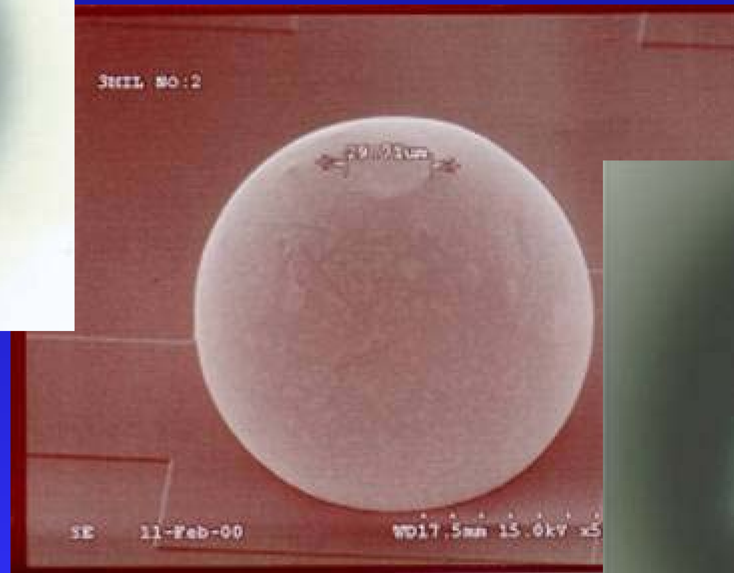


- Marks are barely visible due to surface roughness and hardness
- Marks are variable due to grain structure of the copper plating process

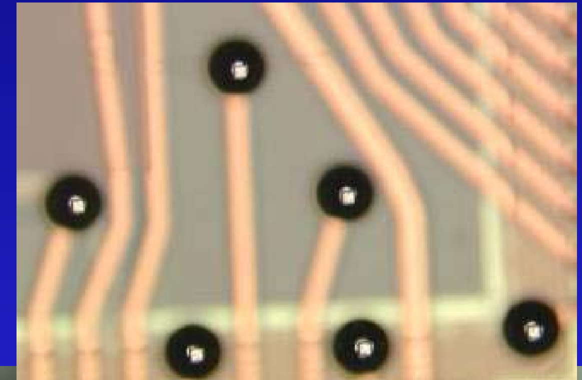
Probe Marks on Solder Balls

Probe Mark on solder ball probed by Epoxy probe card

Probe mark by vertical probe card



Probe Mark by Pyramid probe card



Probe Tip Force Measurements

- Desired capability
- Problem statement
- Micro-hardness tester theory
- Substitution of standard tools with probe tip
- Data
- Photos
- Results

Desired Capability

- Be able to quickly characterize new pad stacks and know whether a given probe tip and force/scrub combination will cause excess damage
- Use this tool to engineer better probe solutions for damage in sensitive applications
  - Low K dielectrics
  - Pad-over-trace
  - Pad-over-active

Problem Statement

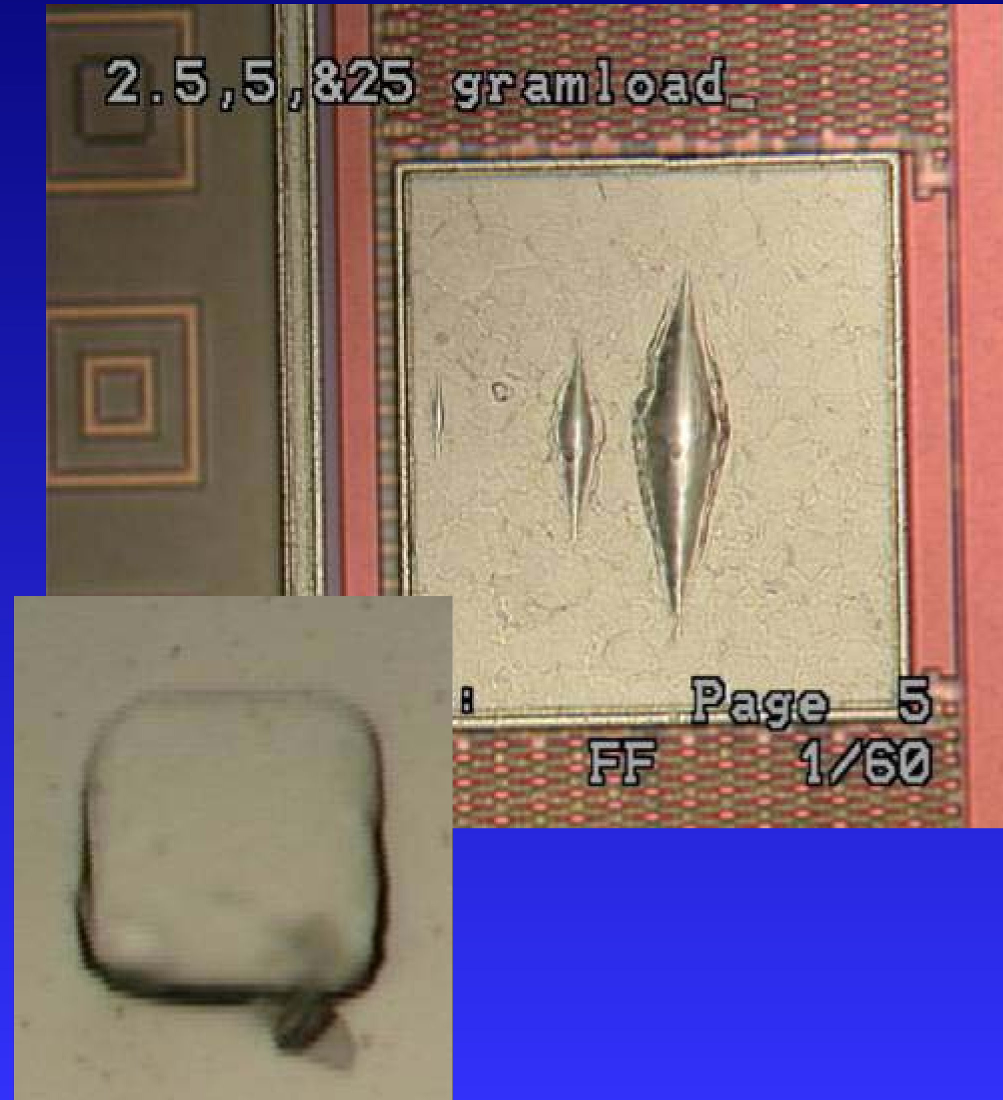
- Interactions among probes, probe stations and wafers make it difficult to relate pad damage to actual probe force applied
  - No available in-situ single probe force measurement method
  - Soft underlying dielectrics yield and convolute spring constant model assumptions
  - Average probe force can be measured but variance is difficult
  - Single probes may not scrub the same as multiple probes

Theory

- Use a micro-hardness tester to measure customer's wafers
- Compare micro-hardness with probe tip force/scrub/pressure and pad damage analysis
- Develop a model and standard process

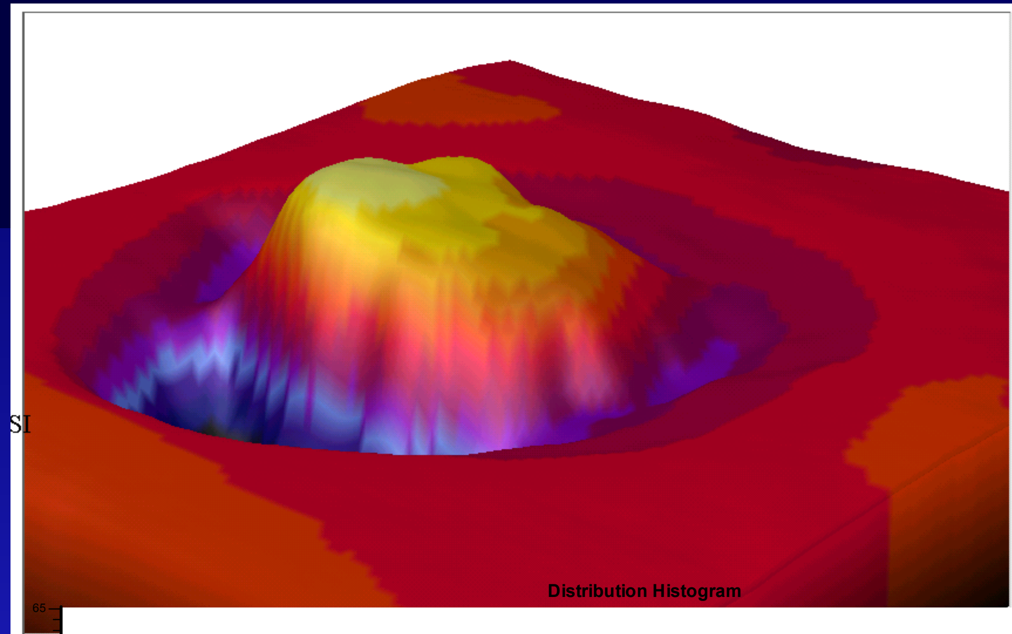
Micro-hardness Tool Capability

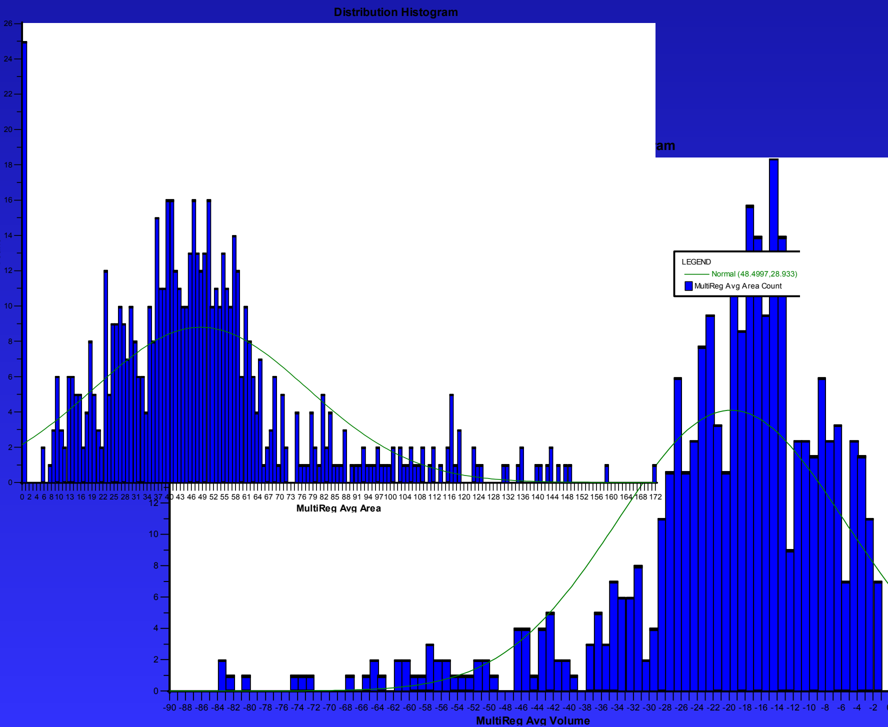
- Micro-hardness testers are almost adequate
  - \+ Easy to align tool and mark pads with known force
  - \+ Rigid mount eliminates vibration and provides scrub
  - \- Excess interaction between measurement and thickness (1 um) of pad stack
  - \- Tool is wrong shape to deal with multilayer stack
- Replace microhardness tool with a probe tip

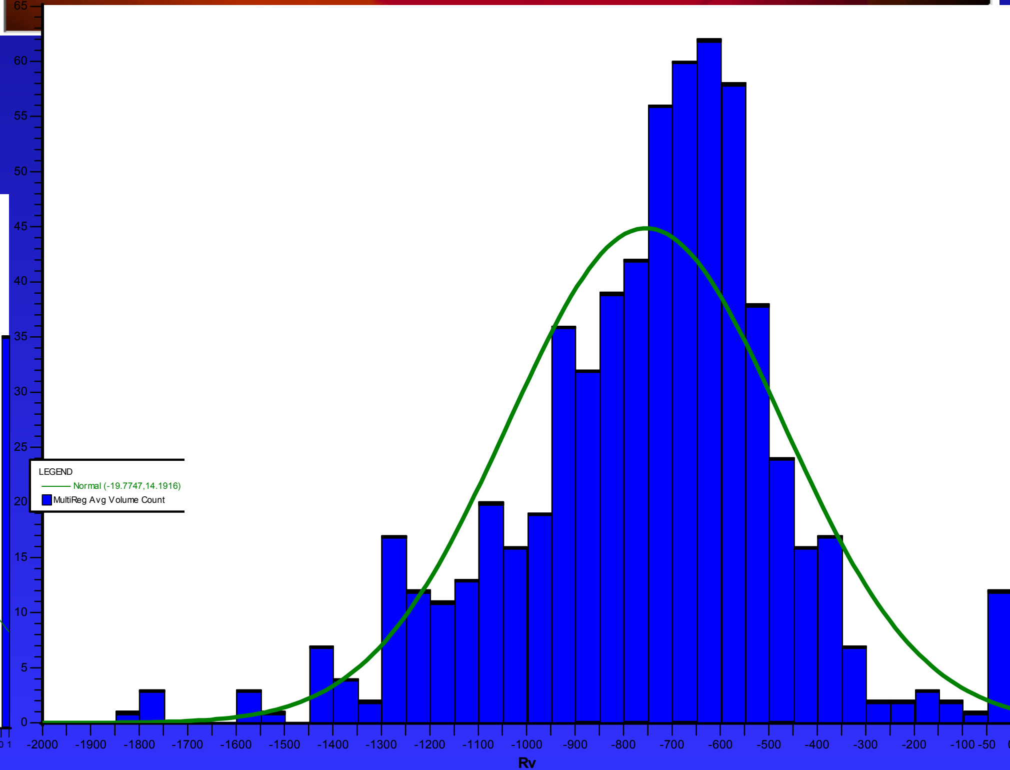


Mark Analysis

- Area, depth and volume interact
- Large data set required







Solution Set

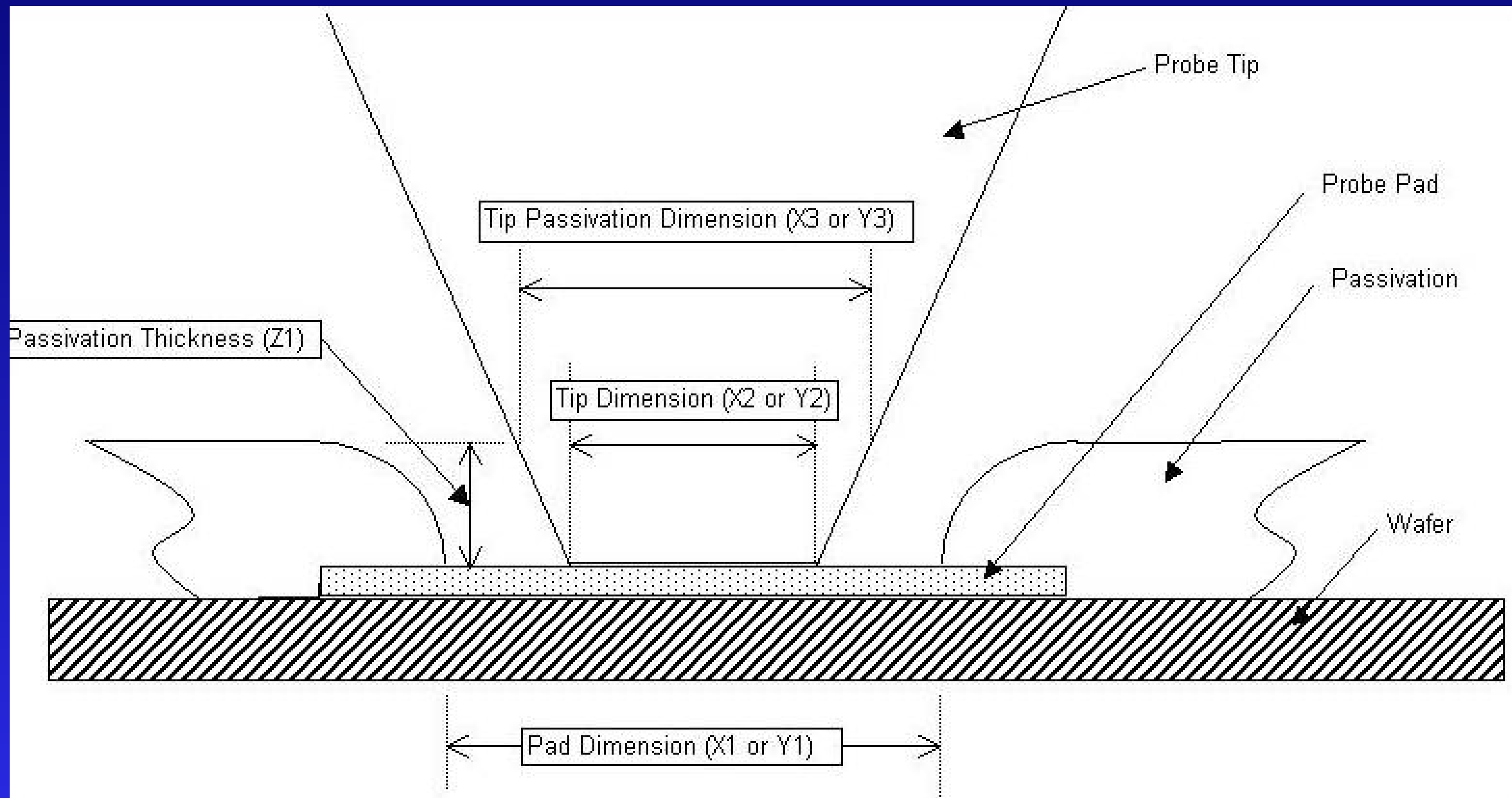
- Improved planarity: Reduced electrical first to last 50%
- Improved balanced contact force
- Reduced contact area variation by 60%
- Qualified for high volume production at multiple sites for low K dielectrics and Pad-over-active designs

4) Rising Pin Counts

….. and tighter pitches and smaller pads/bumps

- Pitches down to 44 microns today and pads sizes down to 35 microns square require
  - Probe tip diameters need to be smaller
  - Better XY positional accuracy of probe tips
  - Better XY positional accuracy of the prober
  - Better characterization across temperature
  - Better metrology tools to correlate customer requirements with delivered product

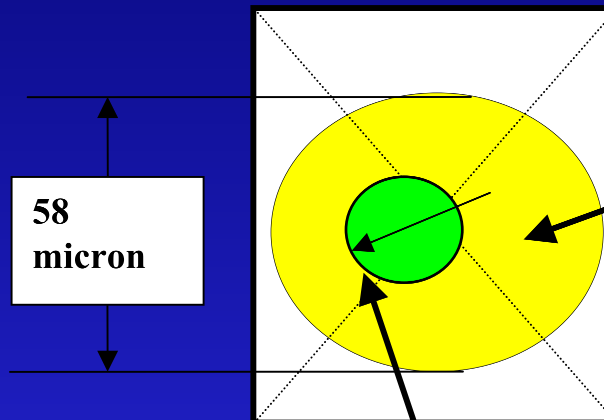
Profile of a Probe Tip on a Pad With Passivation

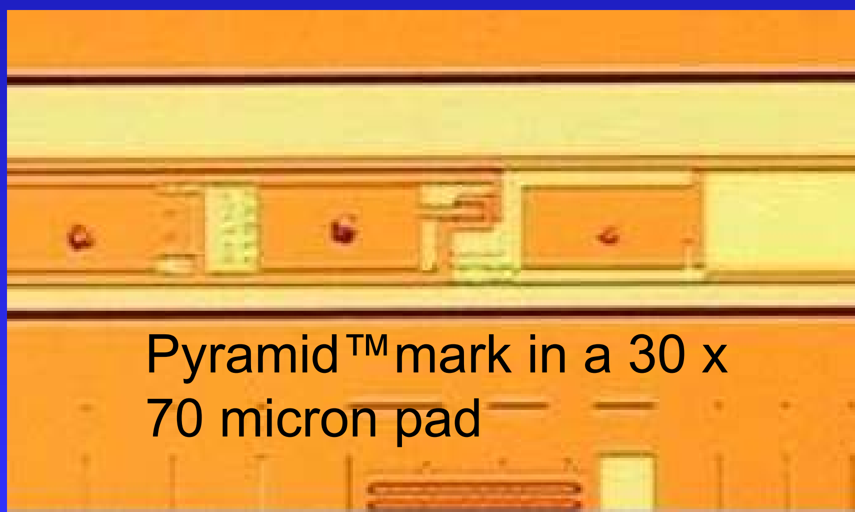


- Passivation determines which probe tip dimension plays a major role for ever shrinking pads

XY Positional Accuracy

Variables that need to be taken into consideration on individual probe tips in order for the calculation of XY positional accuracy of the total probe card



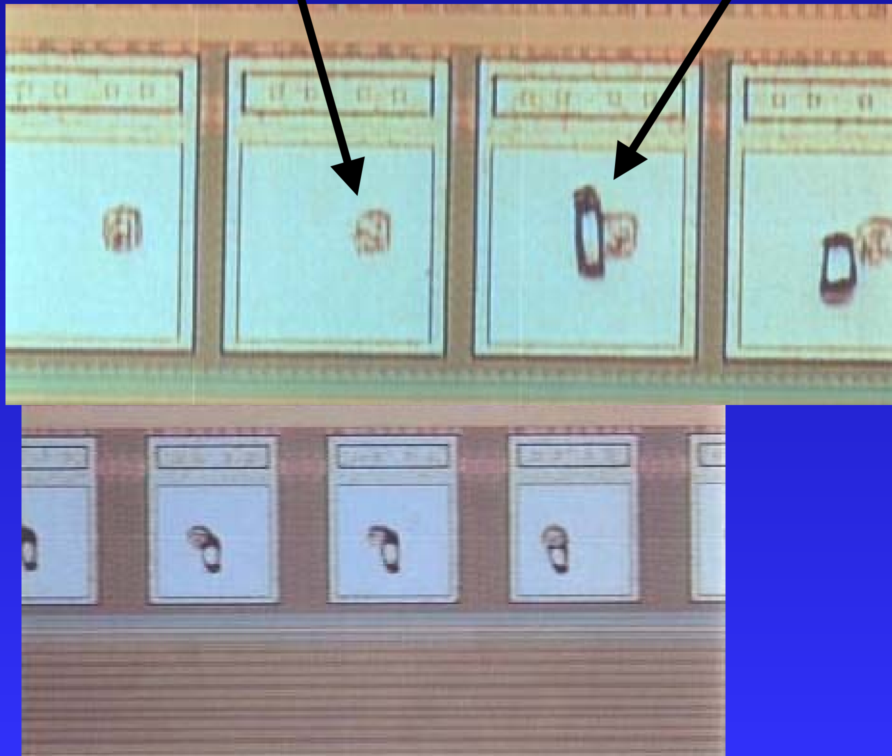


Various Probe Marks on Al Pads

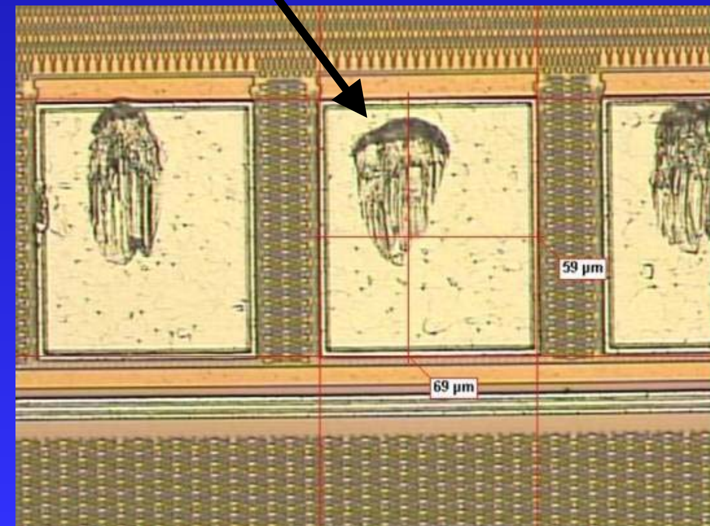
Pyramid™ mark as a point of reference, size is 15 microns wide and 18 microns long

Microspring™, Cantilever and Pyramid Probe™ marks

Note probe mark size, position in the pad, and scrub mark length

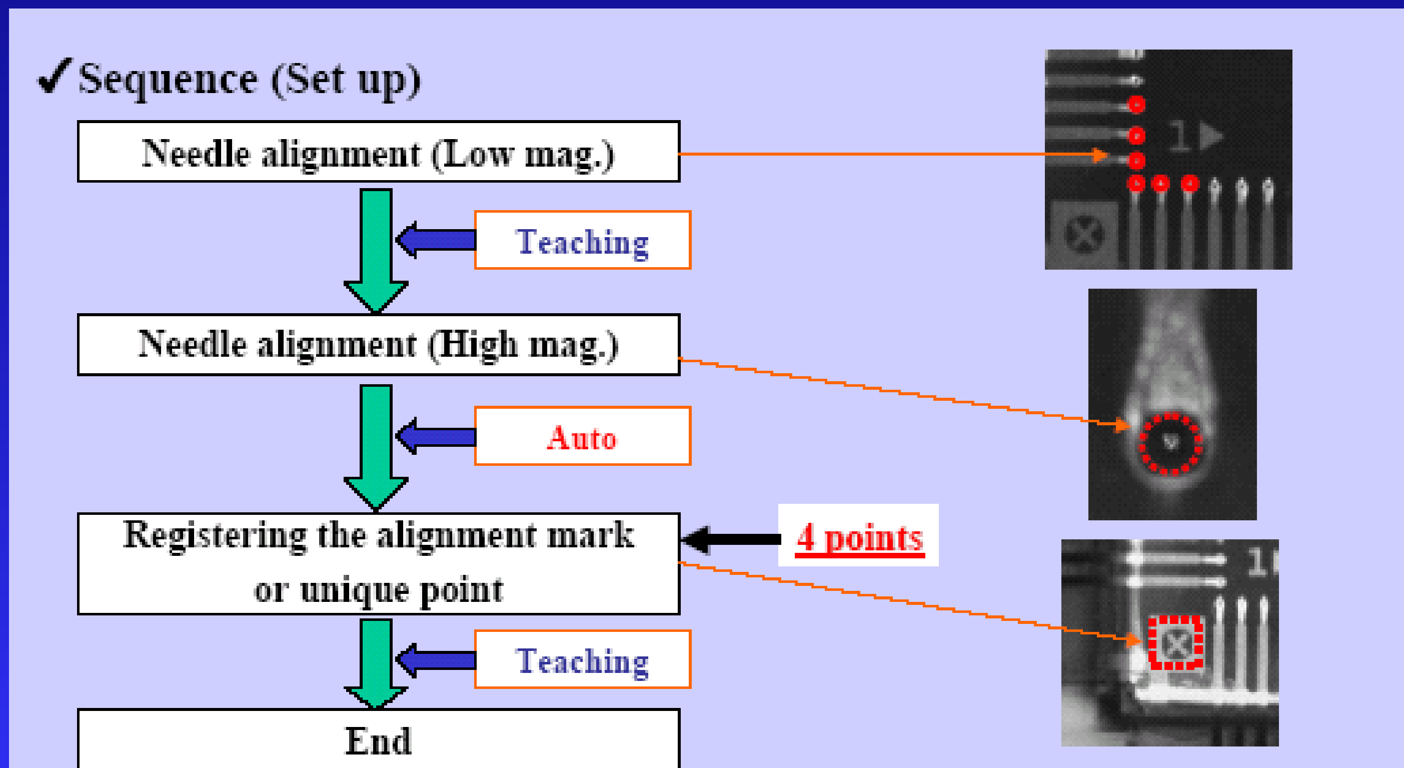


Cantilever on 60 micron pad



Tighter XY Positional Accuracies Require Fiducials to Achieve PTPA Requirement

- Note: Alignment of the Probe tips and the alignment mark



Courtesy of Accretech

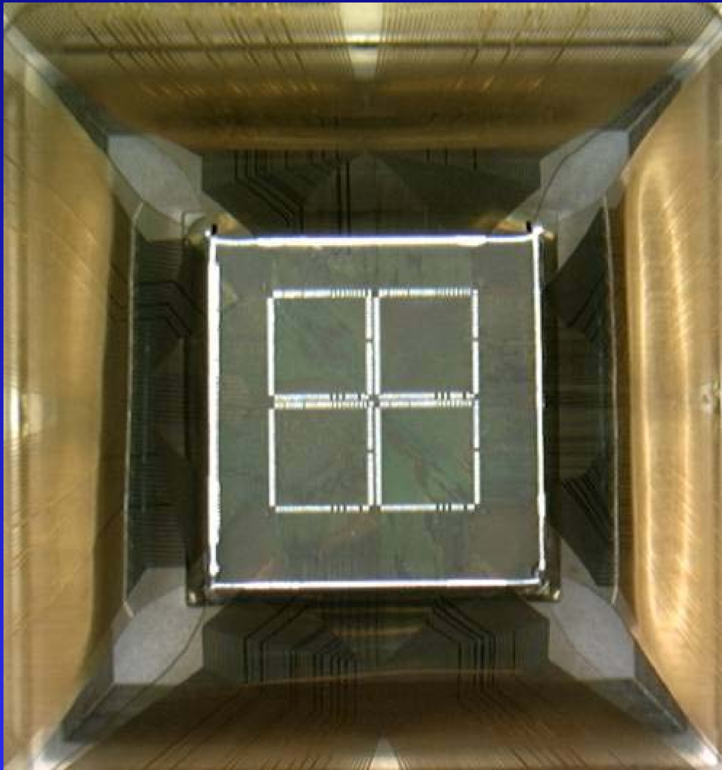
5) Increasing Test Parallelism

All of the previous challenges discussed are multiplied when you have to do this in a Multi DUT configuration

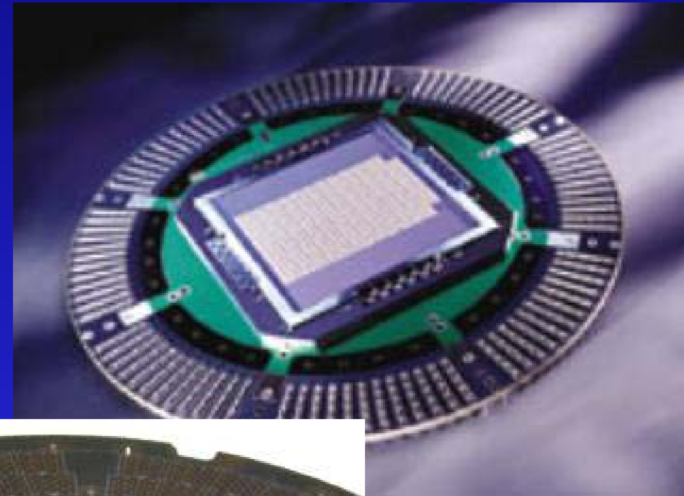
- Lower Inductance
- More current switching
- Less damage
- Better positional accuracy on smaller pads over a larger area with more probe tips
- Better control on balanced contact force over a larger area
- Better cost of ownership

Various Multi DUT Probe Cards

A 2 x 2 Mixed signal Pyramid™ probe card



A 204-DUT DRAM probe card (by FormFactor™)



A 2 x 4 Skip vertical probe card (by Probest)

Summary

- Probe card solutions are available to meet the future challenges
- Requires an ongoing partnership with Semiconductor Manufacturers and Probe Card Vendors
- New metrology tools have to be developed continuously and improved upon to better characterize probe cards and mechanical properties of the area to be probed