“Leading Edge” Of Wafer Level Testing

William Mann

Chair, Southwest Test Workshop

2004 ITC Program Committee

Advisory Board, Design and Test of Computers

Outline

SOUTHWEST TEST WORKSHOP

I. Introduction
II. Contactor Technology
III. Finest Pitch
IV. Highest Pin Counts & Full Wafer Probing
V. Biggest Probe Card & Biggest Prober
VI. Highest Frequency
VII. I/O Pad and Solder Ball Deformation
VIII. Probe Needle Cleaning
IX. Sorting Bad From Good Die

Let's Define "Leading Edge"

- **The smallest, biggest, fastest, most, & best**
- **Utilization must be in reasonable production**
  - **Limited production**
  - **Good size production evaluation**
  - **Prototypes and beta sites don't count**
- **I won't give the semiconductor companies' names unless their accomplishments are in the public domain**
- **The probe card and equipment vendors *were anxious to brag!***

Probe Test Cell

ATE

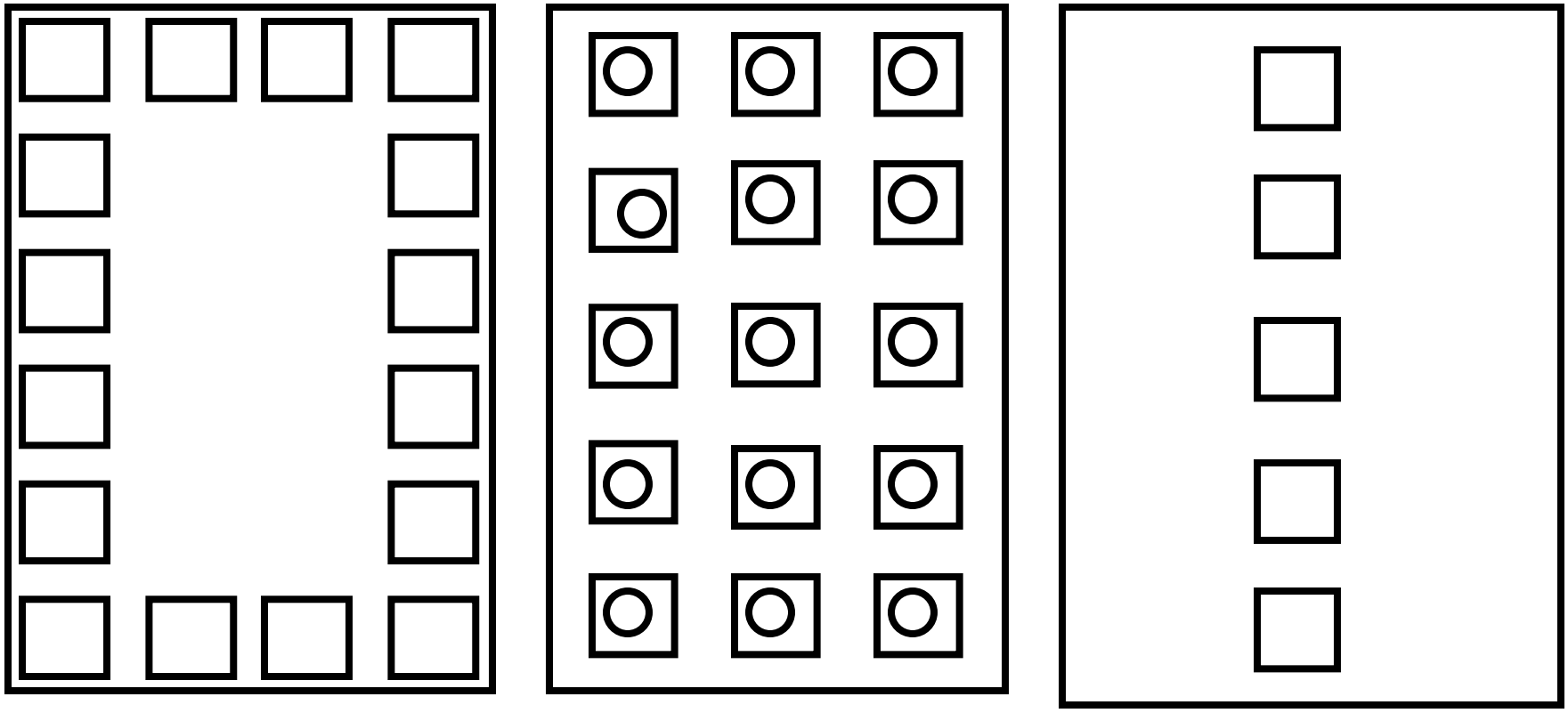
Prober Interface Board

Spring Contactor Assembly

Probe Card

Prober

I/O Pad Configurations

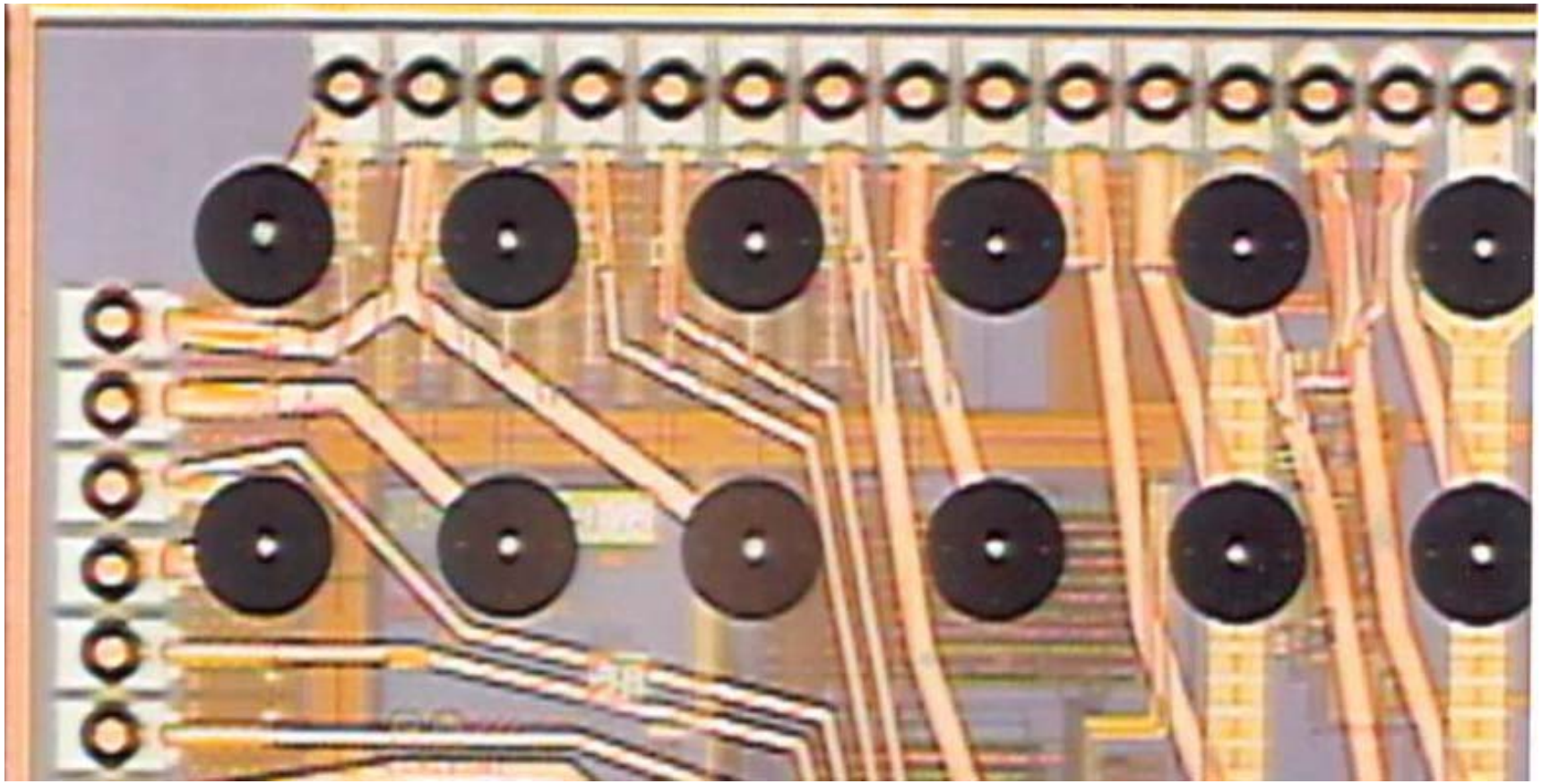


Conventional Perimeter

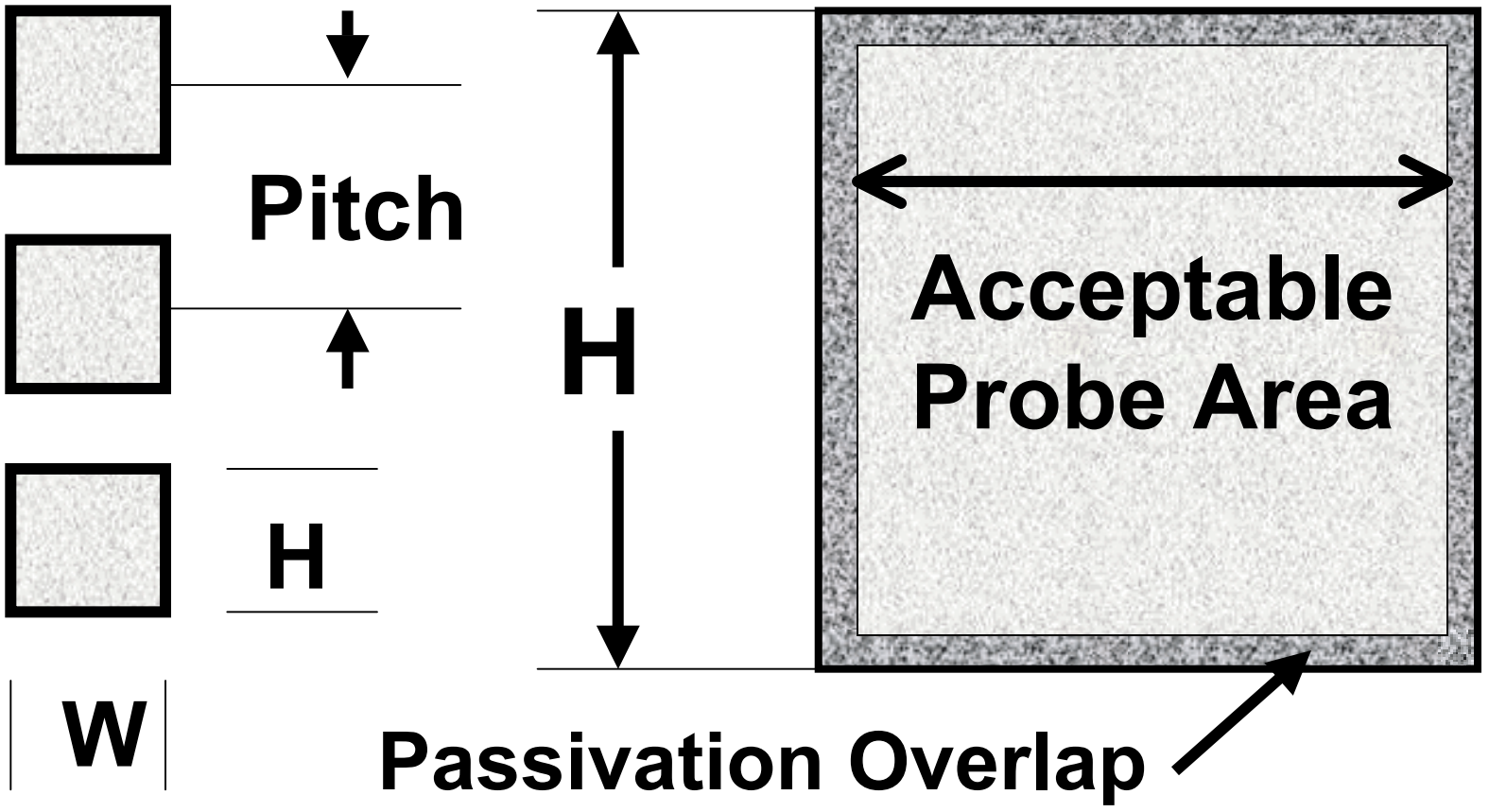
Area Array

Memory Line-On-Center

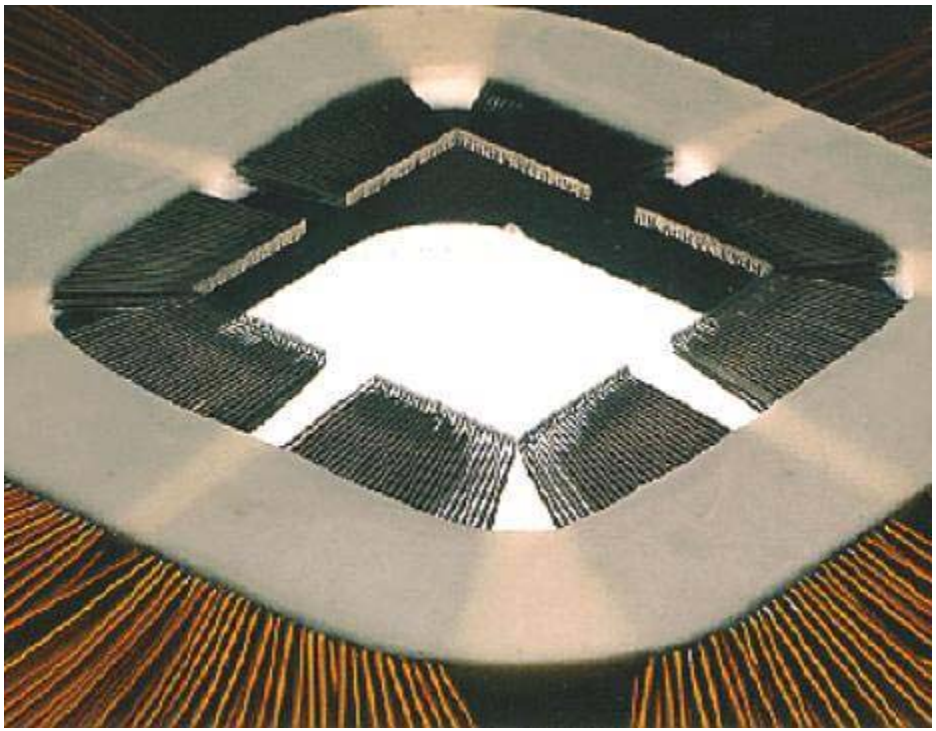
Perimeter I/O Pads Redistributed Into Area Array Solder Bumps



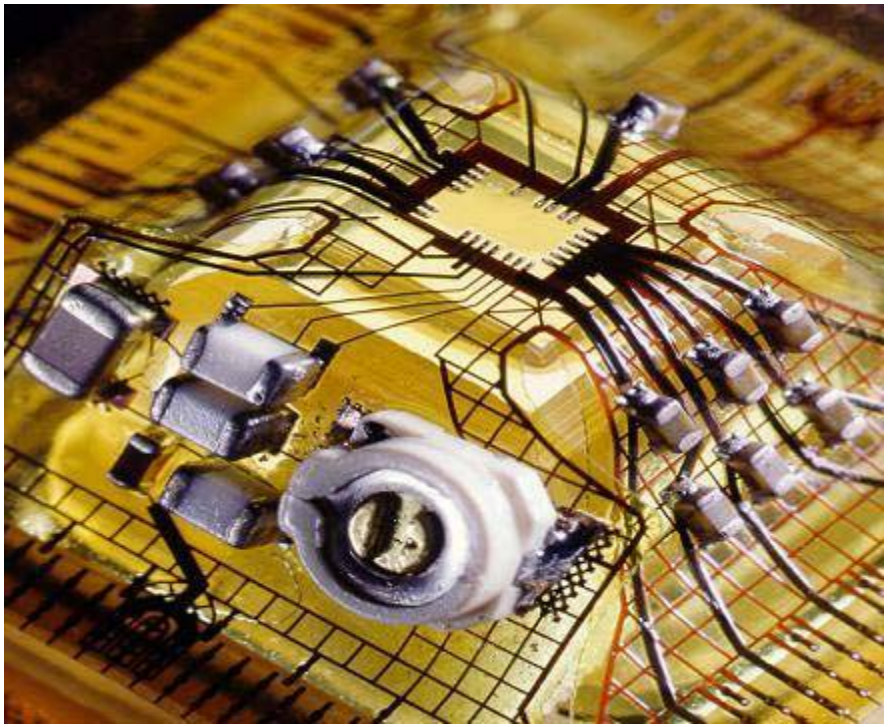
I/O Pad Critical Dimensions



Typical Probe Cards

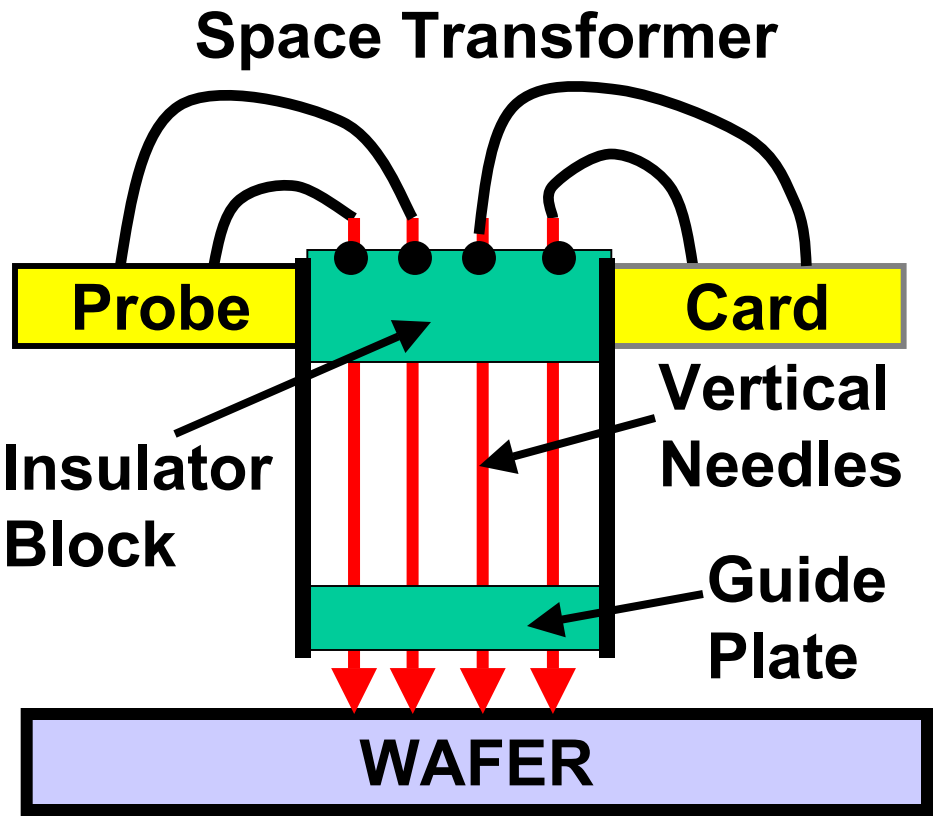


Epoxy Ring,
Cantilever Needle



Cascade Microtech
Membrane

Vertical Probe Cards Used for Area Array I/O Pads



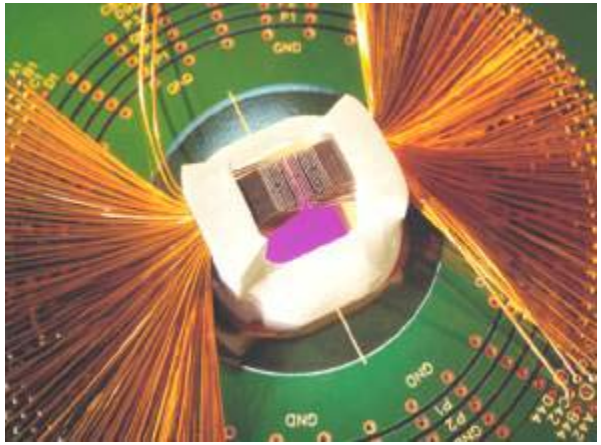
Cobra "Buckling Beam" Card
Patented by IBM in June 1977

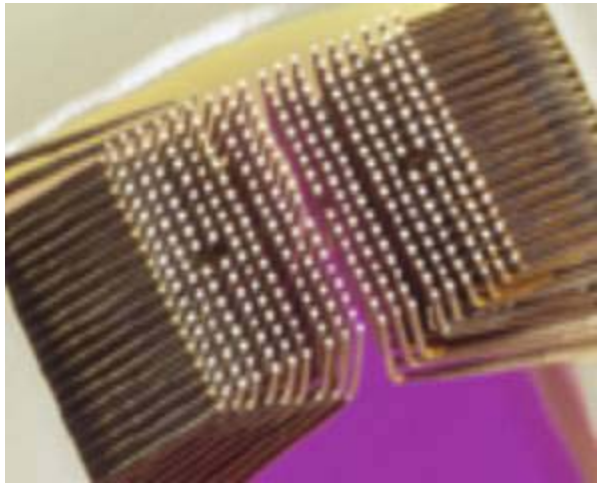
Generally have the x – y location and the force coming from directly above the I/O pad, rather than from a cantilever structure

Needles and clearance holes in guide plate limit minimum pitch

Complicated mechanical assembly

SV Probe Cantilever Vertical Card





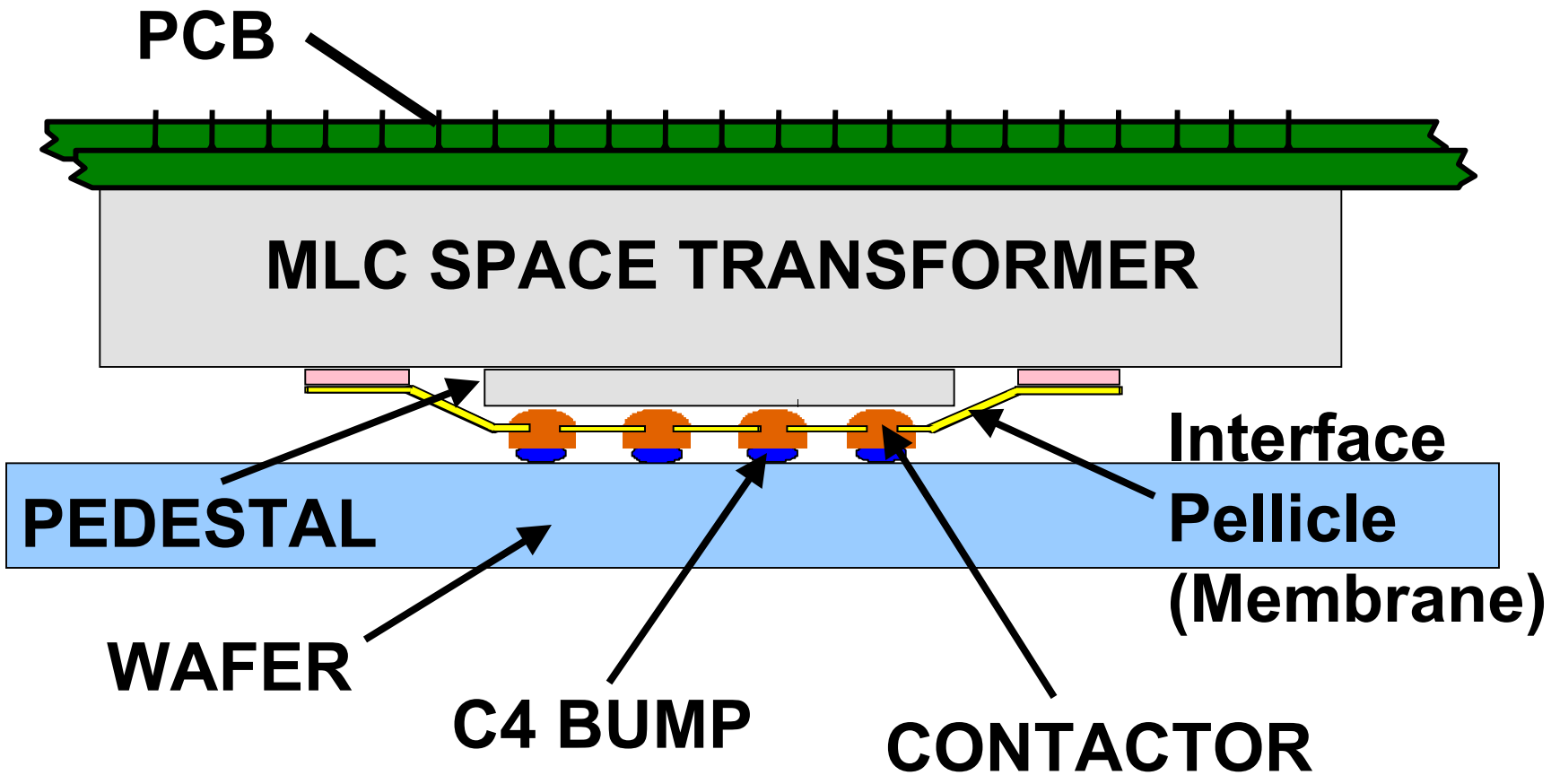
Extends cantilever technology

Hybrid epoxy cantilever needle structure

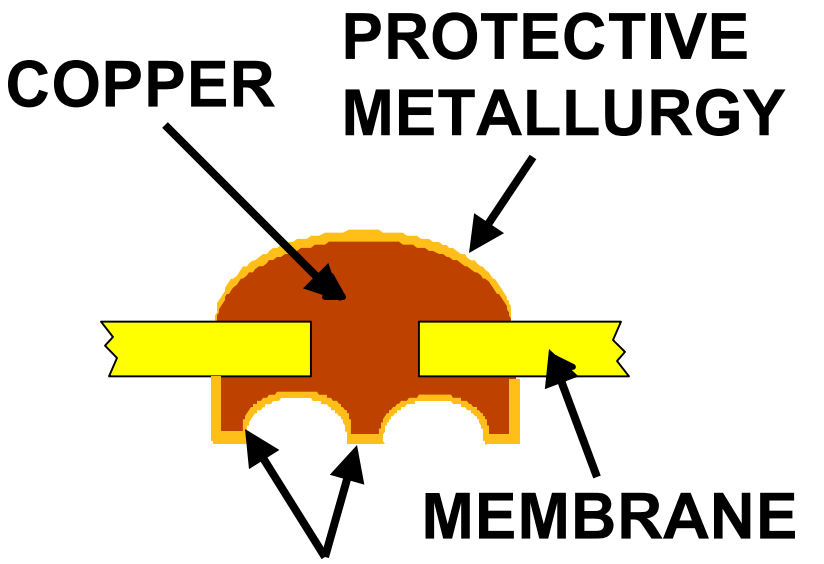
Lower guide plate and insulator block replaced by epoxy structure

Fastest delivery time: 2 - 3 weeks for 1200 needles

IBM Thin Flexible Interposer (TFI) for C4 Solder Bumps



IBM TFI Contactor



PROPRIATARY AUTO-SCULPTING CONTACTOR FOR MINIMAL SOLDER BALL DEFORMATION

IBM has the Leading Edge Performance (dv/dt) in vertical probe cards

Needle is replaced by low inductance contactor

MLC Space Transformer is the device package

Careful fabrication due to little vertical compliance

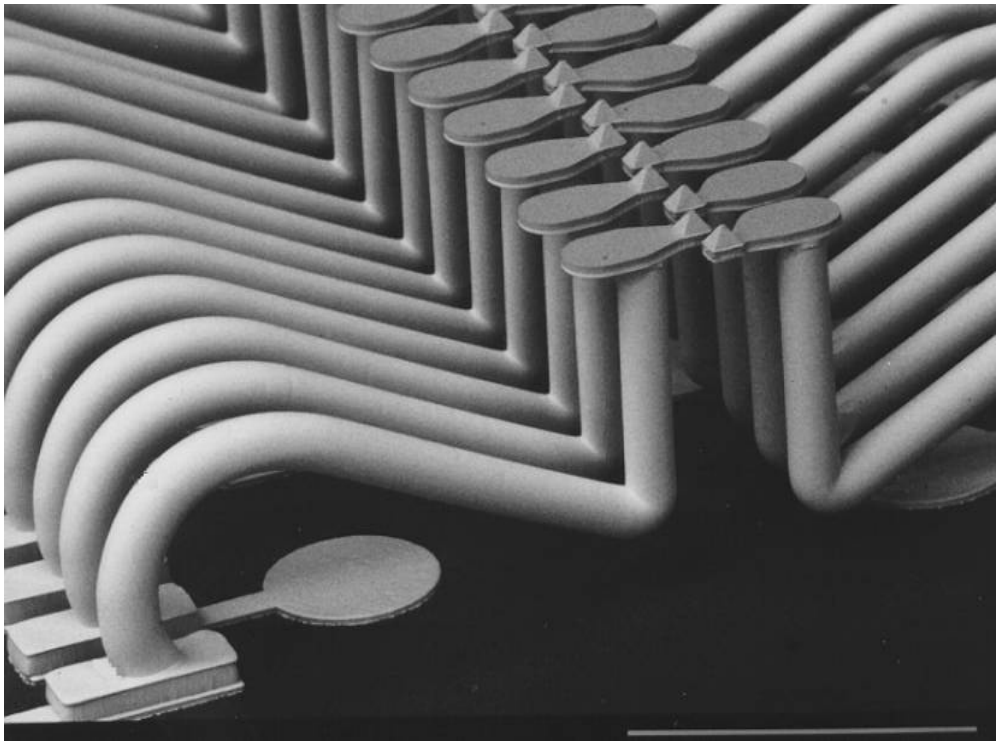
II. Contactor Technology

- Cantilever and buckling beam needles are for the most part, “manually” assembled
- Assembly processes limits the pitch
- Probe Card cost is linearly dependent on the number of contactors
- New photo lithographically defined and positioned contactors are Leading Edge:

  Microsprings

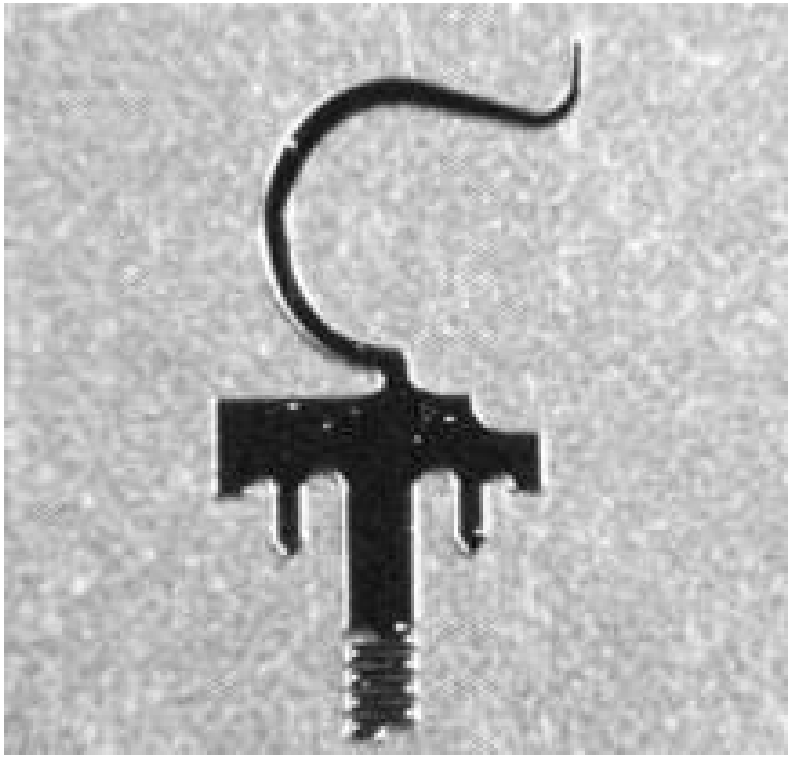
  Micro-Electronic Mechanical Systems

MicroSpring Contactors

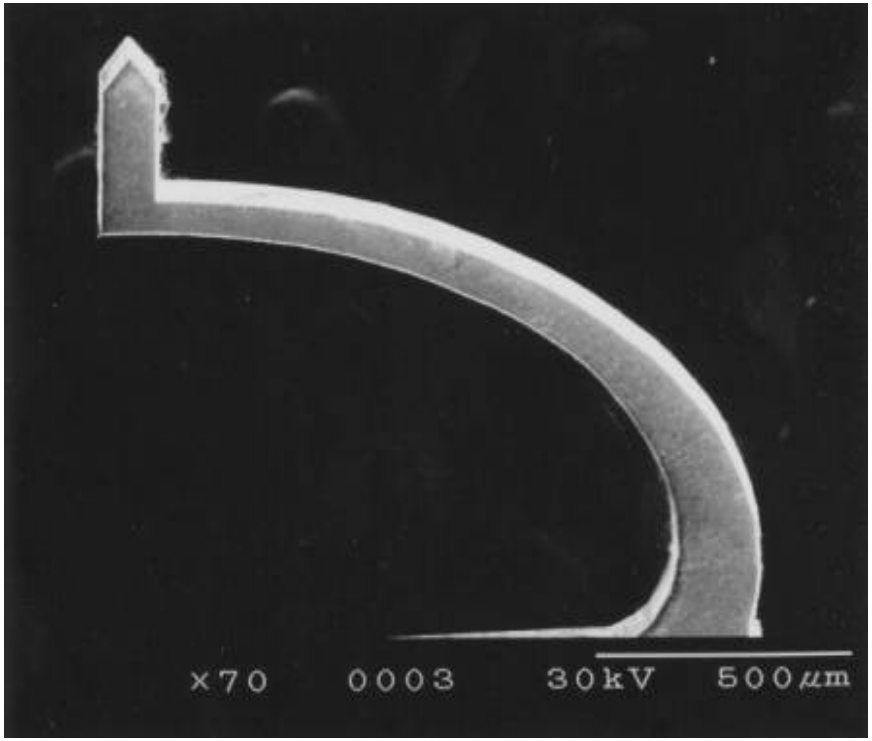


FormFactor MicroSprings **JEM HAWK**

MicroSpring Contactors

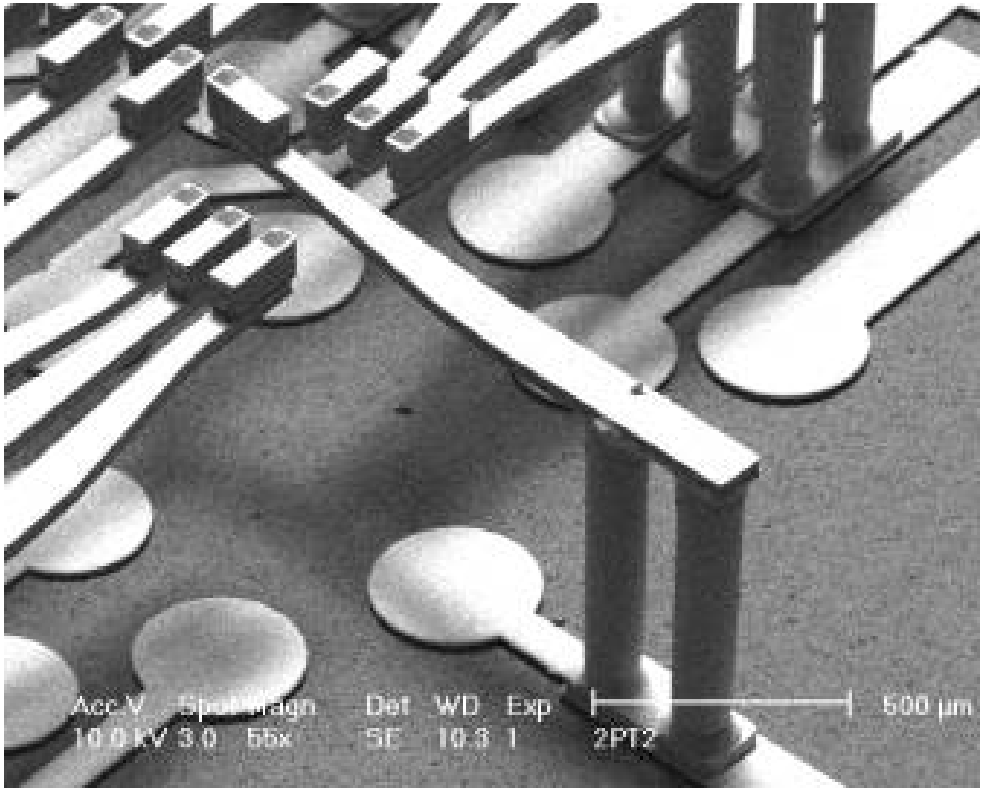


Advantest Labs

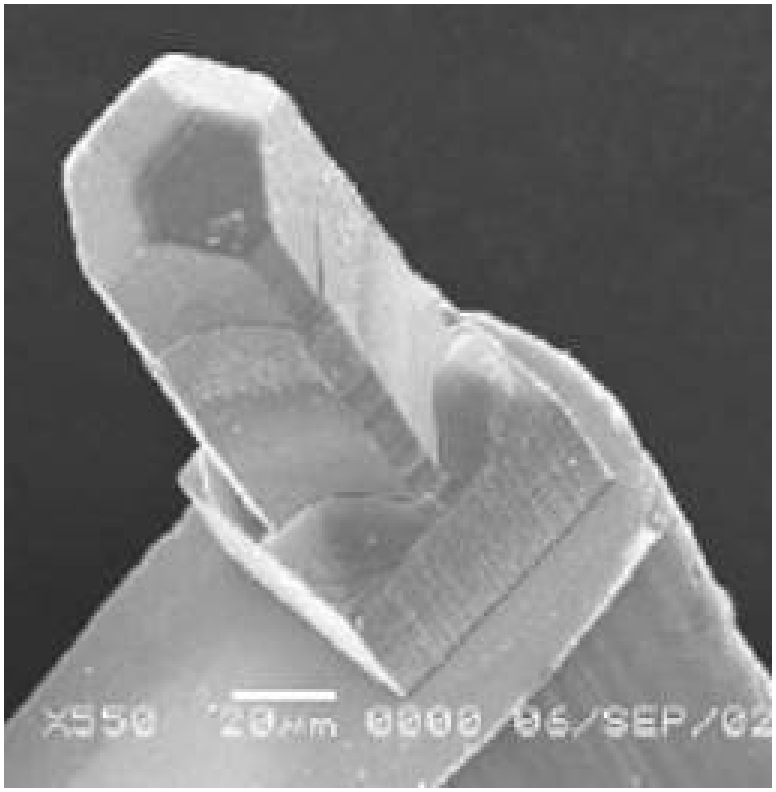


Sumitomo

MEMS Contactors

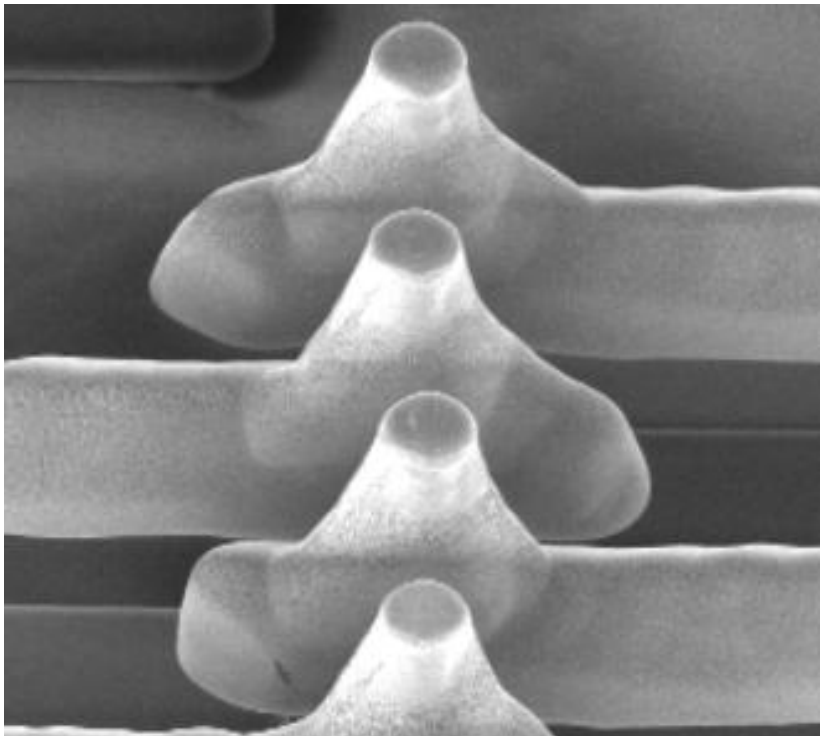


FormFactor

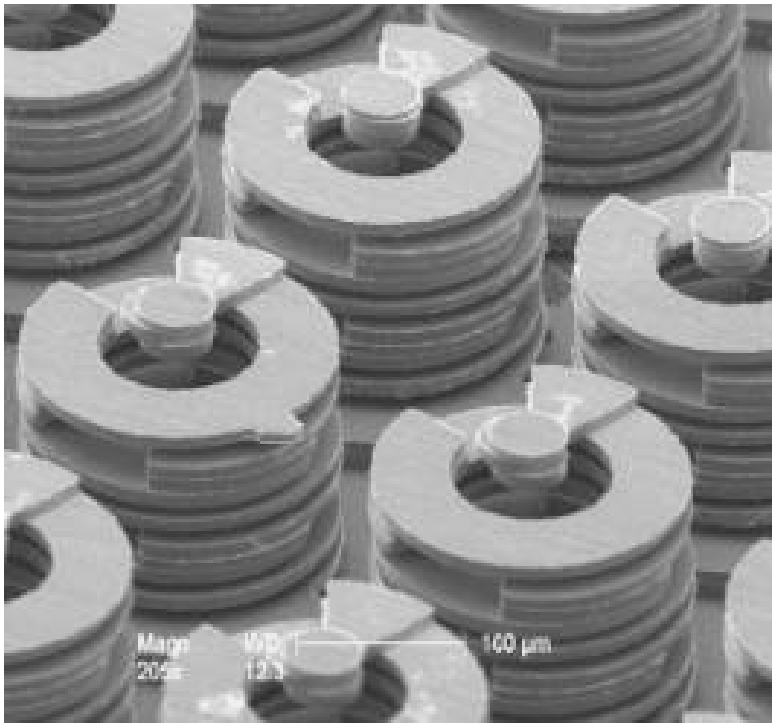


Phicom

MEMS Contactors



AMST



Microfabrica

III. Minimum Pitch In Microns

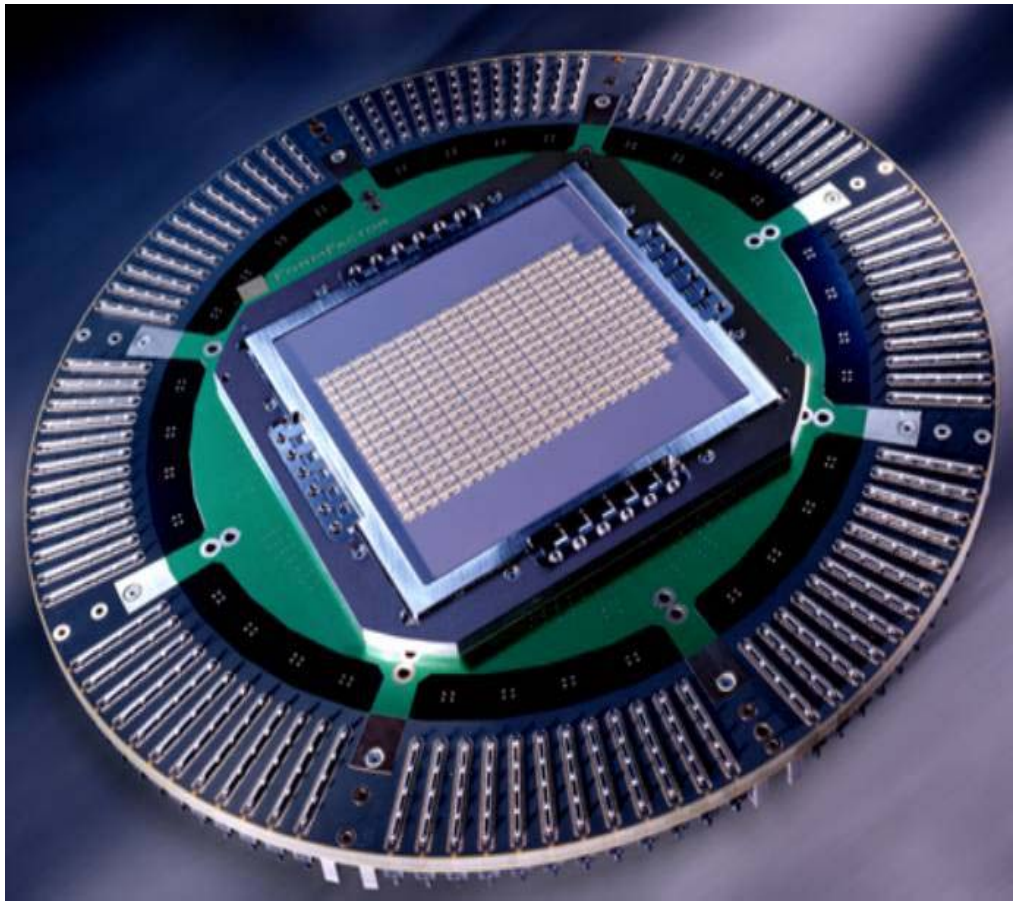
	Perimeter	Parallel Memory	Area Array Square Matrix
FormFactor	-----	MEMS 170	BladeRunner 175
JEM	ECN 45	HAWK 80	VSCC 138
K & S	ECN 37	CobraP 105	CobraP 105
MJC	ECN 47	ECN 50	-----
Wentworth	ECN 50	Cobra 100	Saber 132
TCL	ECN 48	ECN 48	-----
MicroProbe	ECN 42	Apollo 100	Apollo 120 x 115
SV Probe	ECN 37	ECN 80	Hybrid ECN 125
Phicom	ECN 90	MEMS 90	-----
Cascade μT	MEBR 50	-----	-----

ECN = Epoxy Cantilever Needle; MEBR = Membrane

IV. Highest Pin Count

	Parallel Testing	Area Array
JEM	4860 for 64 DUTS	5000
Wentworth	4480 for 64 DUTS	5700
K & S	3000 for 60 DUTS	4264
TCL	1248 for 32 DUTS	-----
MicroProbe	1800 for 32 DUTS	5700
SV Probe	800 for 160 DUTS	3000
MJC	4672 for 64 DUTS	-----

The Leading Edge: FormFactor for Parallel Memory Probing



PH 150, 6 Inches

9867 contacts

253 parallel DUTS

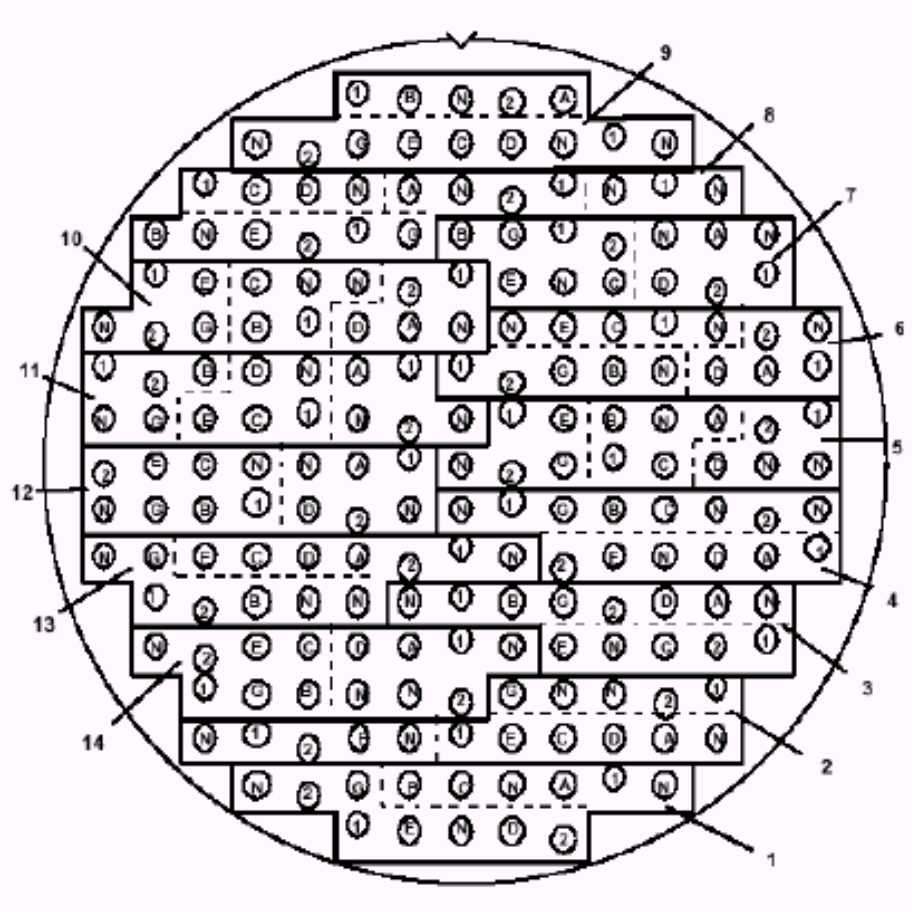
6 touchdowns

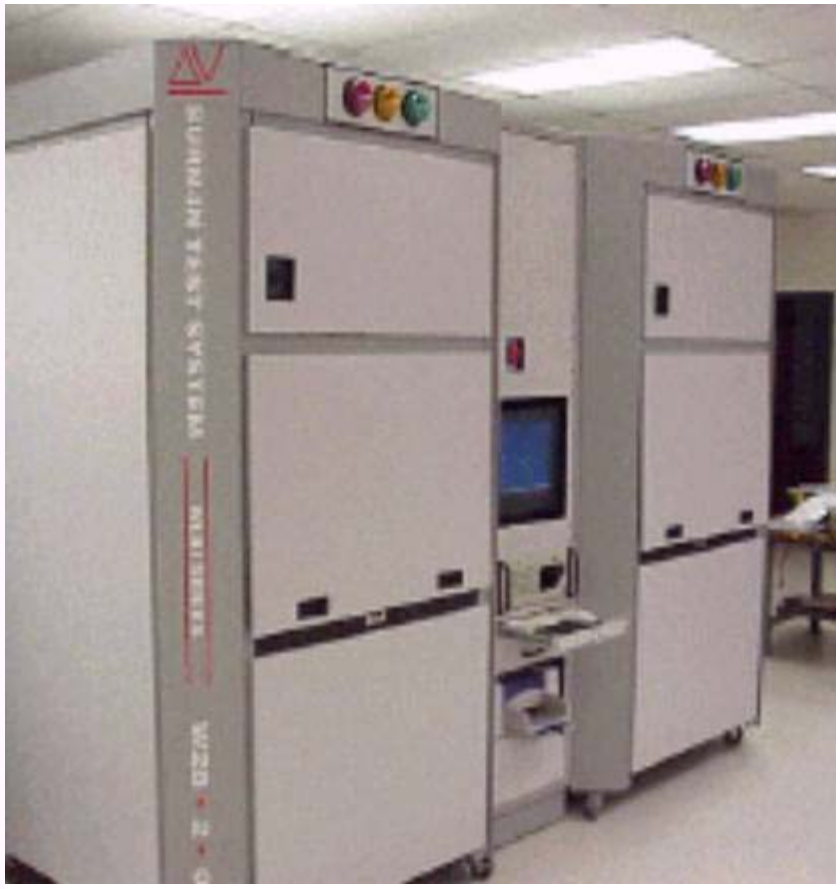
300 MM wafer

IV. Full Wafer Contact

- **Leader: Motorola for Automotive K G D**
- **Full 200 MM wafer contact in conjunction with Wafer Level Burn In**
- **Extensive use of Memory BIST during BI**
- **Multiple parallel die are in 14 clusters**
  - **Sacrificial metal layer interconnects die**
  - **Die I/Os are spread out to lower the pitch**
  - **Temporary BI & test I/Os using top metal layer**
  - **Extra metal layer is removed before delivery**

Motorola Wafer and BI System

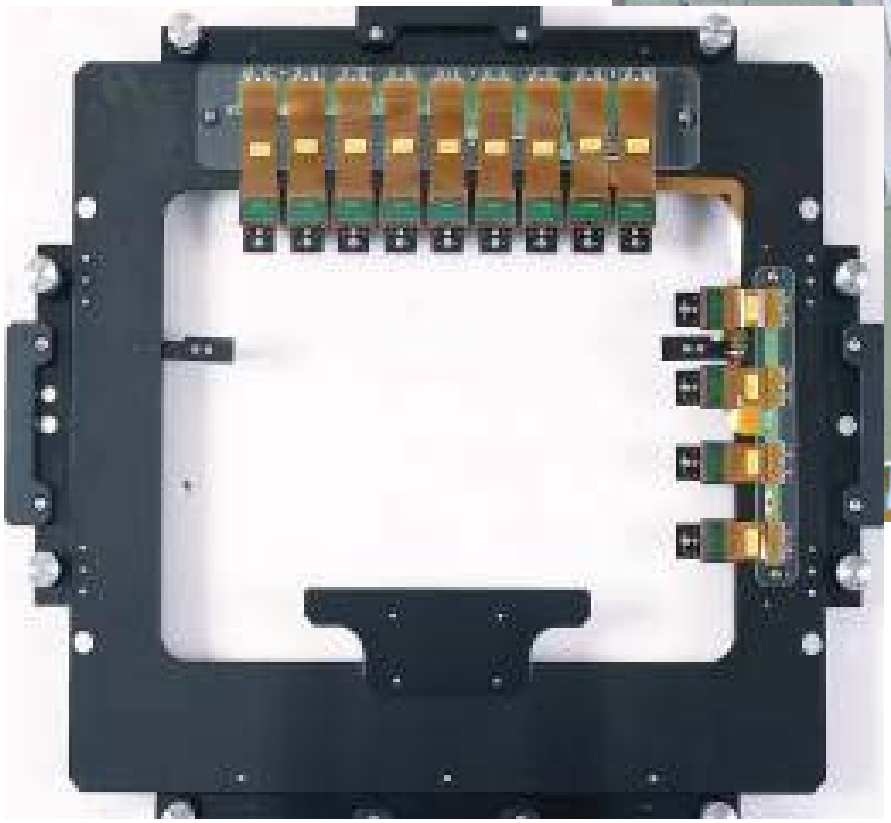




AEHR Wafer BI and Test System

- True full wafer contact to individual die I/Os
- Contactors are pogo pins (200 U Pitch)
- New contactors are nano-springs (60 U)
- Electroglas equipment for wafer alignment
- Air pressure cassettes hold wafer to BI PWB

V. Biggest Probe Card: Phicom



52” By 52” For LCD Displays

V. Biggest Prober: MJC TP 4800 for 1.3 X 1.5 M LCD Displays

By the way,
Next Gen LCD = 1.87
x 2.2 Meters!

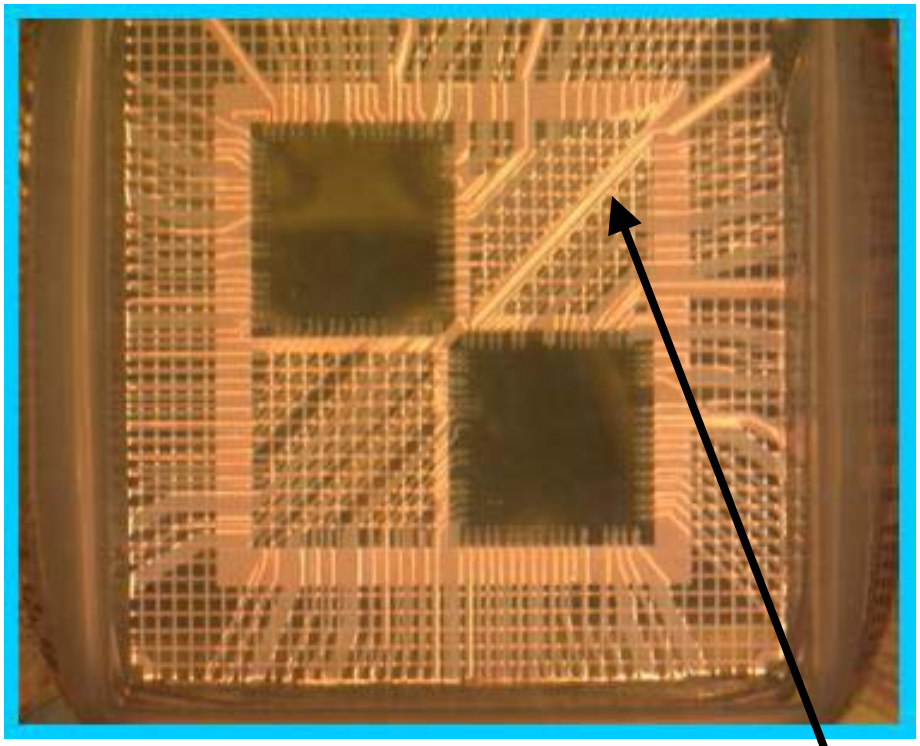
VI. Highest Frequency (4 Classes)

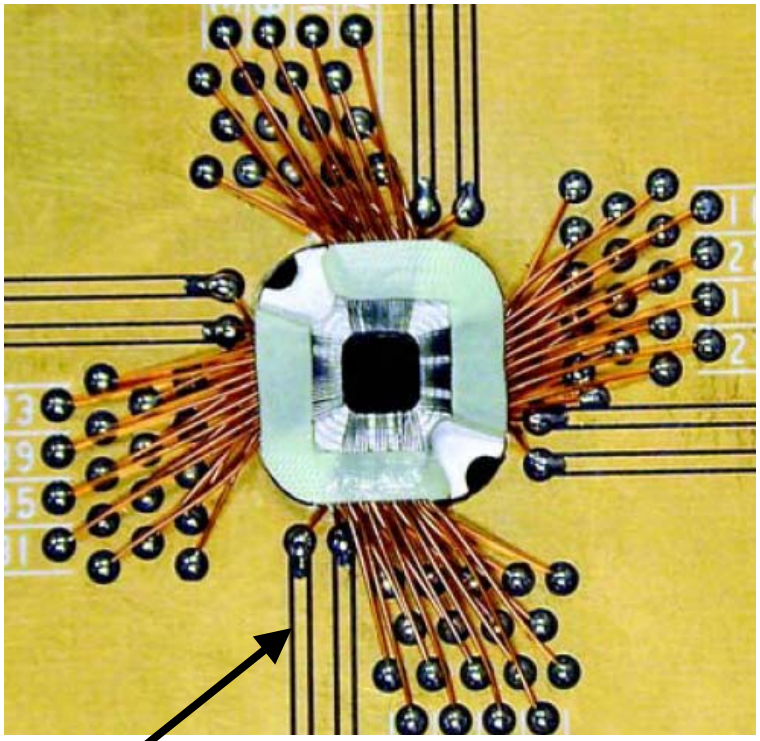
- **High Speed Digital**
  - **Single ended I/Os; very high dv/dt**
  - **Conventional Automatic Test Equipment**
- **Consumer RF Devices**
  - **Controlled impedances; modulated sine waves**
  - **Single ended outputs; conventional RF ATE**
- **Telecom Chips**
  - **Within and at the edge of the Internet**
  - **Balanced and differential I/Os**
  - **Lower volume, rack and stack ATE**
- **Process Evaluation Monitors**

Highest Frequency

- **High Speed Digital**
  - **800 MHz for Graphics RAMS (GDDR II)**
  - **Single ended data but differential clocks**
  - **Switchable termination resistors inside chips**
  - **Variable impedance drive to match tester**
  - **Membrane and epoxy needle probe cards**
- **Consumer RF Devices**
  - **7.2 GHz for Blue Tooth and IEEE 802.11 (3rd harm.)**
  - **Up to 150 I/Os as chips become more integrated**
  - **Cascade Microtech membrane cards**
  - **K & S "Speed Tip" RF Cards**

Casacade Microtech Membrane and K & S Speed Tip Probe Cards



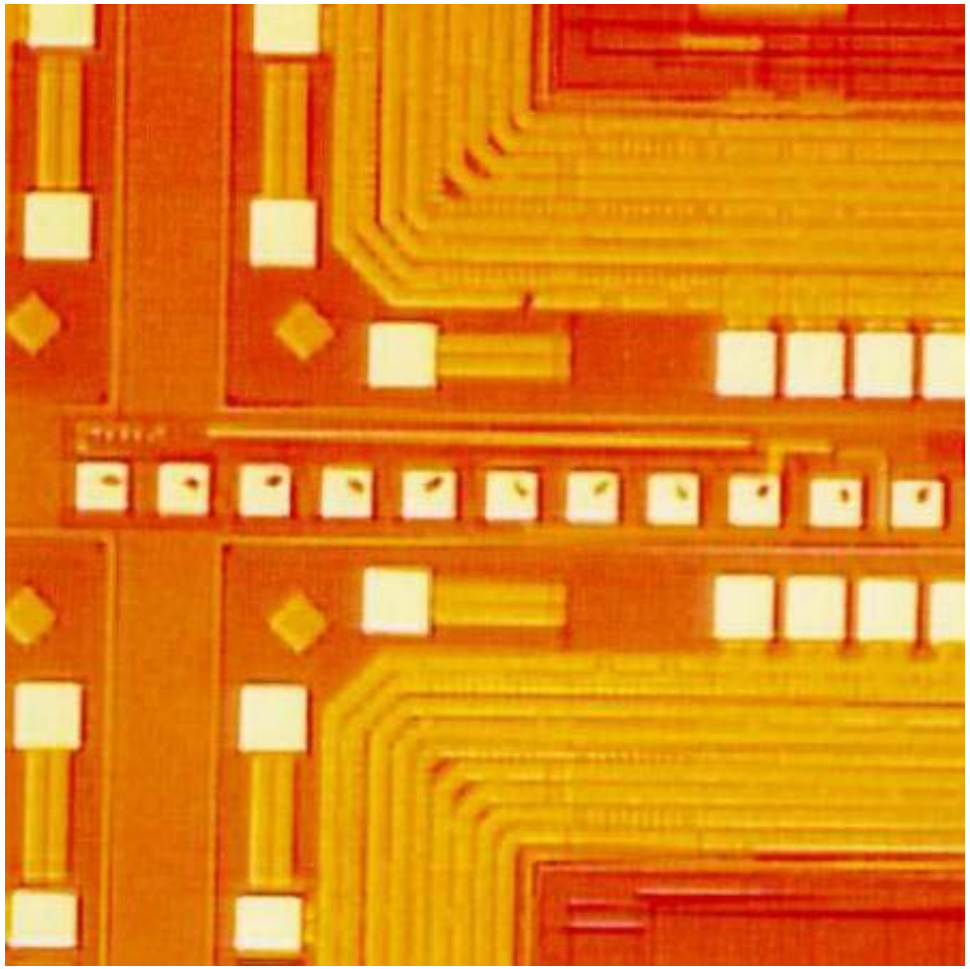


Stripline Controlled Impedance

Telecom Chips

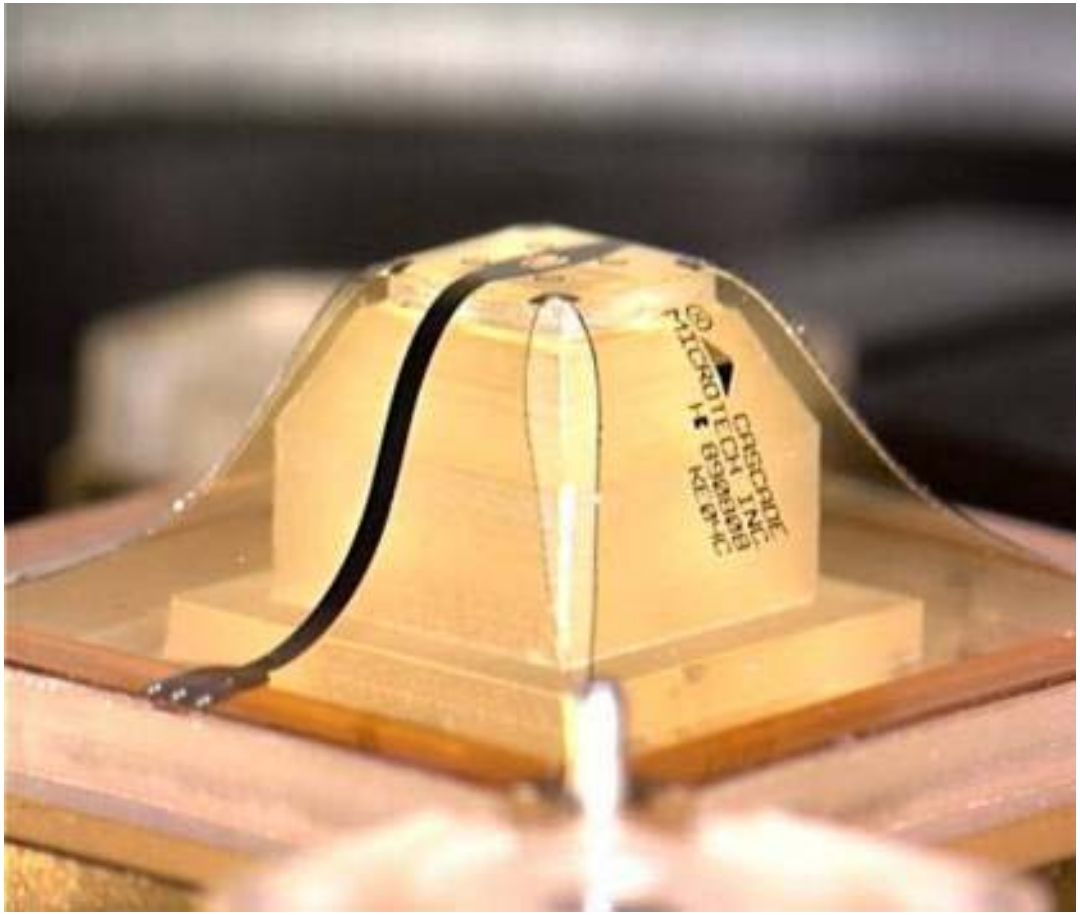
- **4 GHZ for Serial/Deserializer Chips**
  - SERDES drivers and receivers on probe card or load board (testers can't go that fast)
  - DFT digital loop back inside the chips which enable much of the functional testing
  - Probed with "conventional" epoxy needle cards
- **40 GB/S OC 768 Sonnet Devices (20 GHz)**
  - 12 – 15 Pico Second Edges, 60 GHz BW
  - Rack and Stack Test Equipment
  - Probed with membrane cards

Process Evaluation Monitor



- Electrical process monitors: E-Test or Wafer Map
- Process test transistors located between die in the chip scribe lines
- Sampled in production, a few devices per wafer, & a few wafers per lot

Leading Edge: 40 GHz

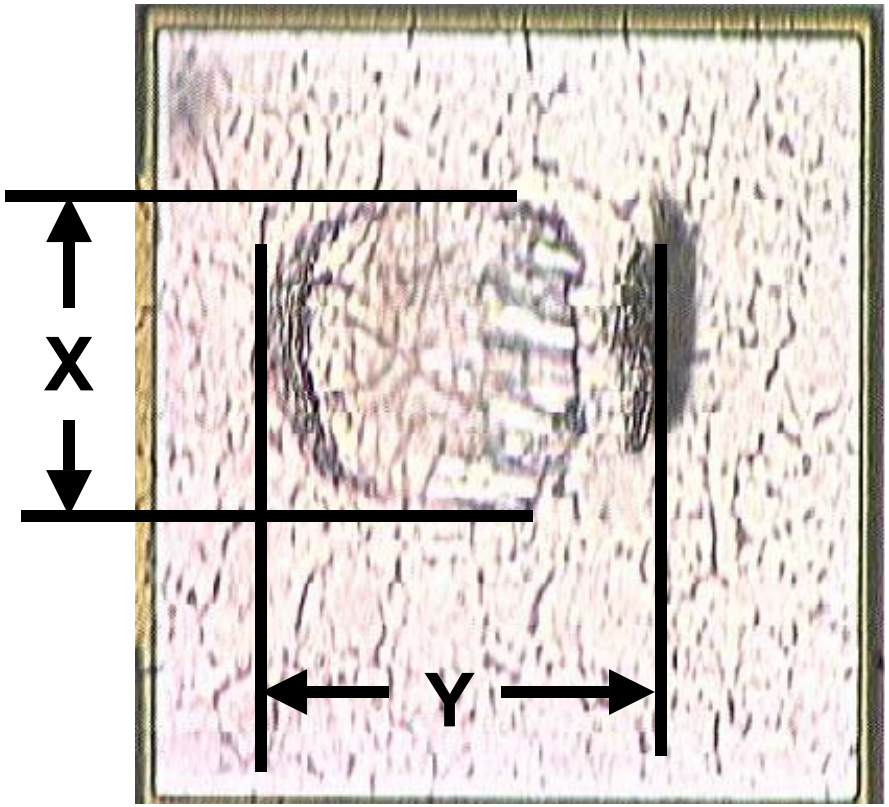


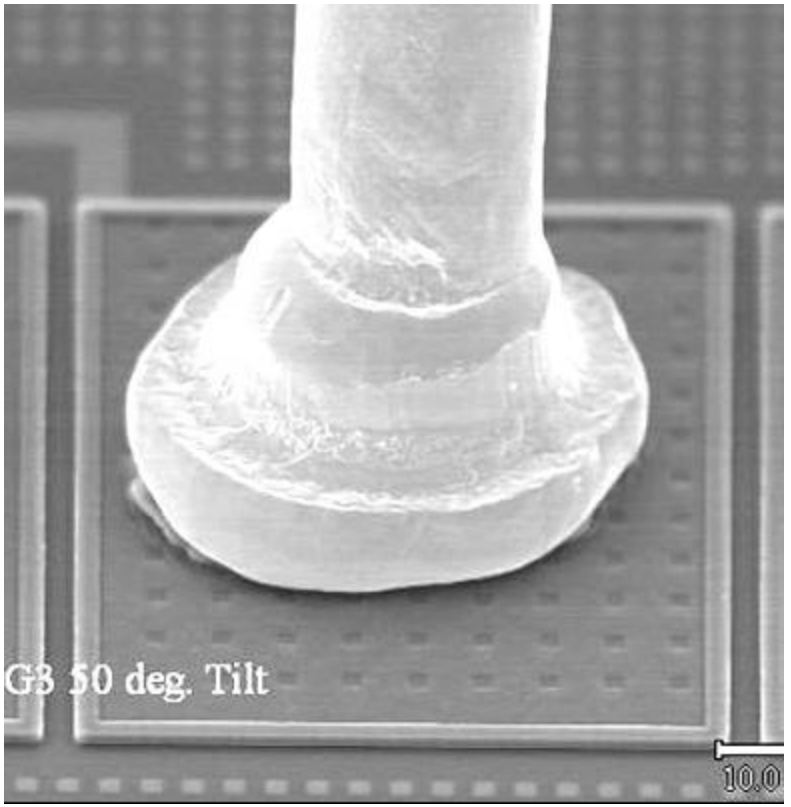
SiGe & GaAs

Full S-Parameter Measurements

Tested with Membrane Card

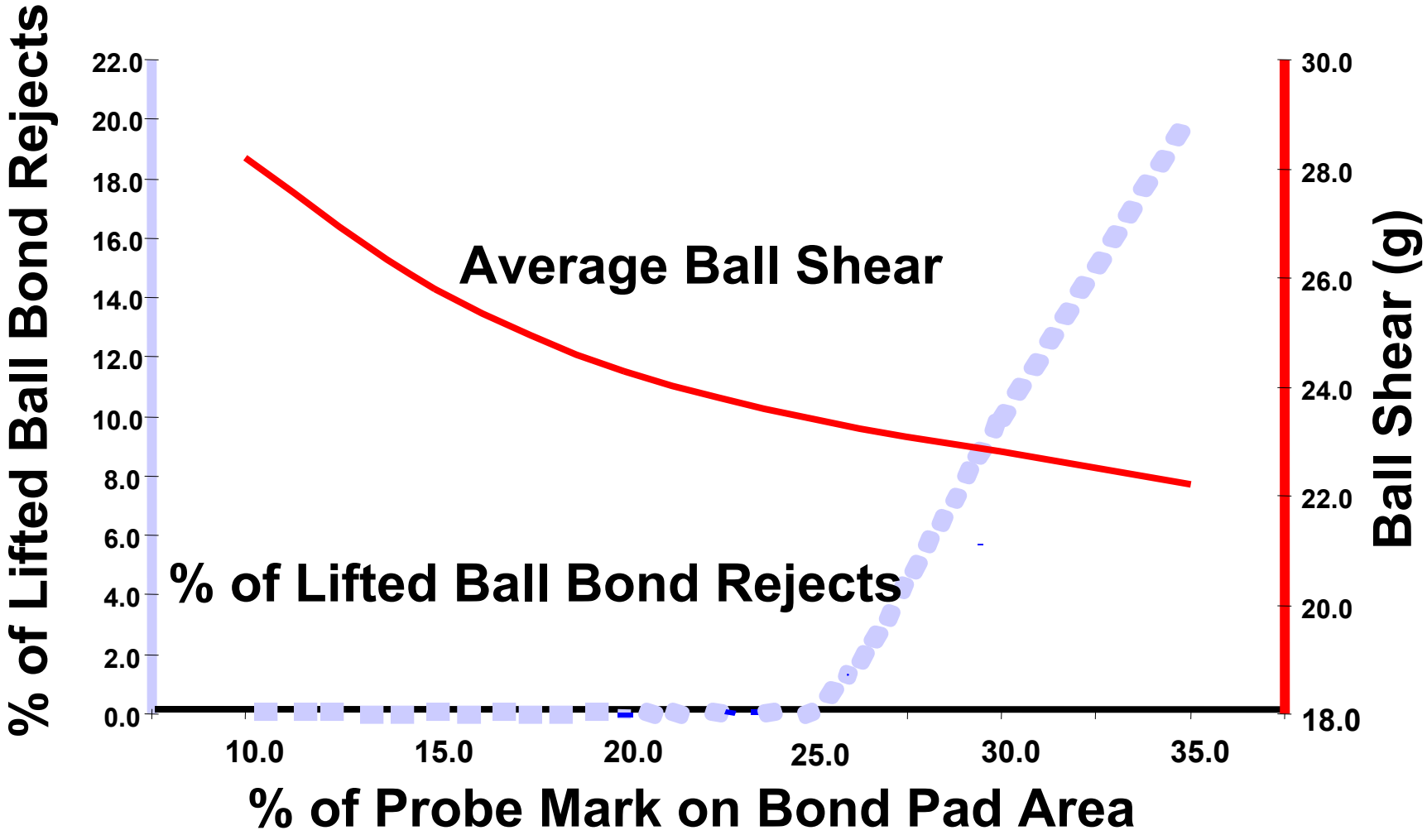
VII. I/O Pad Damage





Excessive needle scrub marks are causing poor ball bond adhesion

Infineon, IBM, ATLAS Data

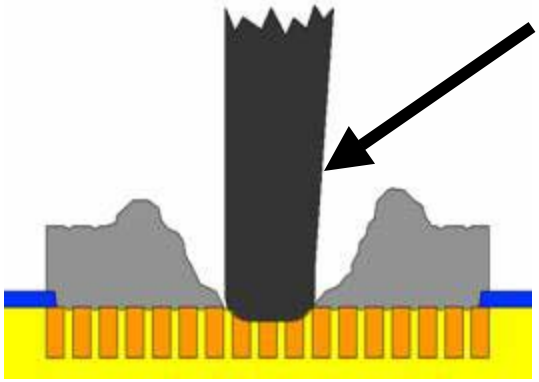


Initial Pad Damage Control

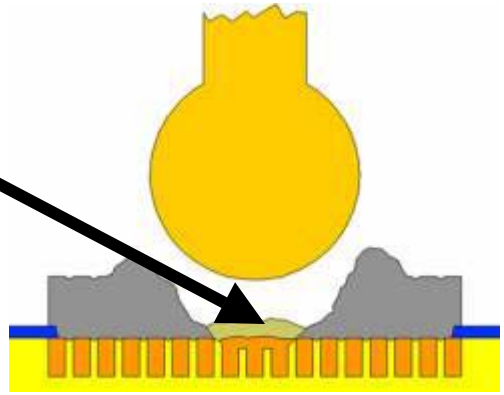
- Preliminary characterization
- Optical scanners
  - Initially developed for card needle accuracy
  - Now being used for scrub mark characterization
  - One hour per wafer!
- Quickly moved to rectangular I/O pads
- Probe card must be parallel to chuck
- Better prober chuck flatness
- Tighter card planarity (.5 mils to .3 mils)
- Controlled over drive and over travel

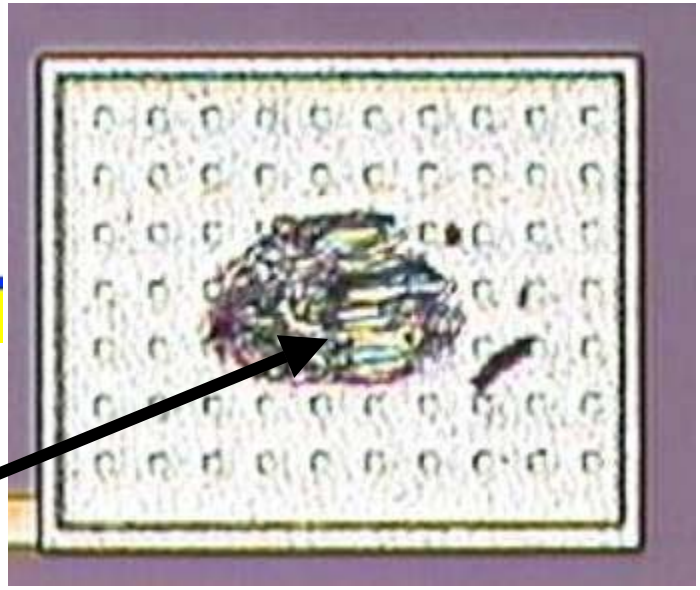
Copper Metalization Made The Problem Even Worse

New processes with smaller I/O pads needed smaller and sharper needles; increased chance to punch through the Al pad and expose copper



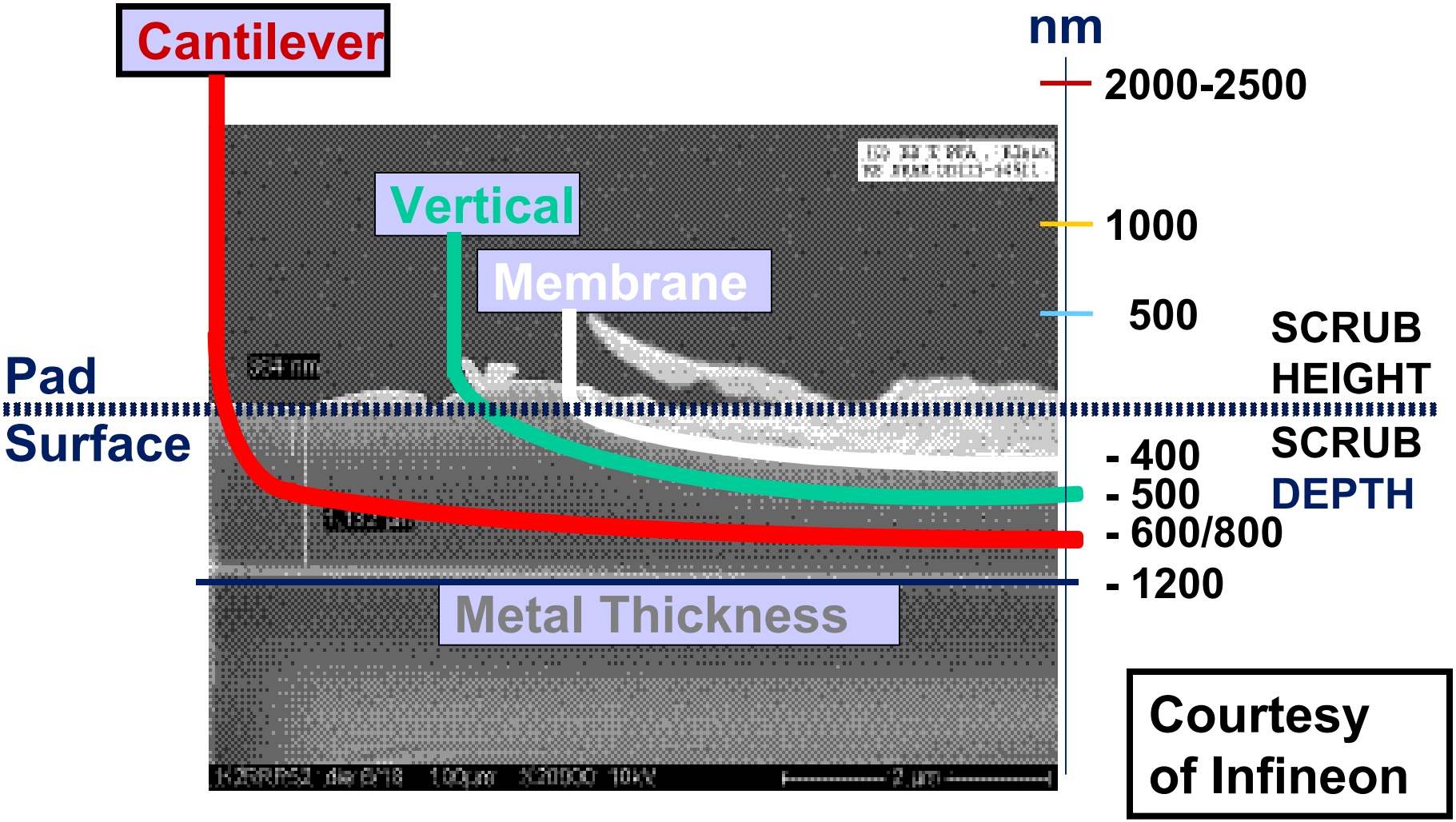
Exposed copper oxidizes fast and adversely effects the ball bonding



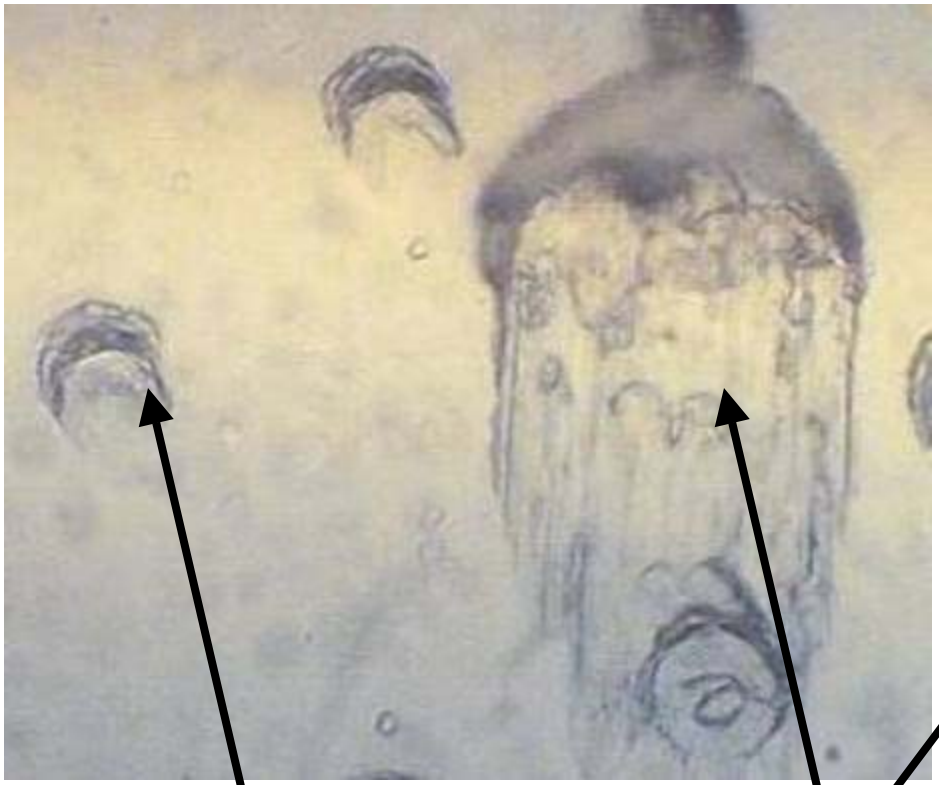


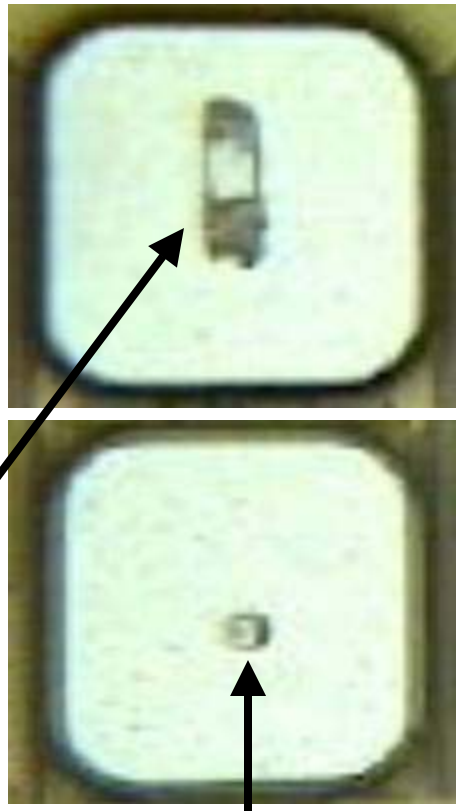
Exposed copper on I/O pad

Pad Damage Versus Technology



Least I/O Pad Deformation





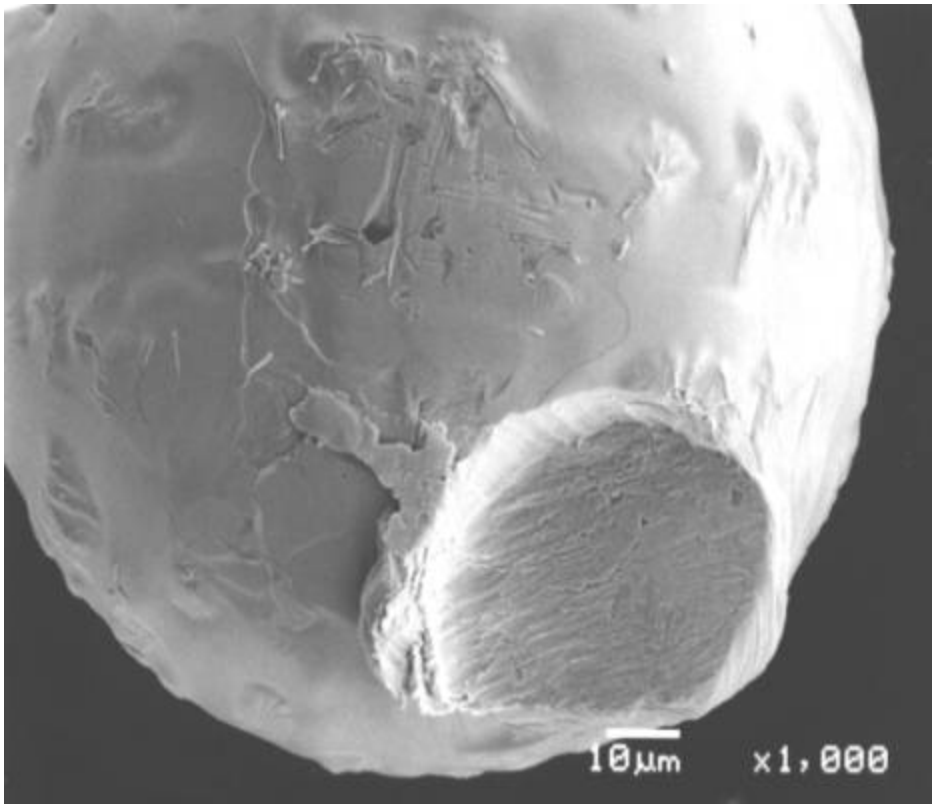
Membrane Scrub Marks

Conventional Epoxy Ring

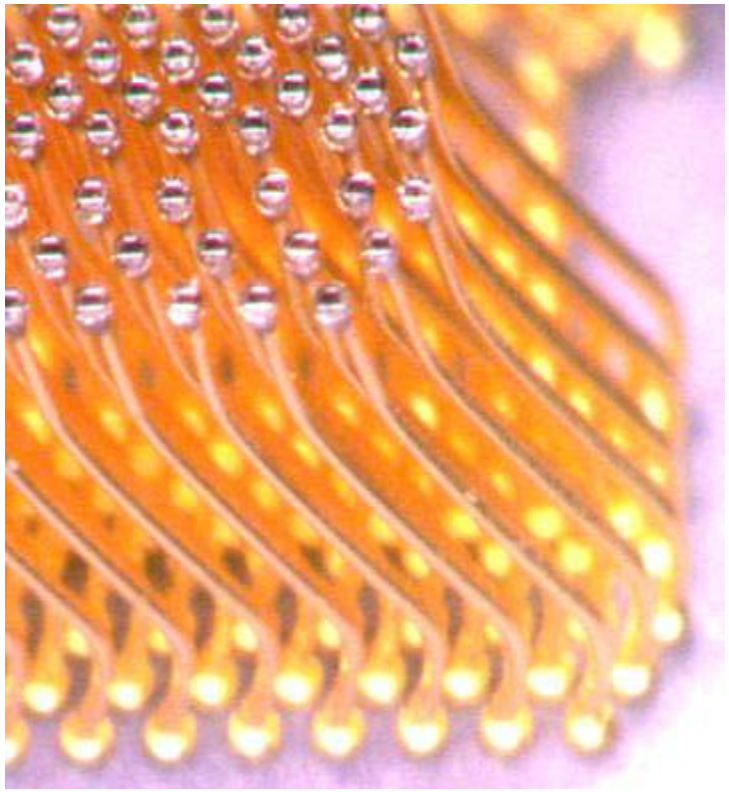
Microprobe Apollo (vertical)

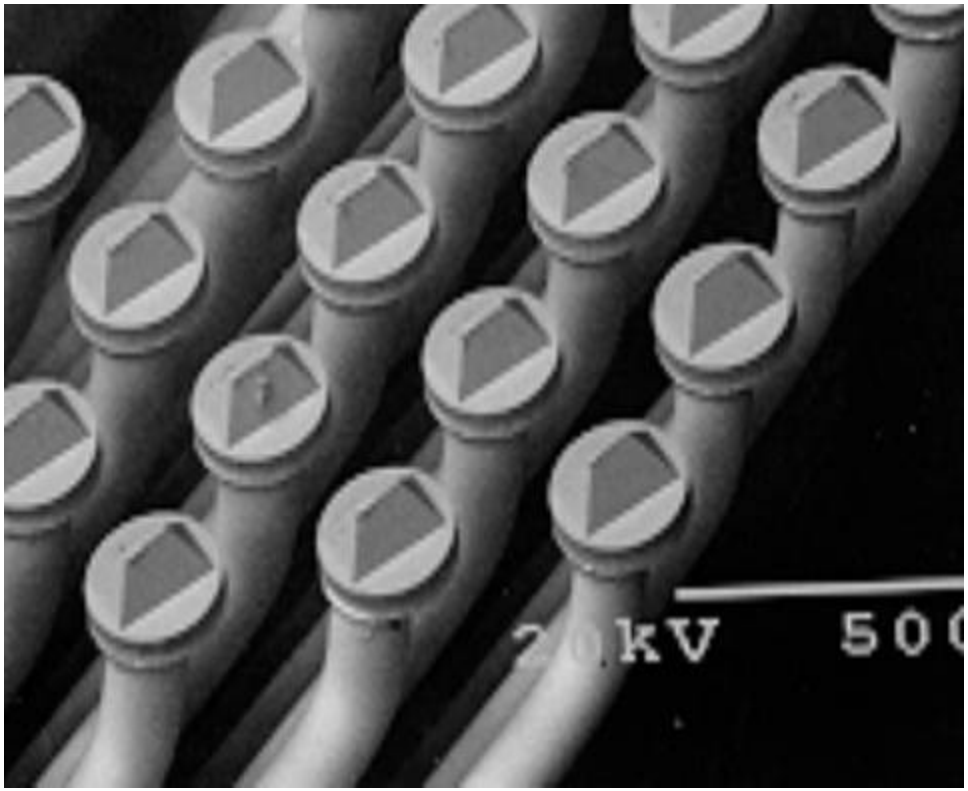
I/O Pad Damage Has Long Been a Problem for C4 Balls

- Solder ball adhesion to pad was critical
- Probe after C4 ball attach
- Ball deformation cause problems in die adhesion to package



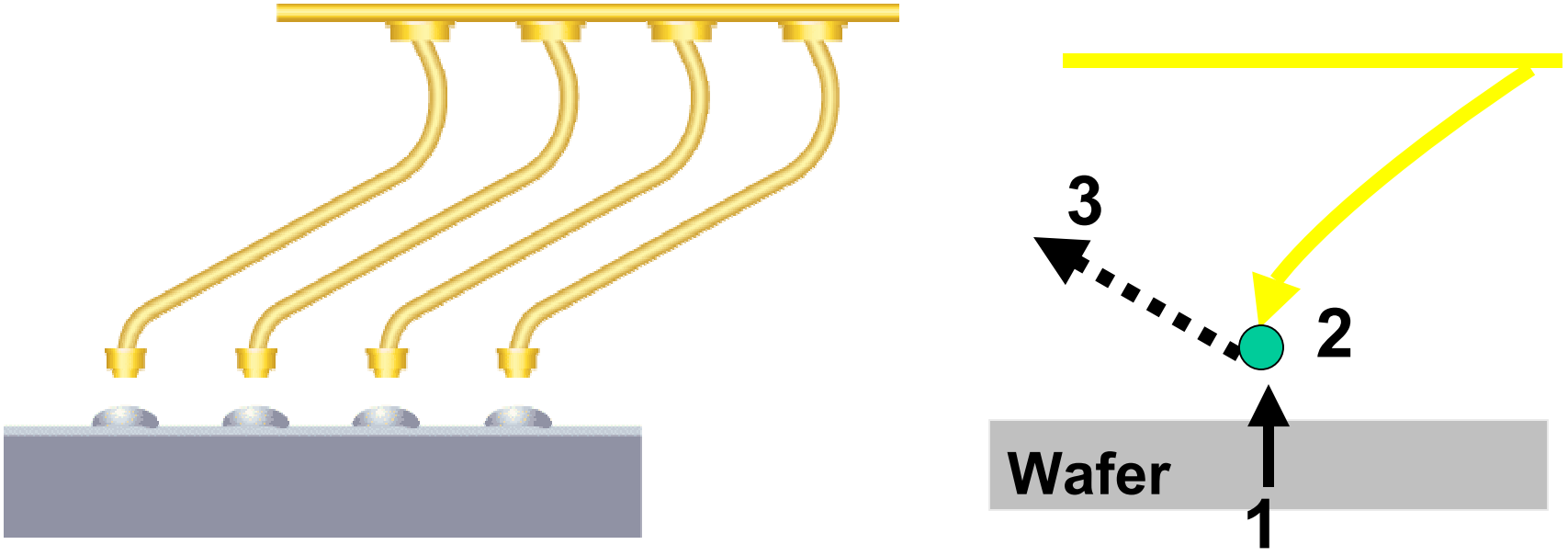
FormFactor Introduces “Blade Runner” for Area Area Probing





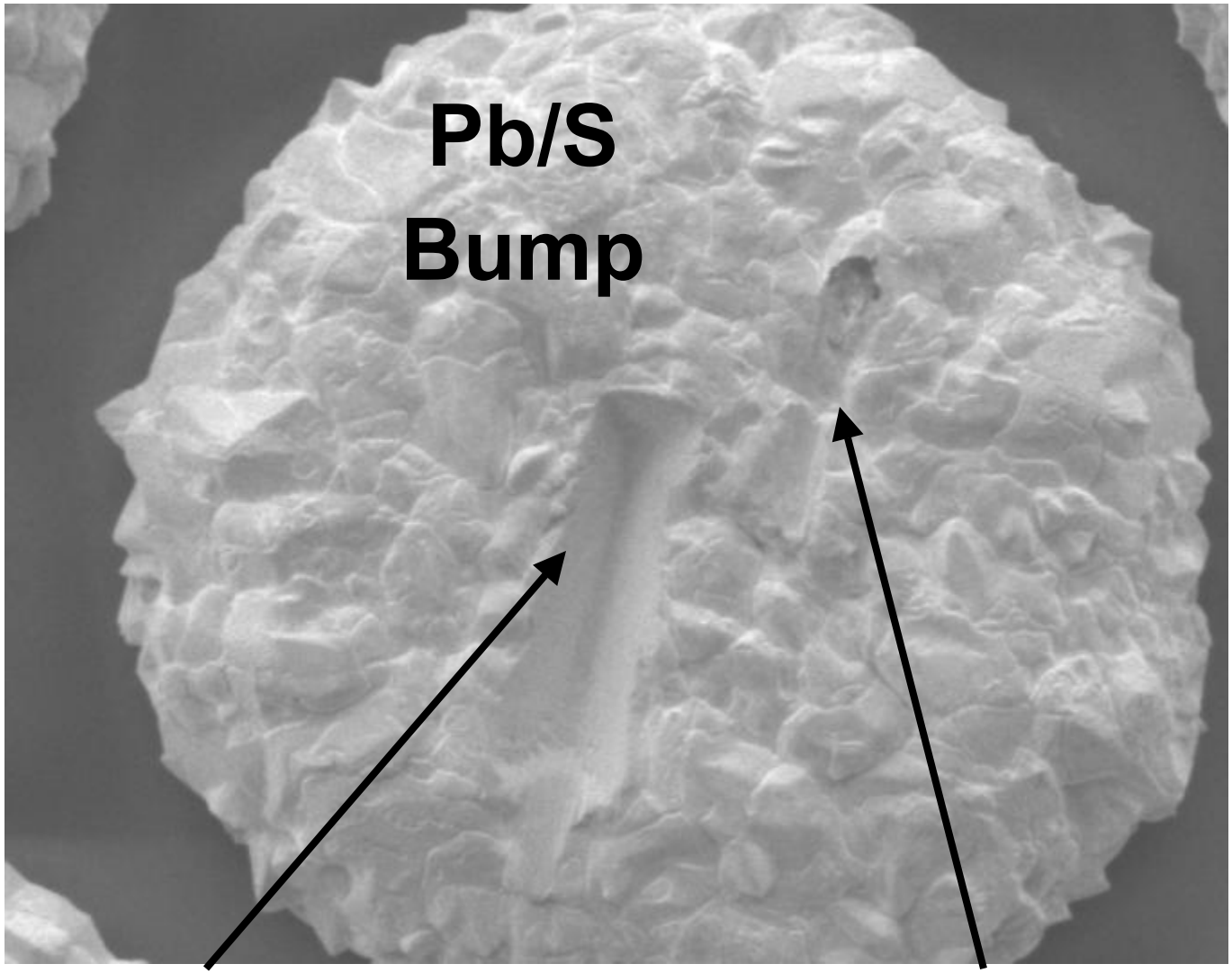
Third Generation needles combined springs and vertical concepts
Enabled finer pitch but had excessive vertical force
Needed unusual probing technique to minimize deformation

MicroForce Probing Technique: Intel, TEL, and FormFactor

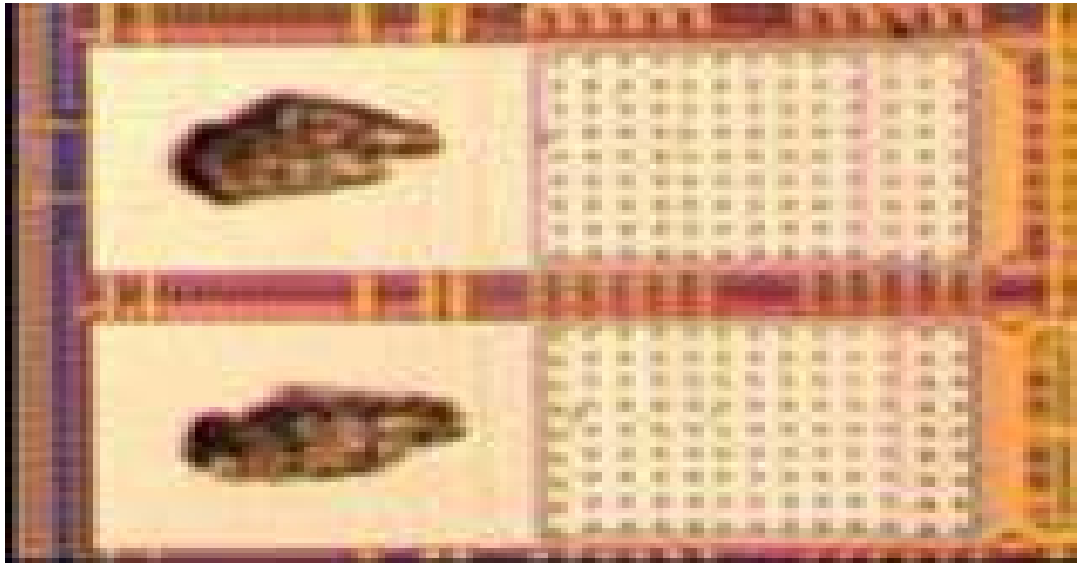


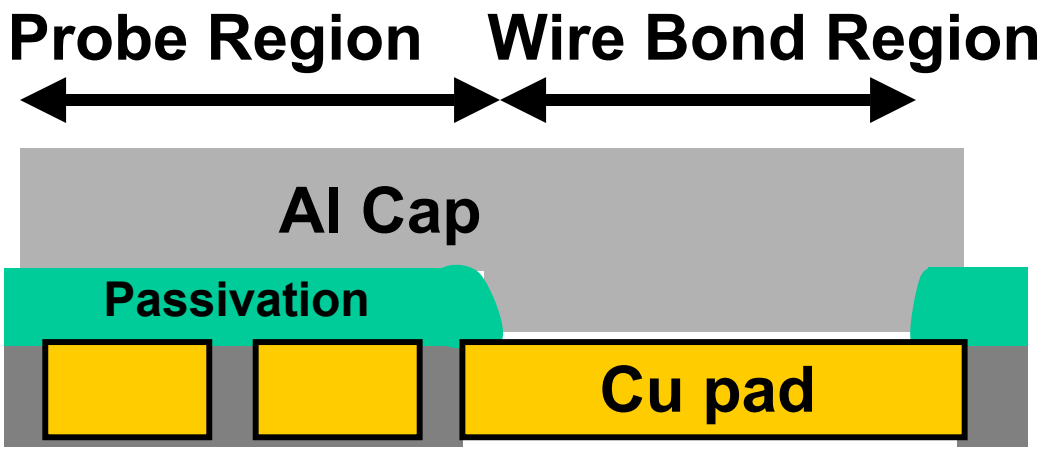
1 – Prober Chuck Moves in Z-axis
2 – Contact with Flip Chip Bump
3 – Chuck moves in X-Y-Z

Solder Ball Probe Mark Comparison



Motorola's "Probe Over Passivation"



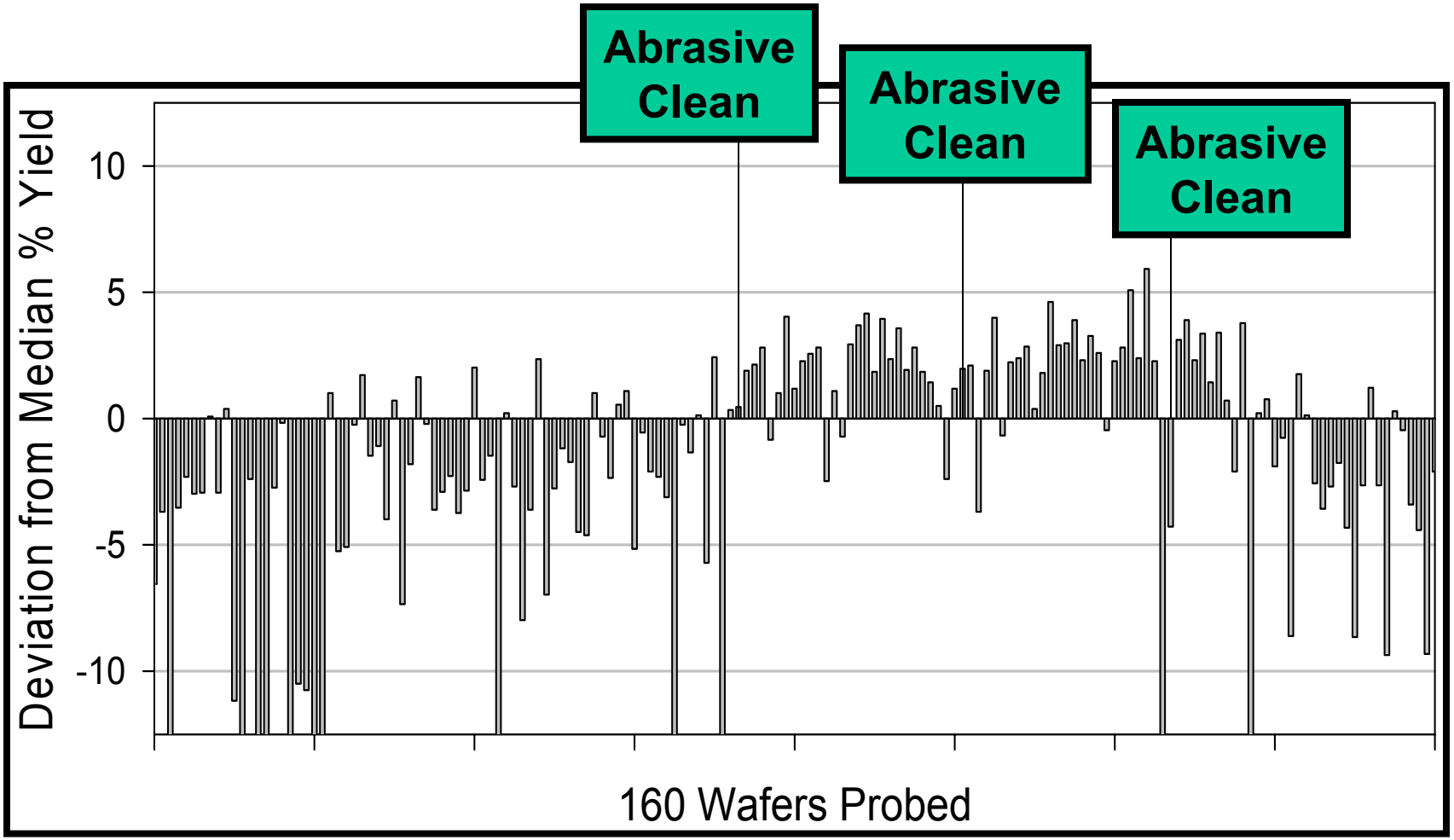


- Eliminate probe and wire bond interference
- Creates longer bond pad but it DOES NOT increase die size
- Requires only 1 mask change
- Eliminate Cu exposure due to probe marks
- Ease of implementation on existing and new Cu technology products

VII. Probe Needle Cleaning

- Probe needles pick up debris in probe process
- Yield falloff noted with continuous probing
- Contact resistance increases (a coincidence?)
- Probe needle contamination investigations
  - SEMs and EDX analysis of contamination
  - Analytical and empirical investigations
- In-Situ abrasive cleaning was initially used
  - Cleaning the needles during the probing process
  - Demonstrated reduced contact resistance and stabilized yields

In-Situ Abrasive Cleaning

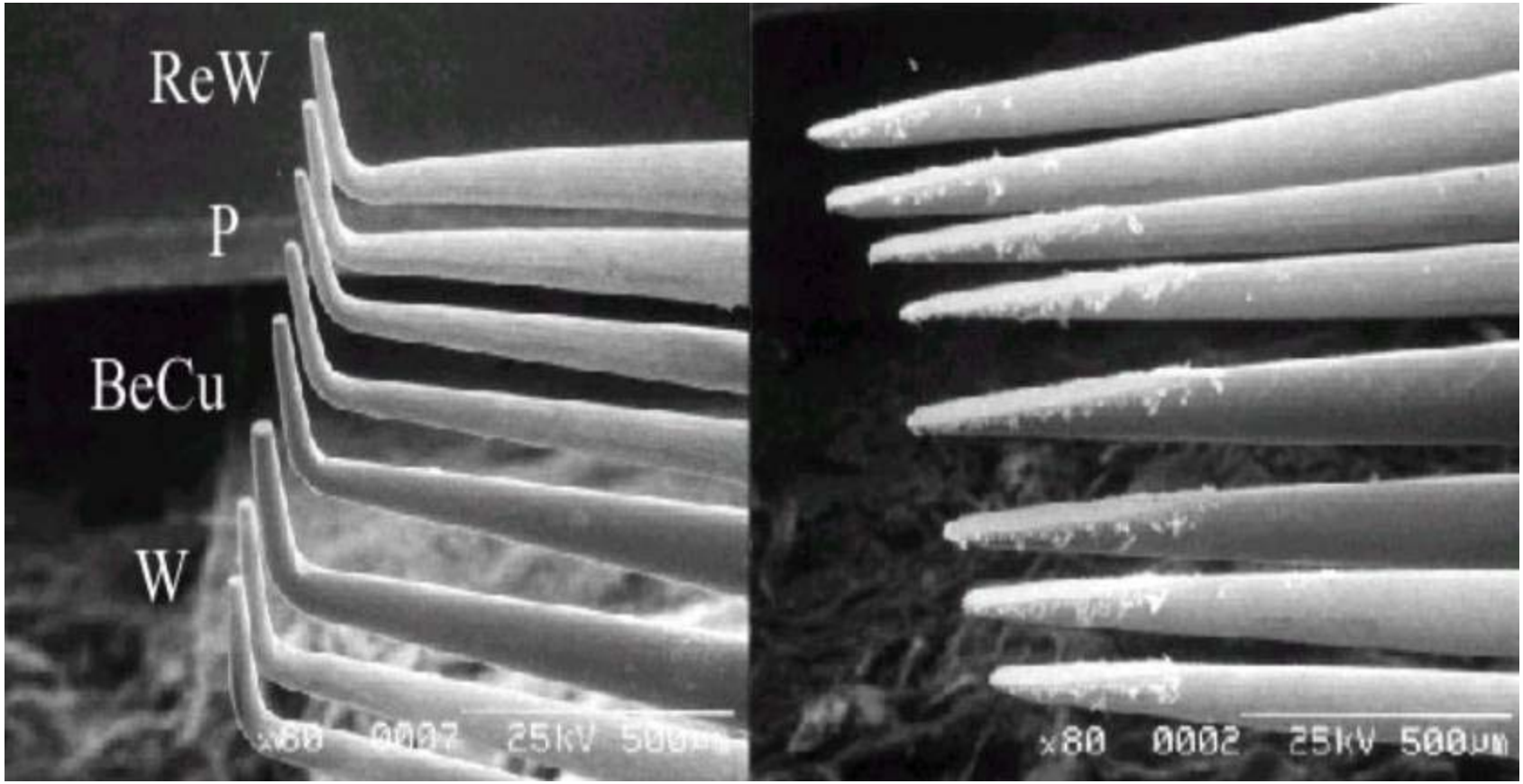


Abrasive Cleaning Implementation

- **Prober chucks have areas for abrasive cleaners**
- **Lapping film, ceramic and tungsten carbide plates are frequently used**
- **Chuck moves to place cleaning sites under the needles**
- **Programmable cleaning motions and frequencies**
- ***Empirically determined* but very widely used…**

If it works so well, just use it!

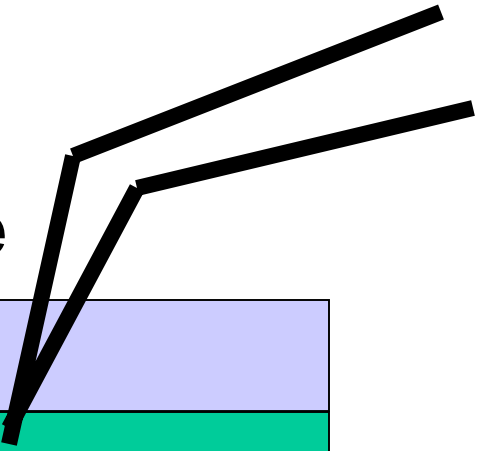
Abrasive Cleaning Works Well But It's Also Destructive

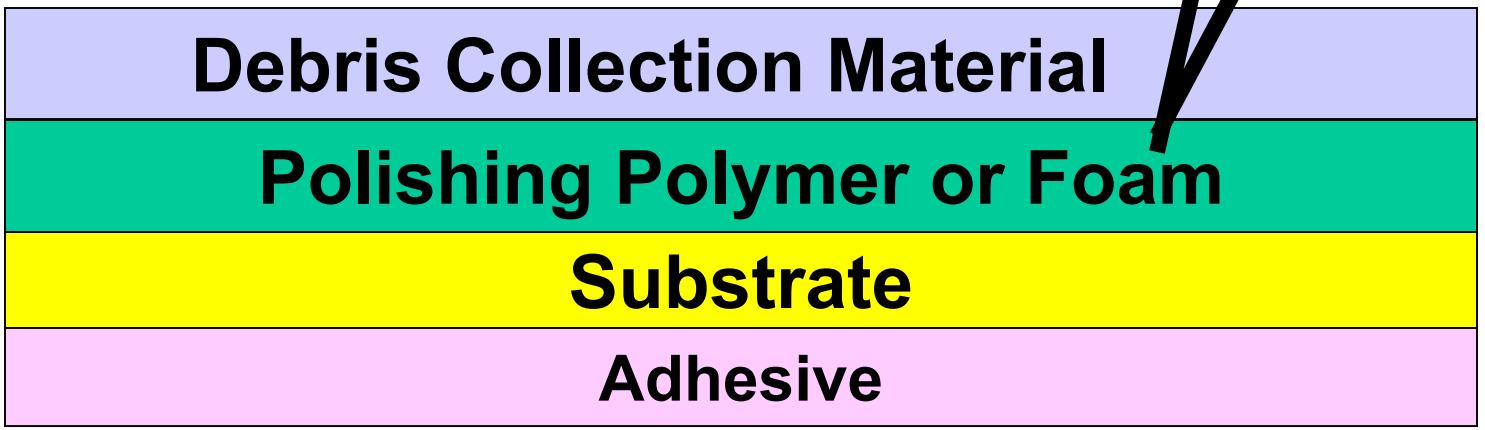


Initial Probe Needles After 100K Cleans!!!

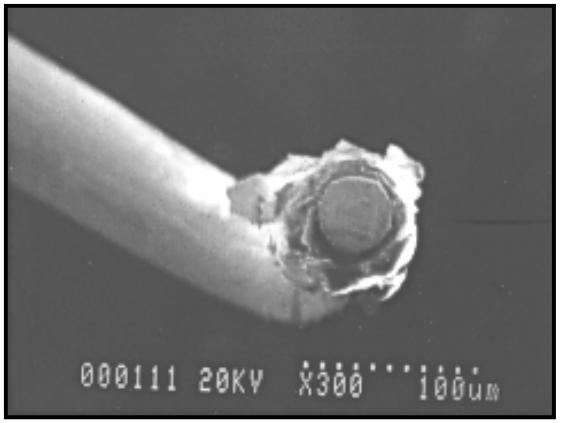
Needle Cleaning Leading Edge:
Semi-Abrasive Cleaner & Polish

- Provided by ELMO, ITS, JEM, K & S, Mipox, MJC, and TIPS
- Probe penetrates polymer or foam
- Cleans and reshapes needles
- Much less abrasive
- In-situ (probe chuck) or off line

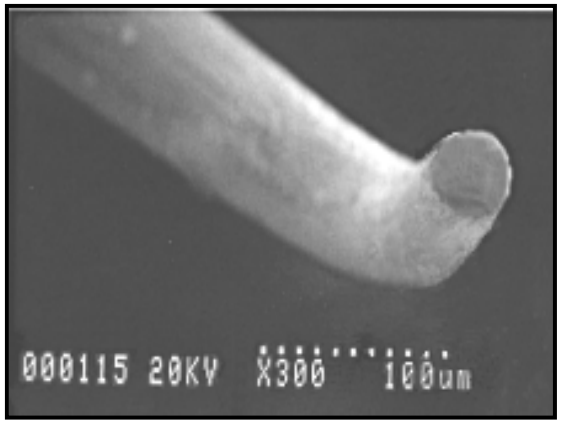




Semi-Abrasive Polish Cleaner



International
Test Solutions
Non-destructive
Probe Cleaning



Off Line Probe Card Cleaning

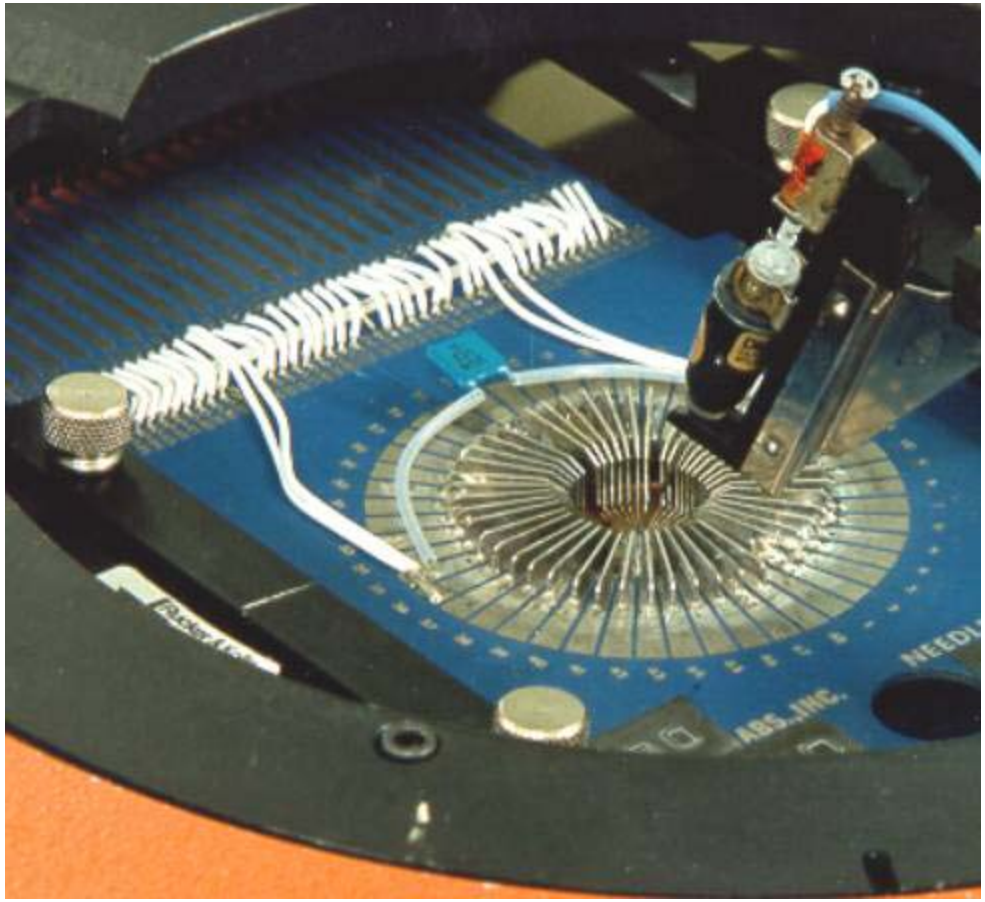
Nippon Scientific Company PC 102

Various chemicals for cleaning

Applied Precision Inc.

Electro Hydro-Dynamic Cleaning

IX. Sorting Bad From Good Chips… The "Good Old Days"

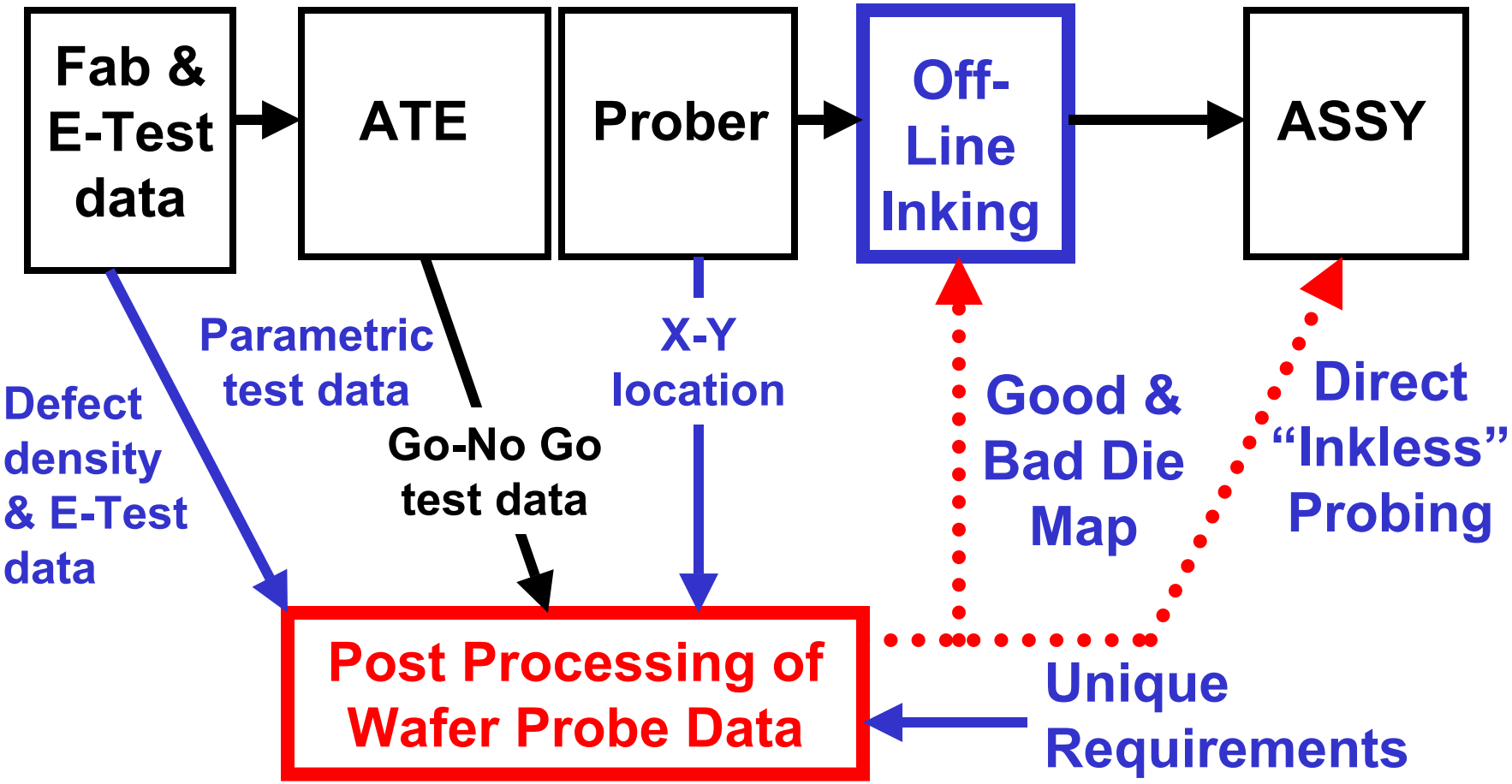


Bad die were determined by a simple pass/fail test criteria

Inker was an integral part of the prober

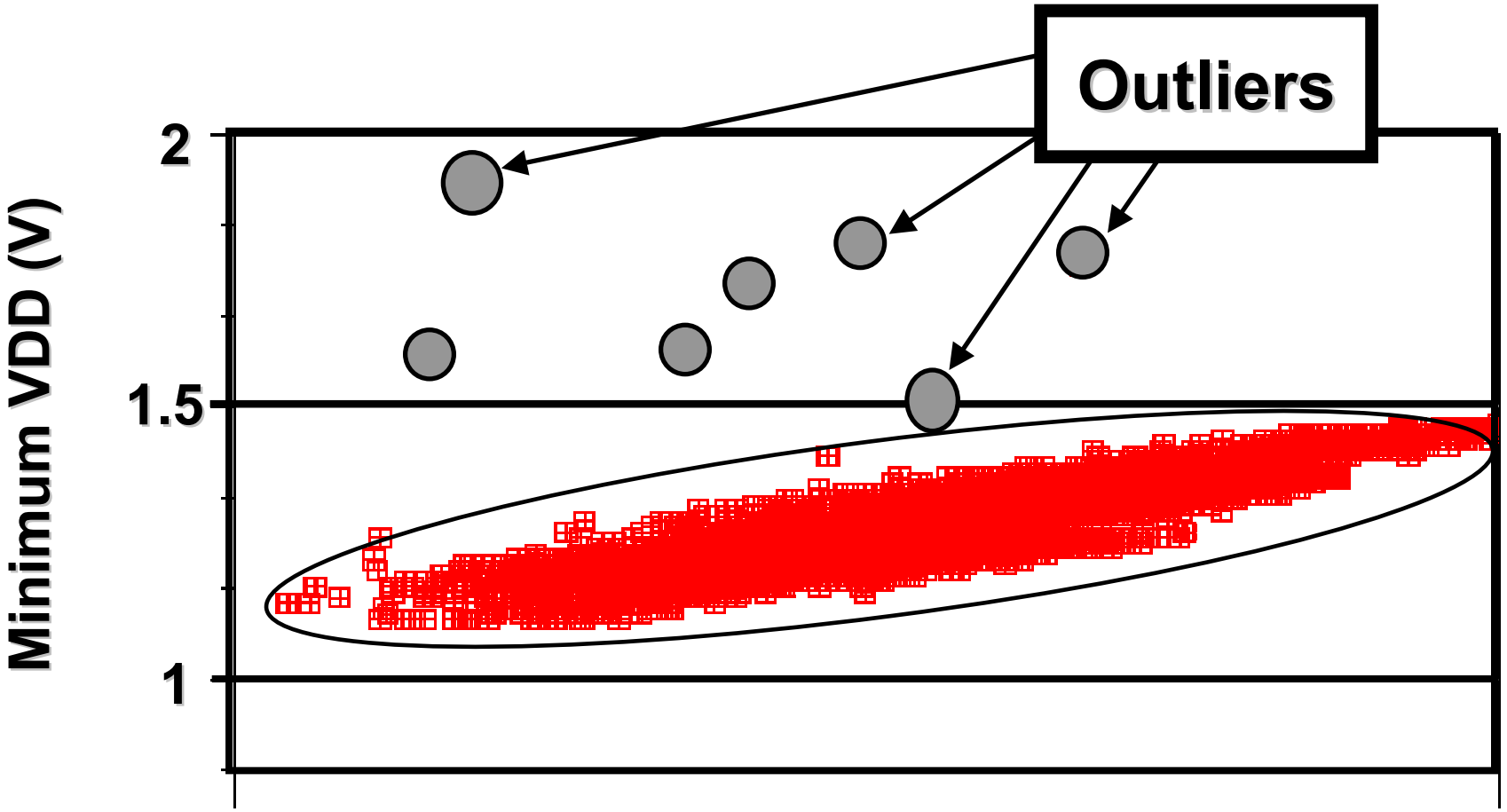
Bad die were immediately inked at the end of the probe test

Today's Leading Edge Sorting



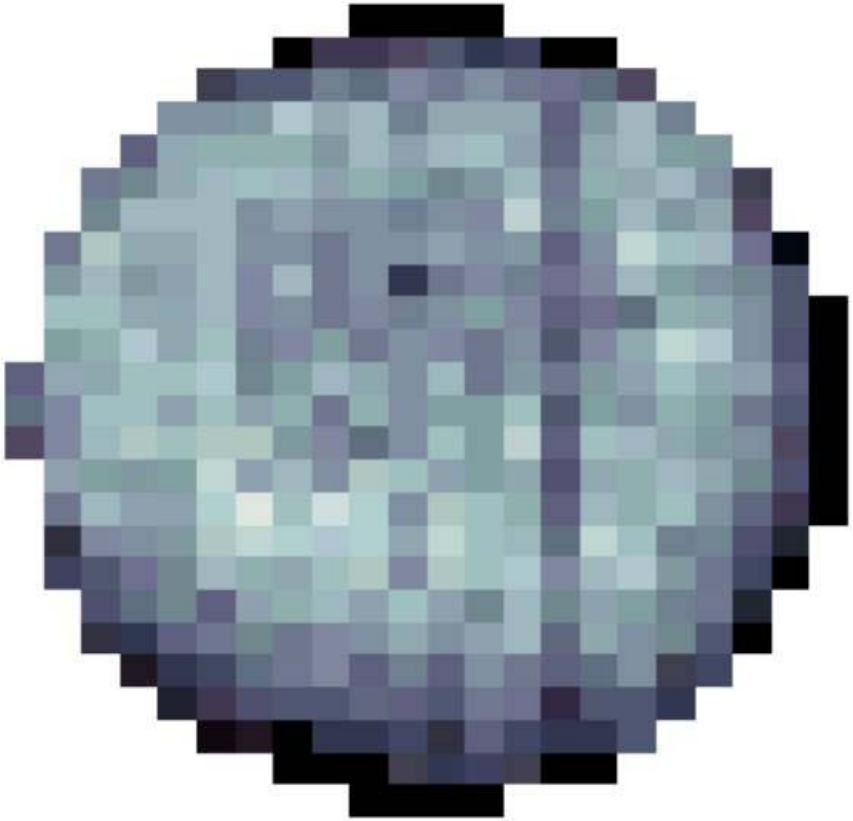
Rejecting V_{DD} Outliers*

Problem: You don't know the outliers until you have completed all the wafer testing!



*Phil Nigh, ITC 2001, Invited Speaker

*LSI Logic and Portland State University: Iddq Nearest Neighbor



Noticeable “donut pattern” for background I_{DDQ} value

Needed “variance reduction” to provide outlier identification

Estimated normal I_{DDQ} by adjacent die values

Subtracts the actual I_{DDQ} from the estimate = Nearest Neighbor Residual (NNR)

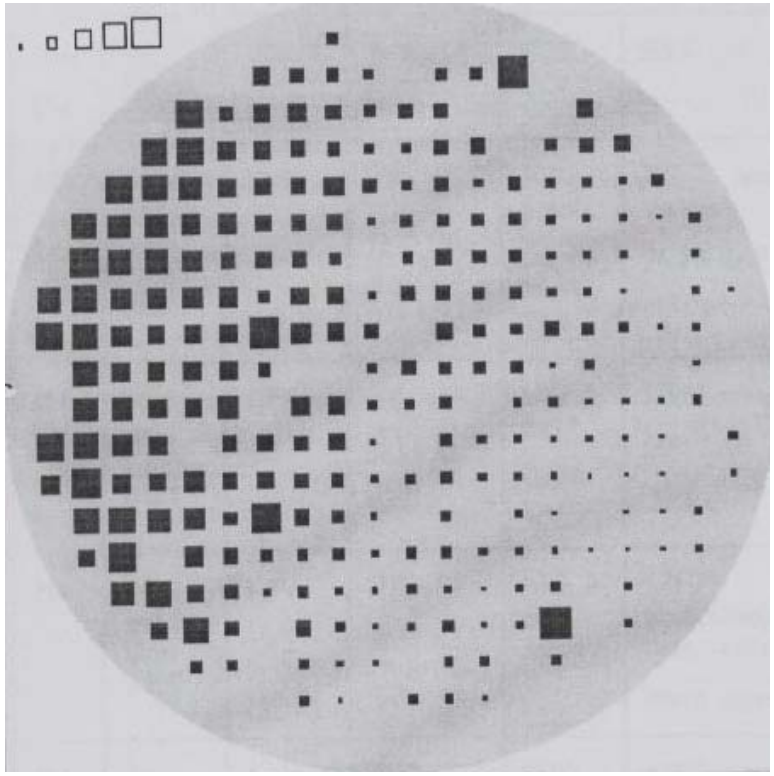
*ITC 2000, pp 189-198, & ITC 2001, pp 1240-1248

*LSI Logic and Portland State University Introduce "Statistical Post Processing" System

- Processes data after the probe test for determination of good and bad die ink map
- Reliability-focused SPP module can down-grade "questionably good" but outlier die
- Outliers based on Nearest Neighbor Residual
- Evaluated an LSI Logic's .18 micron devices
- Demonstrated 30% to 60% reduction in Early Failure Rate

*VTS 2002, Paper 4.1

*The Same Group Extended Work to V_{DD} Min Outliers

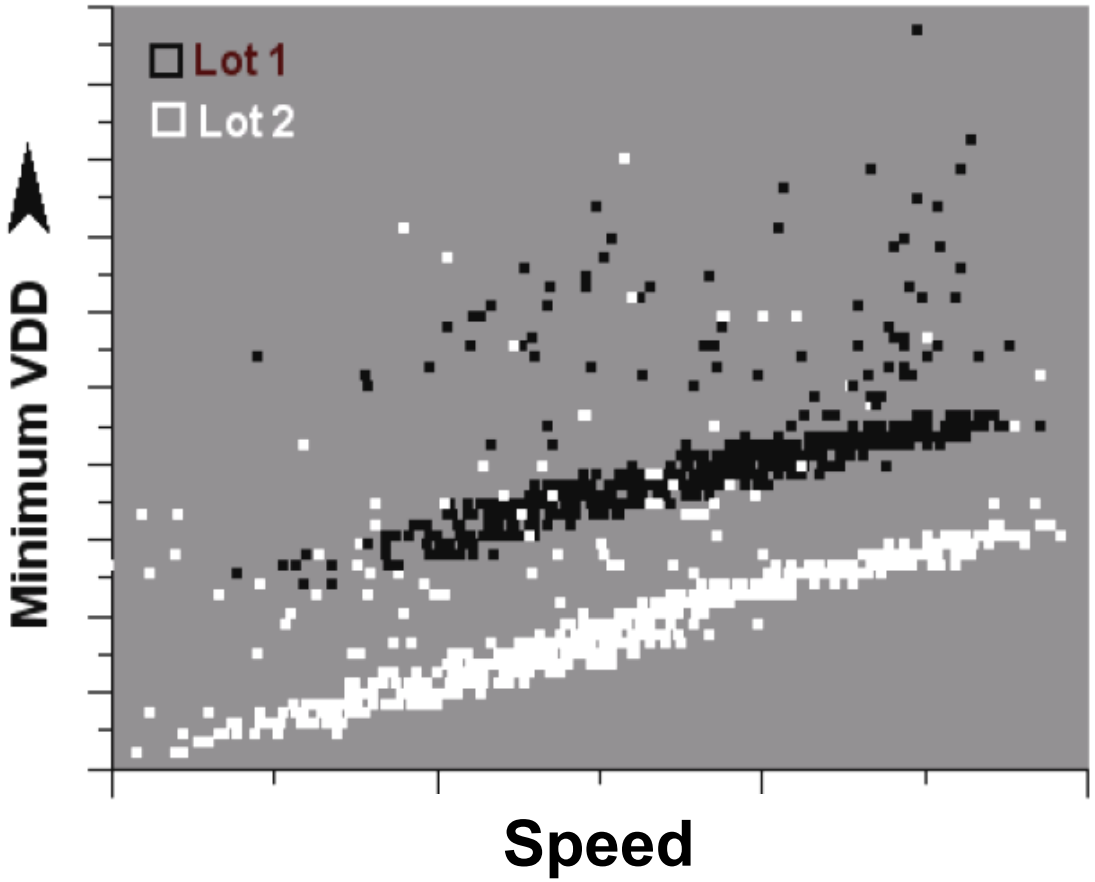


V_{DD} Min versus Die Location

- Extensive work to determine V_{DD} Min with reasonable test time impact
- Initially used a Reduced Vector Set (RVS) and binary search
- Feed forward parameters for full test vector characterization
- Applied Nearest Neighborhood Residual to determine outliers

*ITC 2002, Paper 24.1

*The Same Group Includes Transition Delay Faults Fmax



TDF vectors generated for Scan designs

TDF coupled with Min VDD for RVS search and feed forward for full vector testing

Determined VDD Min and TDF Fmax

Used NNR for outliers

*VTS 2003, Paper 1B.2

*Same Group Includes I_{DDQ} Extrapolation From Low V_{DD}

- Measures I_{DDQ} at nominal V_{DD}, then re-measures I_{DDQ} at low threshold (less than 2Vt taking precaution not change the logic states)
- Estimates the nominal I_{DDQ} leakage value from the equation,

  $\text{Log (Est Iddq}_{\text{Nom}}\text{)} = m \text{ Log (Iddq}_{\text{SubTh}}\text{)} + b$
- Rejects if the difference between the estimated and actual I_{DDQ} exceeds a threshold

*ITC 2003, Paper 22.3

In Case You Were Keeping Track

Year	Outliers Rejected
ITC 2000	Study the I_{DDQ} Neighborhood
ITC 2001	Validated NNR with 2 new ASICs
VTS 2002	Implemented SPP for NNR I_{DDQ}
ITC 2002	Added V_{DD} Minimum NNR
VTS 2003	Added Transition Delay Fault Fmax
ITC 2003	Sub-Threshold I_{DDQ} Estimate

LSI Logic is clearly the Leading Edge in Rejecting Outlier Die at Wafer Sort

Rejecting Outlier Wafers

Burn In experiment:

We selected wafers with less than 50% of expected yield

It took 6 months to complete 9 samples!

Compare results to ongoing Quality Monitor System:

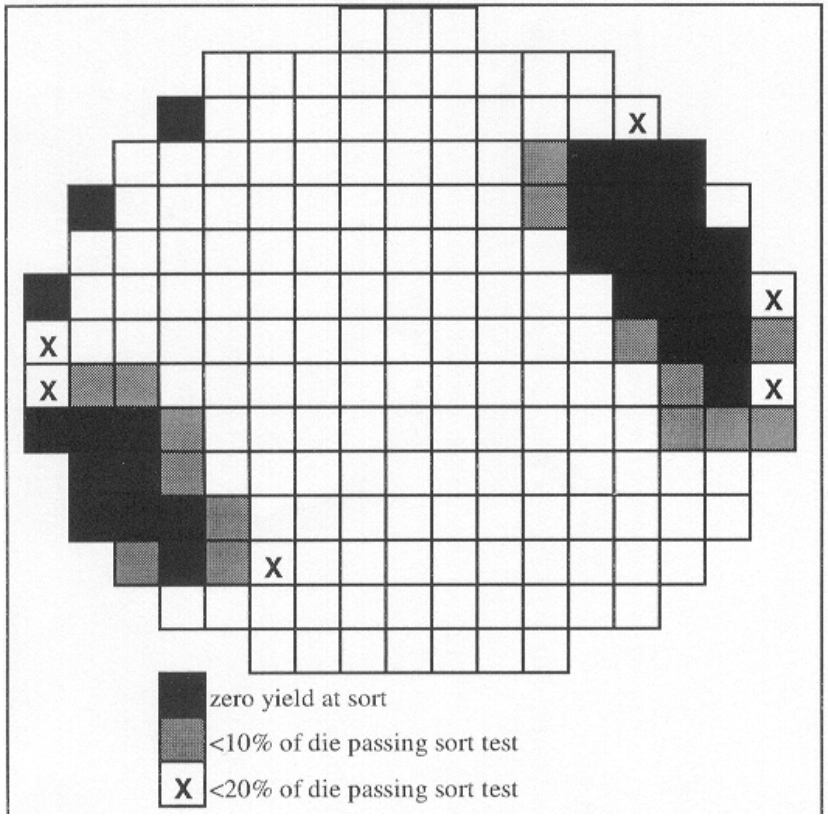
- **Over 200 lots were sampled**
- **1008 hour BI, 125^{O} C, 120% Vdd**
- **5,914 devices had zero failures!**

	QTY	FAILS
A	140	0
B	390	0
C	48	2
D	48	2
E	48	0
F	28	0
G	11	0
H	36	4
I	61	3

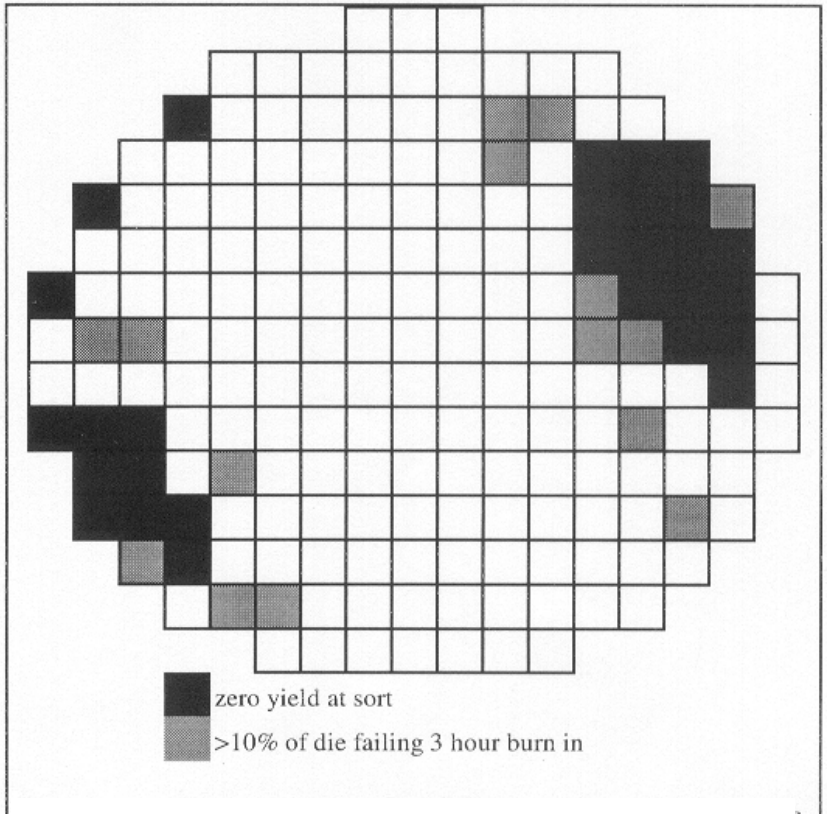
Vs.

13,580 PPM FR

“Good Die” in a Bad Neighborhood*



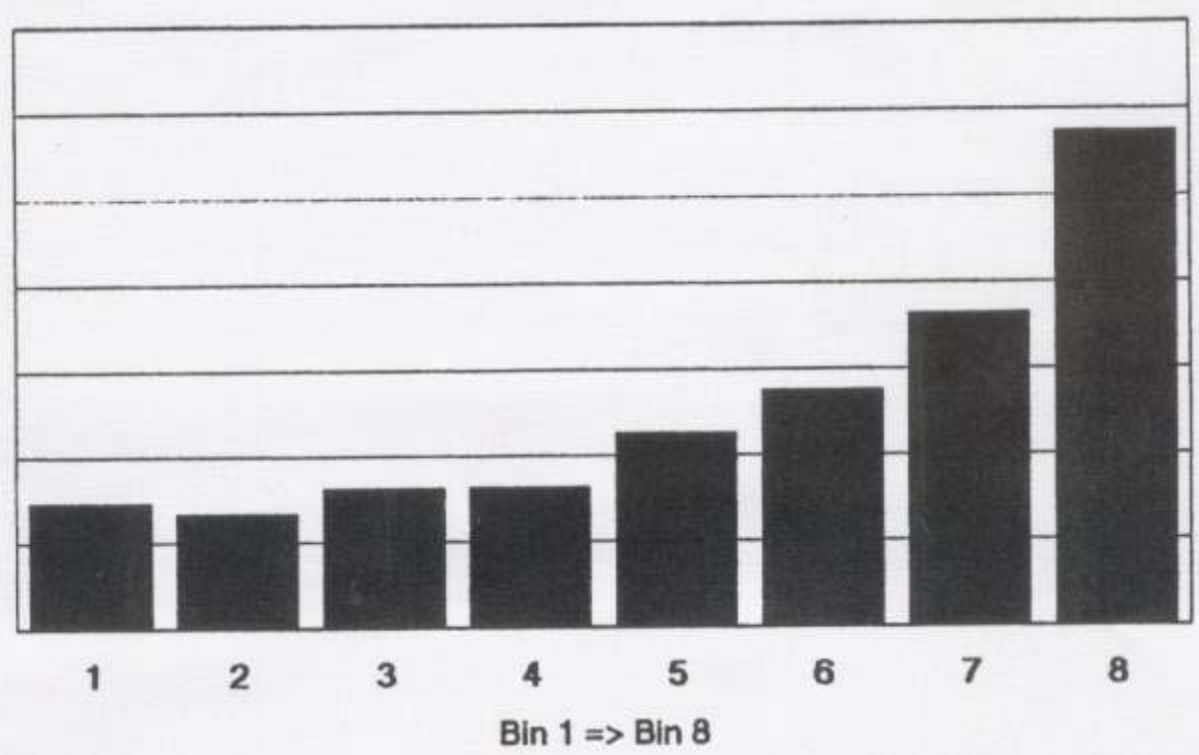
Probe map of zero and low yielding die locations



Map of low yielding locations after 3 hours of burn-in

*Intel, International Reliability and Physics Symposium, 1999

*IBM Burn In Failure Rate Vs. Neighborhood Yield at Probe



77,000 devices tracked thru BI

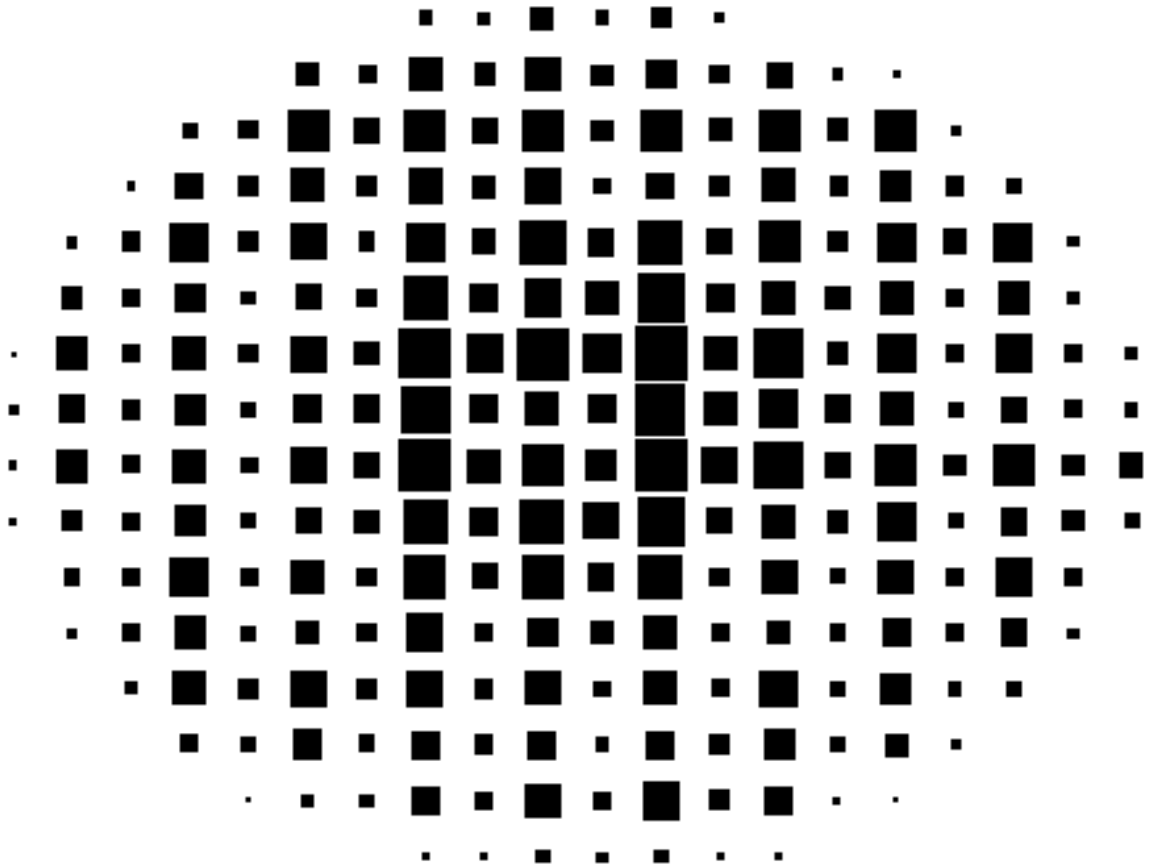
Over 3 X higher Failure Rate for devices with numerous bad neighbors

No "good die" rejection plan

Failure Rate Vs. the number of surrounding bad die

***VTS 2000 paper 23.3**

*Intel's Scrapped Unreliable Die



Die passing sort, but were rejected for reliability concerns (size of box is proportional to % rejected)

*International Test Conference 2001, Paper 40.3

Reliability Screening at Probe Voltage Stress Testing

- Voltage stress followed by test
- Interesting experiment on .18 micron chip
- Early Failure Rate was 2000 - 3000 PPM
- Five lots, 112 wafers, were split three ways
- Stress levels up to 1.6 x V_{DD} for 1 sec
- Two splits evaluated stress temperature
- Last split demonstrated final test flow
- Stress replaced 100% production Burn-In!

Voltage Stress Experiment