Microprocessor Probing Challenges:
Scaling Sort Cost with Moore's Law

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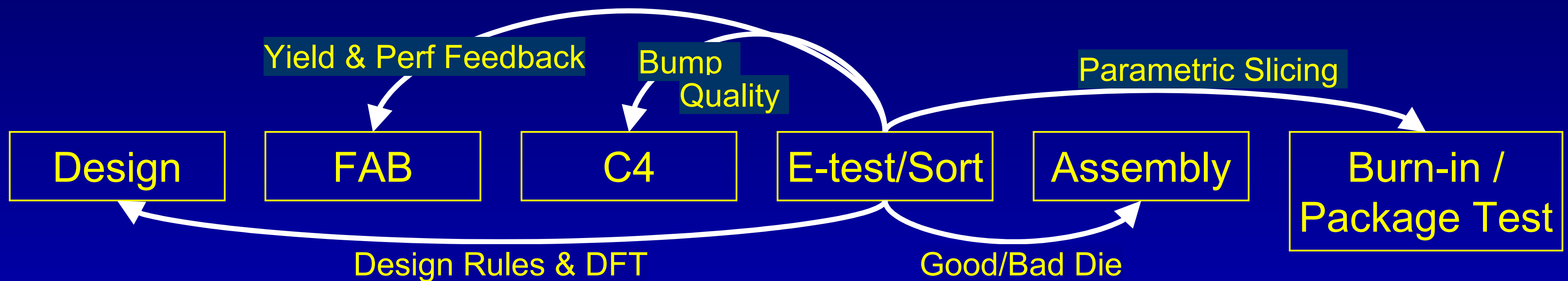
Outline

- ✓ Performance Impact at Wafer Sort
- ✓ Performance Requirement Trend
- ✓ Cost Trend
- ✓ Performance Sort
  - ➢ Disruptive Technology for Meeting Goals
- ✓ Value Sort
  - ➢ Cost Reduction with Lowered Performance
- ✓ Key Messages

Sort Purpose

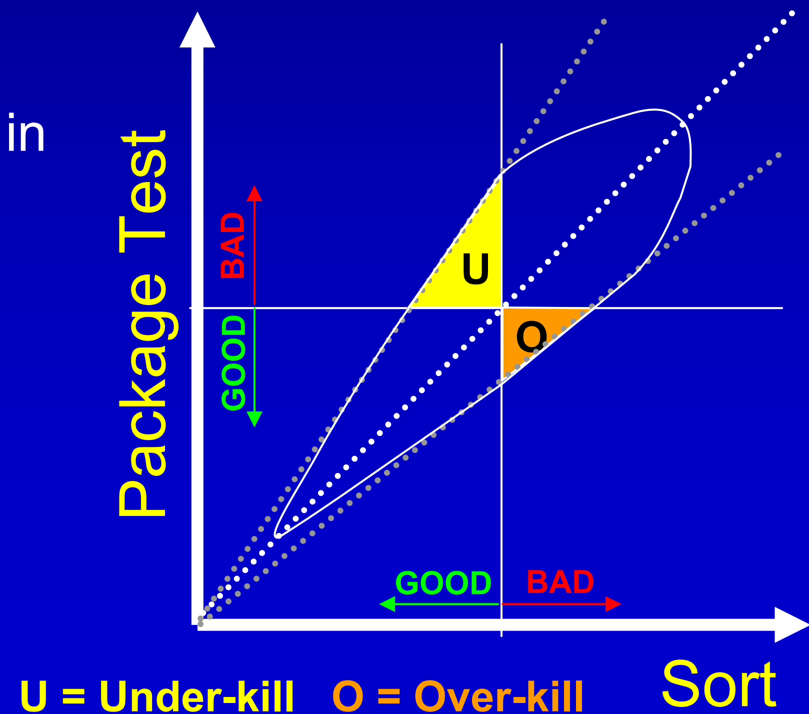
- Sort data feeds into entire manufacturing flow
  - ✓ It's Integral upstream & downstream



- Data Feedback
  - ✓ Provides key Yield/Parametric data to Fab/C4
  - ✓ Design Debug/Marginalities
- Data Feed-forward: Optimize back-end test operations
  - ✓ Screen Bad Dies → Save packaging costs
  - ✓ Parametric Slicing

Performance Impact

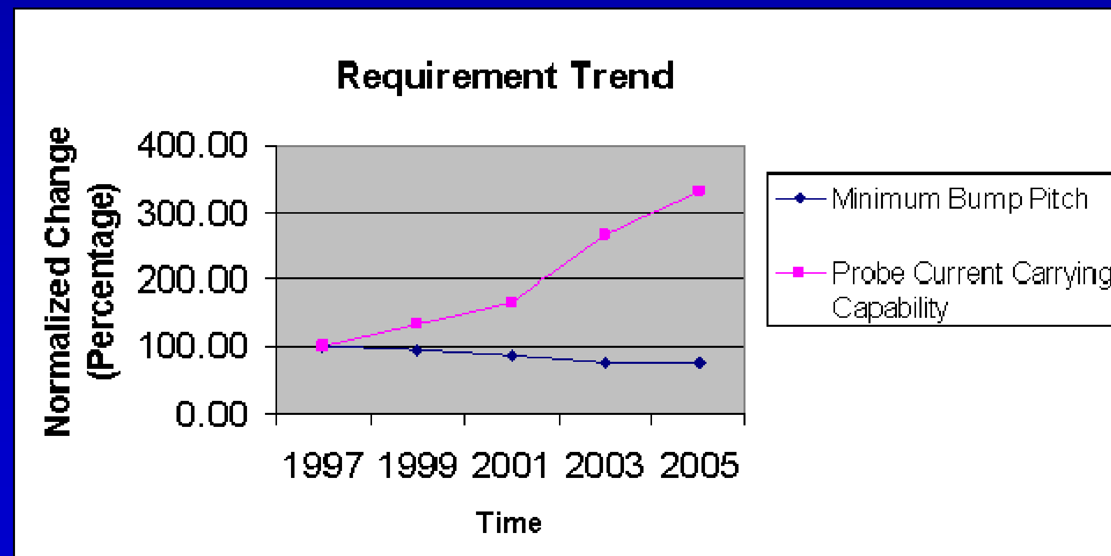
- There is always a concern regarding correlation between sort and down stream test results
  - ✓ Correlation → Equivalent results at both testing steps
  - ✓ Over-kill → Die failed at sort and passed at package test
  - ✓ Under-kill → Die passed at sort and failed at package test
- Example
  - ✓ Sort test may require large power in short bursts
  - ✓ Sort result lower than true performance
  - ✓ A Root cause → Electrical imperfection of tooling



Requirements Trend

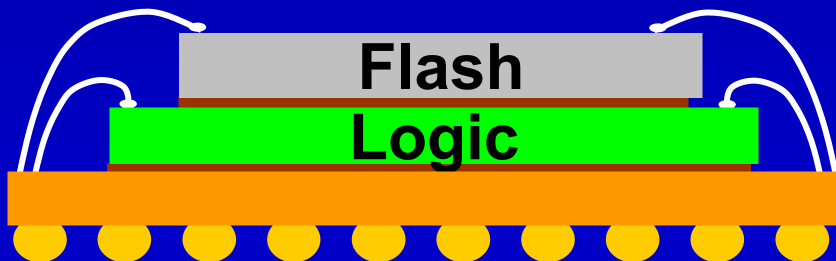
- Conflicting Product requirements
  - ✓ Pitch reduction vs. current carrying capability
    - ➢ 5-10% per generation pitch size reduction
    - ➢ 30-40% per generation current per contact historically (15-25% post Right Hand Turn)
  - ✓ True for many other competing attributes
    - ➢ Low K ILD protection vs. lead free material probing
    - ➢ Power delivery enhancement vs. probing cost

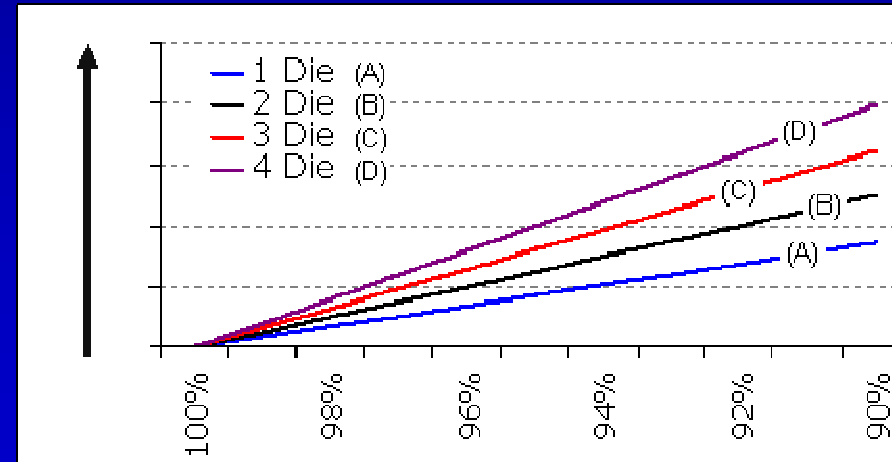
Key message: Keeping pace by evolutionary change will not be easy



Requirement Trend

- Multi-chip Package (MCP)
  - ✓ Cost reduction, size compaction & performance increase
- Compounded yield loss results in high scrap cost
- Known good die (KGD) testing required to lower the scrap cost

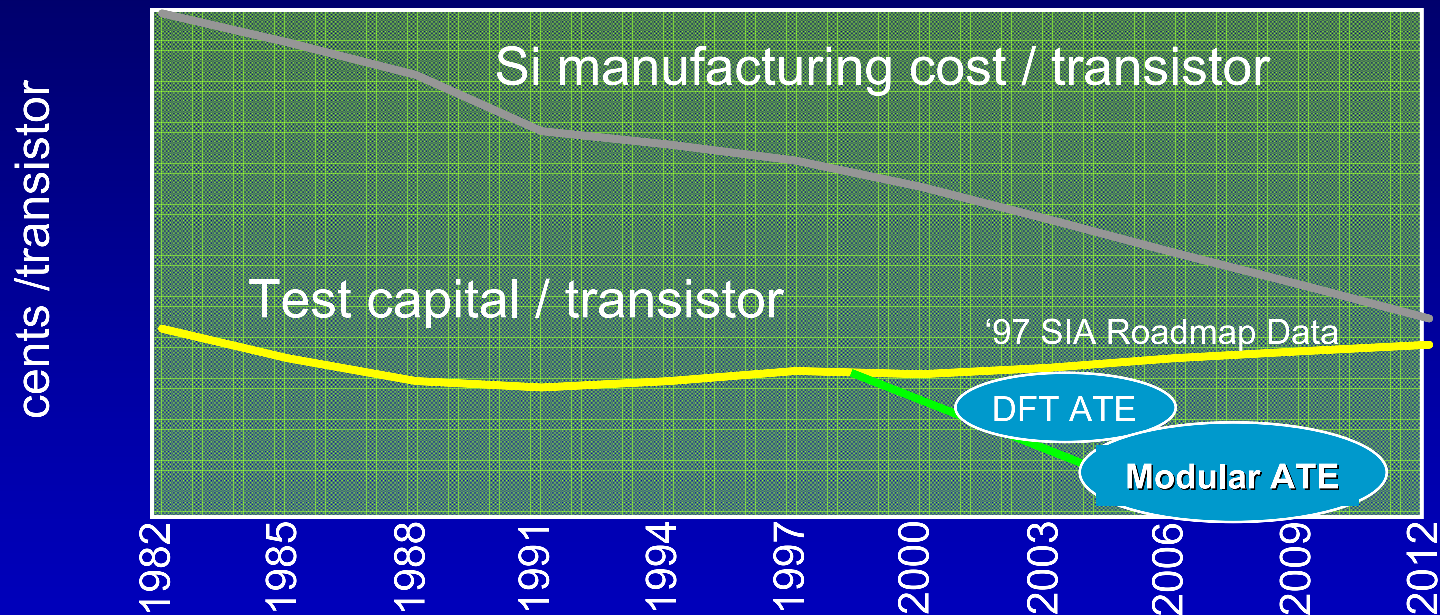




Tester Cost Per Transistor is Declining

Tool cost is trending down

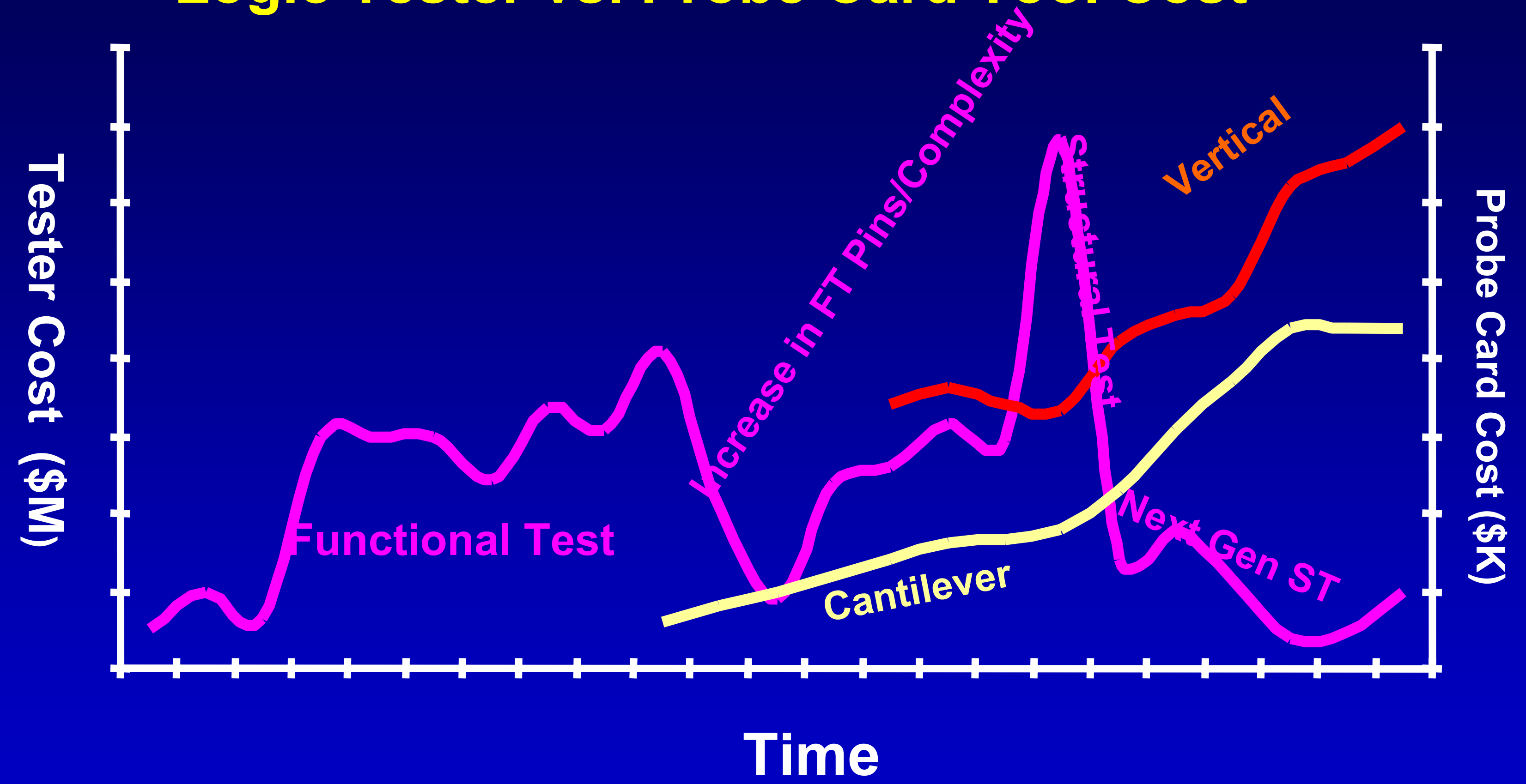
Cost Reduction Roadmap: Functional → DFT → Modular



- **DFT & Structural Test reduce equipment cost & complexity**
  - ✓ **Reduced I/O data rate and accuracy requirements**
  - ✓ **Reduced tester channel count**
  - ✓ **Reduced resource flexibility requirements**

Tooling Cost is Increasing

Logic Tester vs. Probe Card Tool Cost

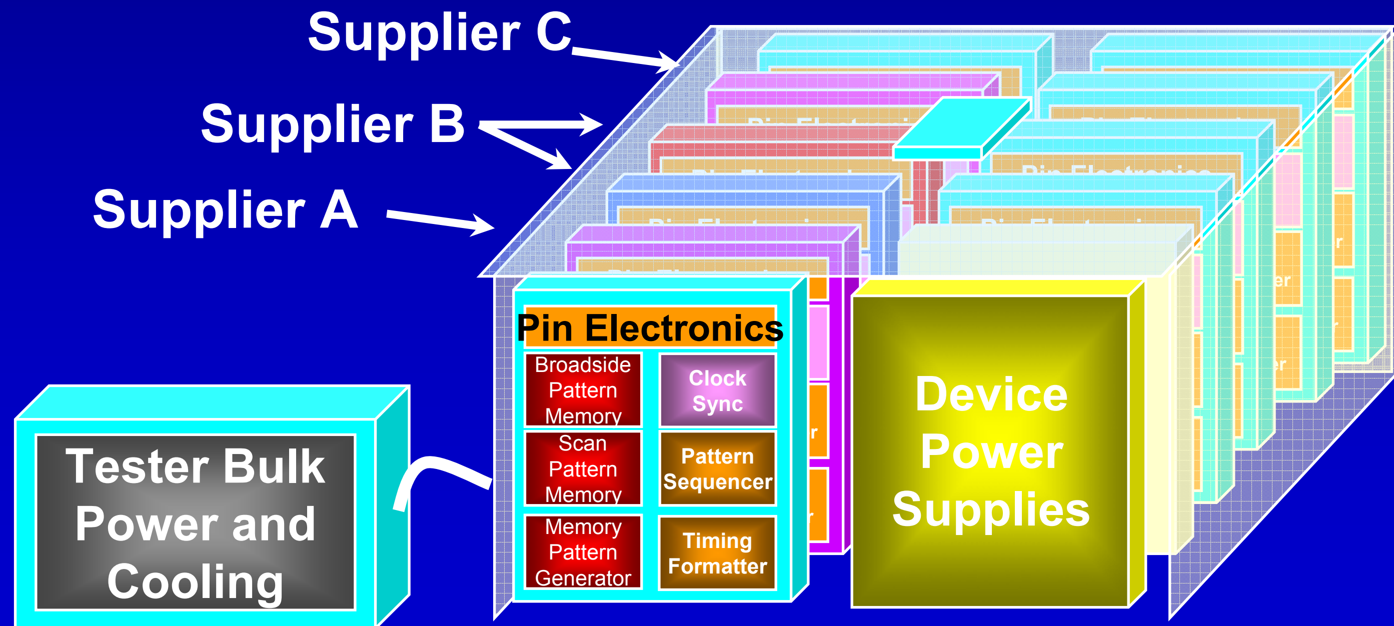


Disruptive technology innovation is needed to “right hand turn tooling cost

Source: Intel and Dataquest

CMT* – Disruptive Test option

- Modular open architecture
  - ✓ Multiple suppliers using industry standards
  - ✓ Reusable base platform
    - ➢ new capabilities with incremental modules
  - ✓ Standard OS and equipment interface software
  - ✓ Scalable

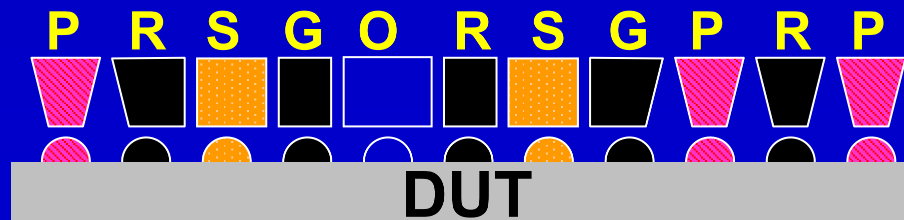


* Configurable Module Tester

Thinking inside the probecard

- If technical expectations continue their pace, one exotic solution may be interconnect customization
  - ✓ Build custom probes for each type of contact
    - Power probe for maximum power for power contact
    - Signal probe for maximum SI for I/O contact
    - Optical "probe" for optical interconnect

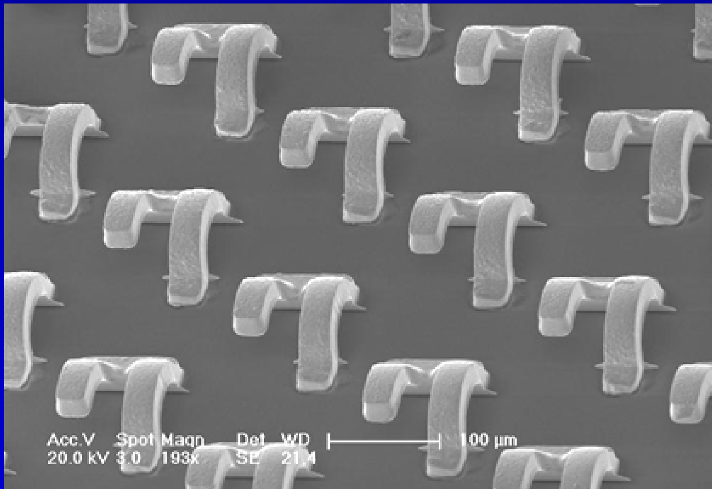
When	Relative Needs	Contact answer
Was	Low Power / Low Speed	Just connect it
IS	High Power / Low Speed	Optimize for power
Next	High Power / High Speed	Optimize for both power & data
?	Power , Speed and optical	?

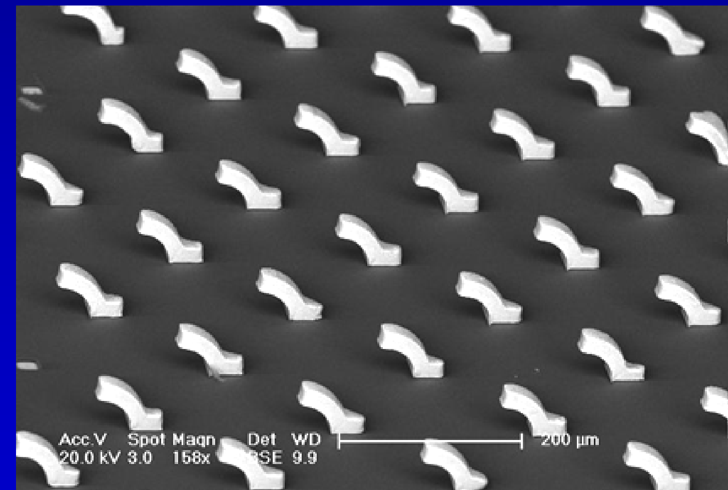


If the DUT requires power, signal and optical interconnect to DUT, will your technology work?

Thinking inside the probecard

- Litho (batch based) technology
  - ➢ Lower Cost
  - ➢ Better Pitch capability
  - ➢ Lower parasitic
  - ➢ Insensitive to # of Probes





Changing technical landscape

Green = introduced

Item	Date	Solution — time —→			Key SIU metrics	
Periphery pad	1960s – today	WB	Litho	Vertical	Pad size Pad pitch	# of rows # of DUT
C4 interconnect	1980 – today	Vertical	Pogo	MEMS/ V.Litho	Cres Current carrying	Pitch
Lead free	2000 – today	MEMS/ V. Litho	Vertical			
Optical	> Today	TBD; are you ready?			Bandwidth Intensity	? ?

Key message: interfaces technologies don't die. Market segment per style decreases with time.

Value Sort Pros/Cons

- ✓ Value Sort Definition
  - ➢ Reduced content
  - ➢ Reduced speed
  - ➢ Reduced parametric test accuracy
- ✓ Pros:
  - ➢ Lower sort unit cost through tool/tooling/TT reduction
  - ➢ Less challenge PF/Dev engineering efforts
- ✓ Cons:
  - ➢ Overall higher (after Fab) back end cost by the consequential underkill
  - ➢ Resultant overkill at sort – Time to market

Summary

✓Key message 1: Drive disruptive solutions innovation/development that reduce cost and sustain performance

- Performance Sort

✓Key message 2: Value sort is not our preferable solution, but a cost reduction option if performance sort encounters showstopper and/or invokes too high cost.