Optimizing Test Strategies for Multi-DUT Wafer Probing

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Abstract

- The demand for reducing test costs is causing a rapid adoption of on-wafer Multi DUT test strategies for Advanced Logic IC applications such as personal communications, automotive controllers, and other embedded processors. This paper shows several examples of the unique requirements and design-for-test opportunities presented by these highly integrated devices. Decision guidelines are presented for determining the appropriate number of die to test in parallel, selection of optimal stepping patterns, meeting signal integrity and power delivery requirements, and minimizing bond pad damage over low-K dielectrics and pad-over-active device applications. This includes recommendations for bond pad layout rules, passive RF structures, high current applications and elevated temperature test. We will follow the total solution design process for an 8 DUT embedded controller application as an example of this new industry trend. Engineering decisions include selection of bond pad locations to avoid "corner crowding", power distribution networks and voltage sensing to avoid voltage droop, and the tradeoff between a 1 x 8 array vs a 2 x 4 array for routing capability vs thermal expansion at 125 C.

Outline

- Market trend
- Unique requirements for Multi-DUT cards
- Design methodology / process flow
- Decision guidelines for determining Multi-DUT test architecture
- Total solution design example
- Summary

Multi-DUT Market Trends

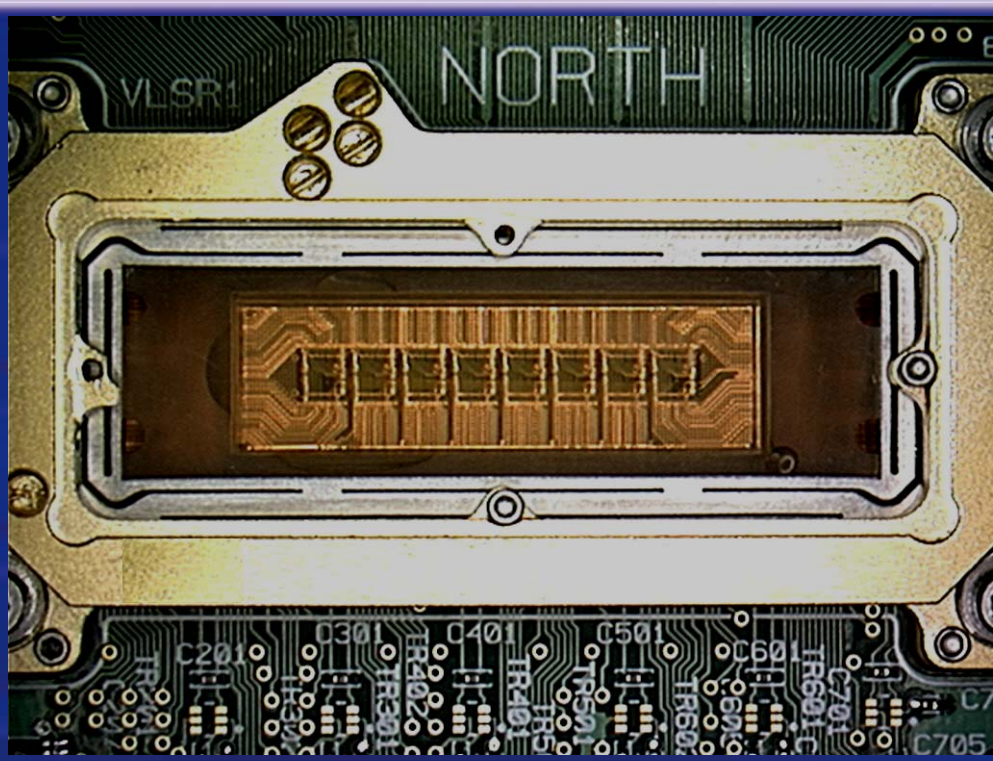
- Rapid adoption of on-wafer Multi DUT test strategies for logic IC applications to reduce cost of test
- Depending on tester overhead, indexing speed and other factors, test cost can be reduced by 50-90%
- Logic, mixed signal and SOC design life, tester costs, and test times create a different economic model from RAM test
- Our Multi-DUT product mix > 50% in 2004
  - Personal communications
  - Automotive controllers
  - Embedded processors

Why Multi-DUT? (the real reason..)

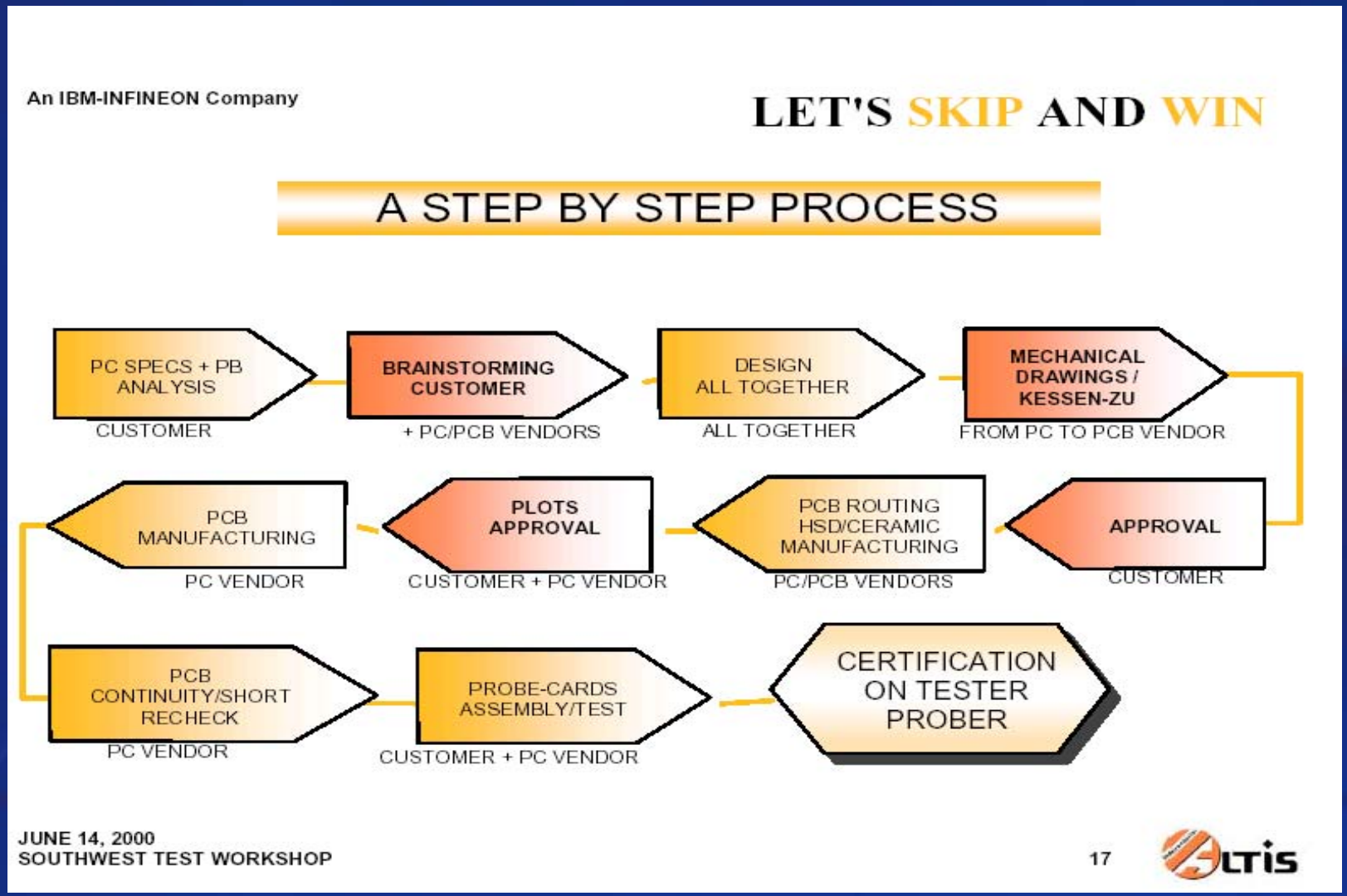
- So you can go “Flying by” your competition ☺
- Photo courtesy Sailinganarchy.com

Unique Requirements for Multi-DUT Probe Cards

- Routing density
- I/O count
- Dimensional accuracy
- Planarity
- Elevated temperature (expansion, Cres)
- Known Good Die: Final test at wafer (at speed test)
- Functions / components on load boards and cards



Multi-DUT Design Flow (Altis, 2000)



Design Process Flow (1)

MultiDUT Probe Card Decision Matrix

Typical Flow

- POAA
- Bond Pad Layout
- Corner Pads

Design Process Flow (2)

IC Design → **Test engineering** → **Test Floor**

- POAA
- Bond Pad Layout
- Corner Pads

- Tester Resources
- Test Temperatures
- Keep out area
- At Speed Test issues
- Loopback
- Customer Preferred Pattern
- Critical Signals
- Power Supplies
- MultiDUT Pattern
  - Layout Study
  - Pad Size
  - Die Size
  - Probe area

Design Process Flow (3)

IC Design → **Test engineering** → **Test Floor**

- POAA
- Bond Pad Layout
- Corner Pads

- Tester Resources
- Test Temperatures
- Keep out area
- At Speed Test issues
- Loopback
- Customer Preferred Pattern
- Critical Signals
- Power Supplies
- MultiDUT Pattern
  - Layout Study
  - Pad Size
  - Die Size
  - Probe area

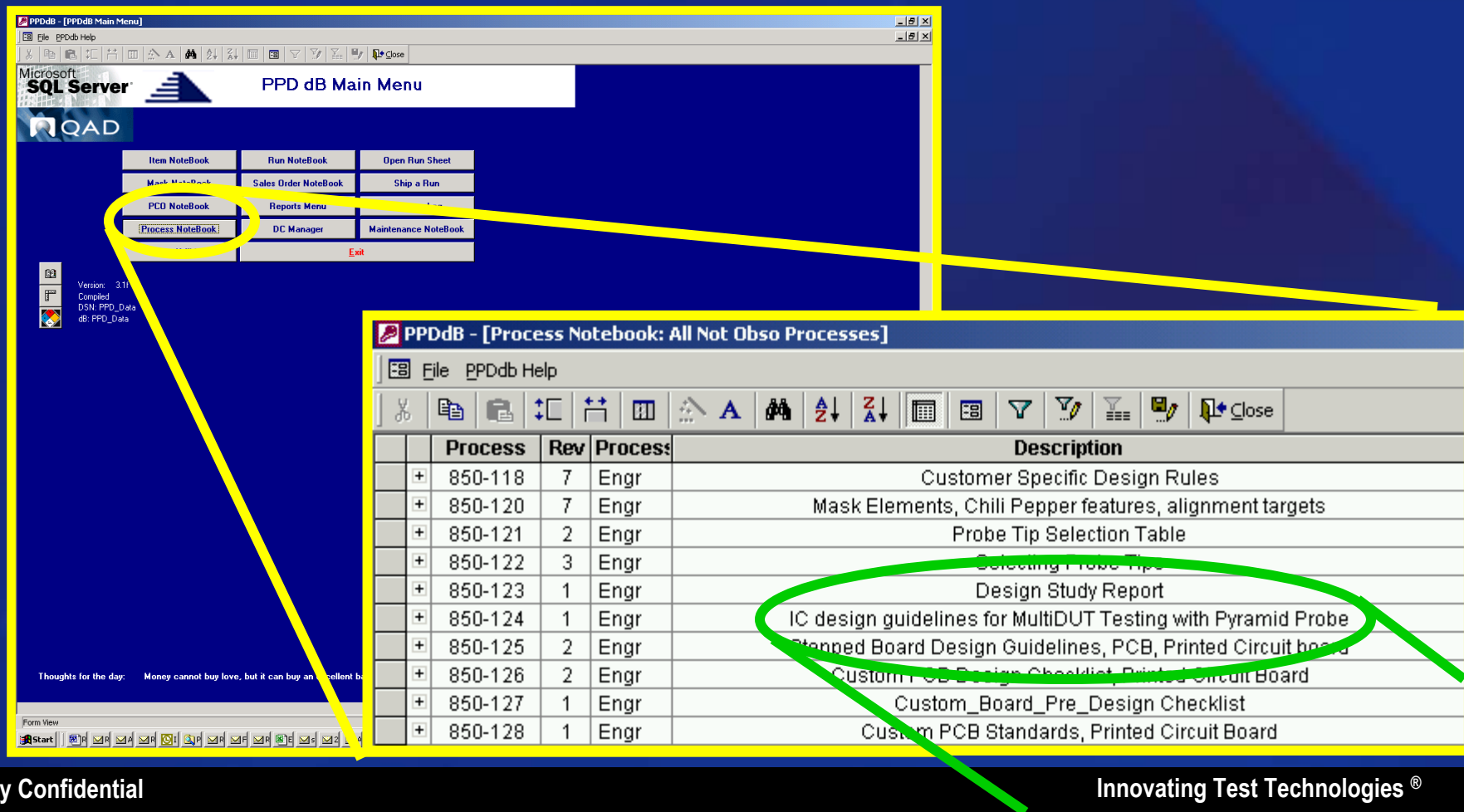
- Service
- Inventory
- Training
- Cleaning

Probe Card Design Guidelines

- Appropriate number of die to test in parallel
- Selection of optimal stepping patterns
- Meeting signal integrity and power delivery requirements
- Minimizing bond pad damage over low-K dielectrics and pad-over-active device applications.
- Bond pad layout rules
- Passive RF components
- High current applications
- Elevated temperature test

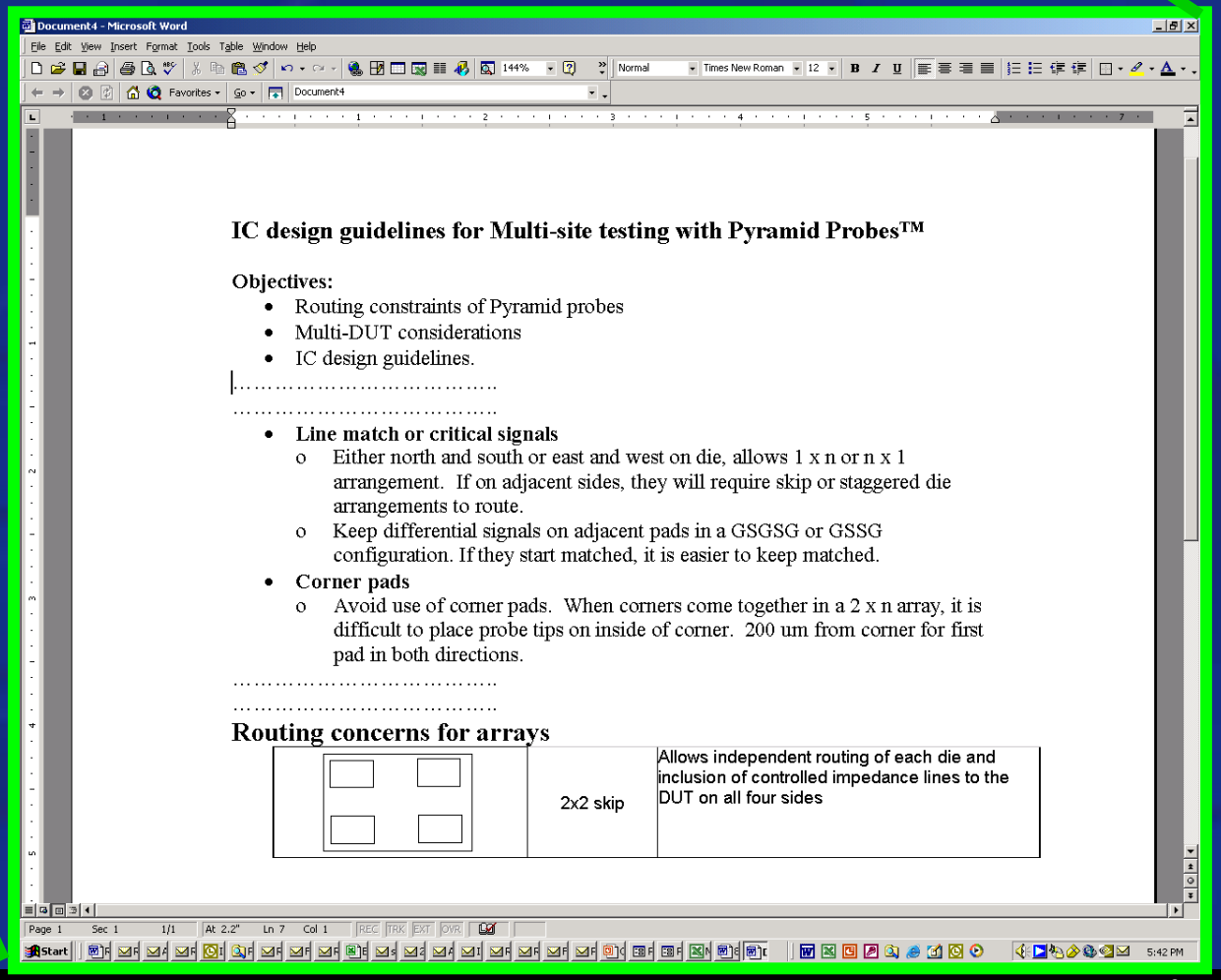
Detailed And Rigorous Design Rules

- Increasingly complicated process requires disciplined documentation and rev control to capture learning



"IC design guidelines for Multi-site testing…"

- Line matching
- Differential signals
- Corner pad spacing
- Routing concerns for arrays



Document4 - Microsoft Word

IC design guidelines for Multi-site testing with Pyramid Probes™

Objectives:

- Routing constraints of Pyramid probes
- Multi-DUT considerations
- IC design guidelines.

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- **Line match or critical signals**
  - Either north and south or east and west on die, allows 1 x n or n x 1 arrangement. If on adjacent sides, they will require skip or staggered die arrangements to route.
  - Keep differential signals on adjacent pads in a GSGSG or GSSG configuration. If they start matched, it is easier to keep matched.
- **Corner pads**
  - Avoid use of corner pads. When corners come together in a 2 x n array, it is difficult to place probe tips on inside of corner. 200 um from corner for first pad in both directions.

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Routing concerns for arrays

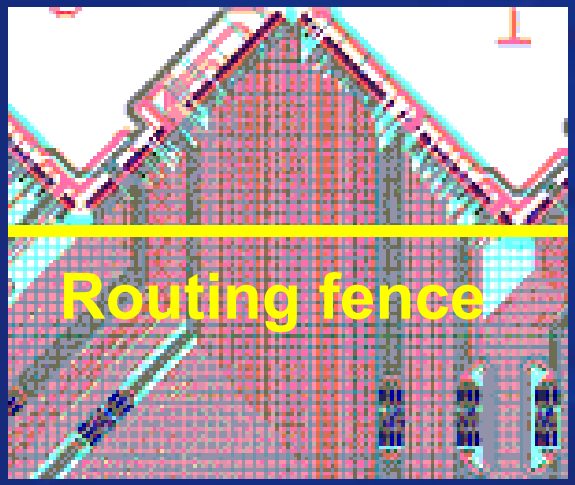
	2x2 skip	Allows independent routing of each die and inclusion of controlled impedance lines to the DUT on all four sides

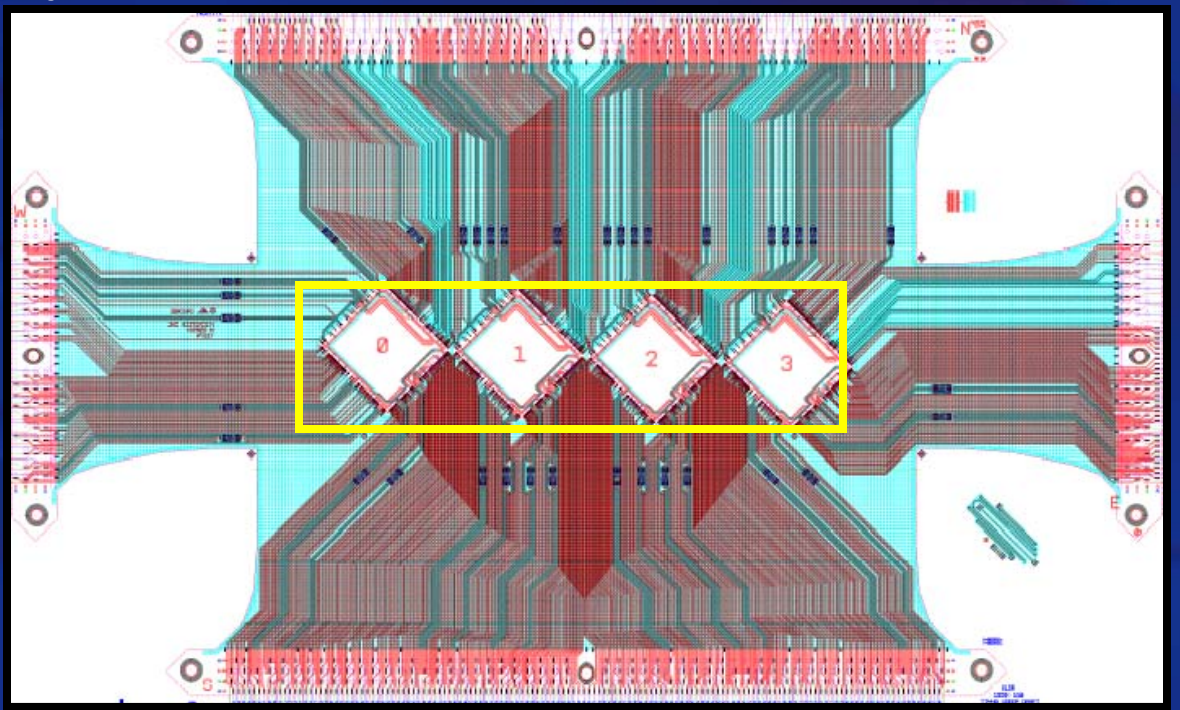
Multi-DUT Pattern Selection Process

1. Routing study
2. Probe area vs pad size
3. Wafer map efficiency
4. Critical signal routing / component placement

1. Routing Study: Parameters

- Focus on high density areas
- 60 um pitch pads = 42 um trace pitch at 45 degree angle
- Power lines wider for current handling
- “Routing fence efficiency” ~ 70% of theoretical best



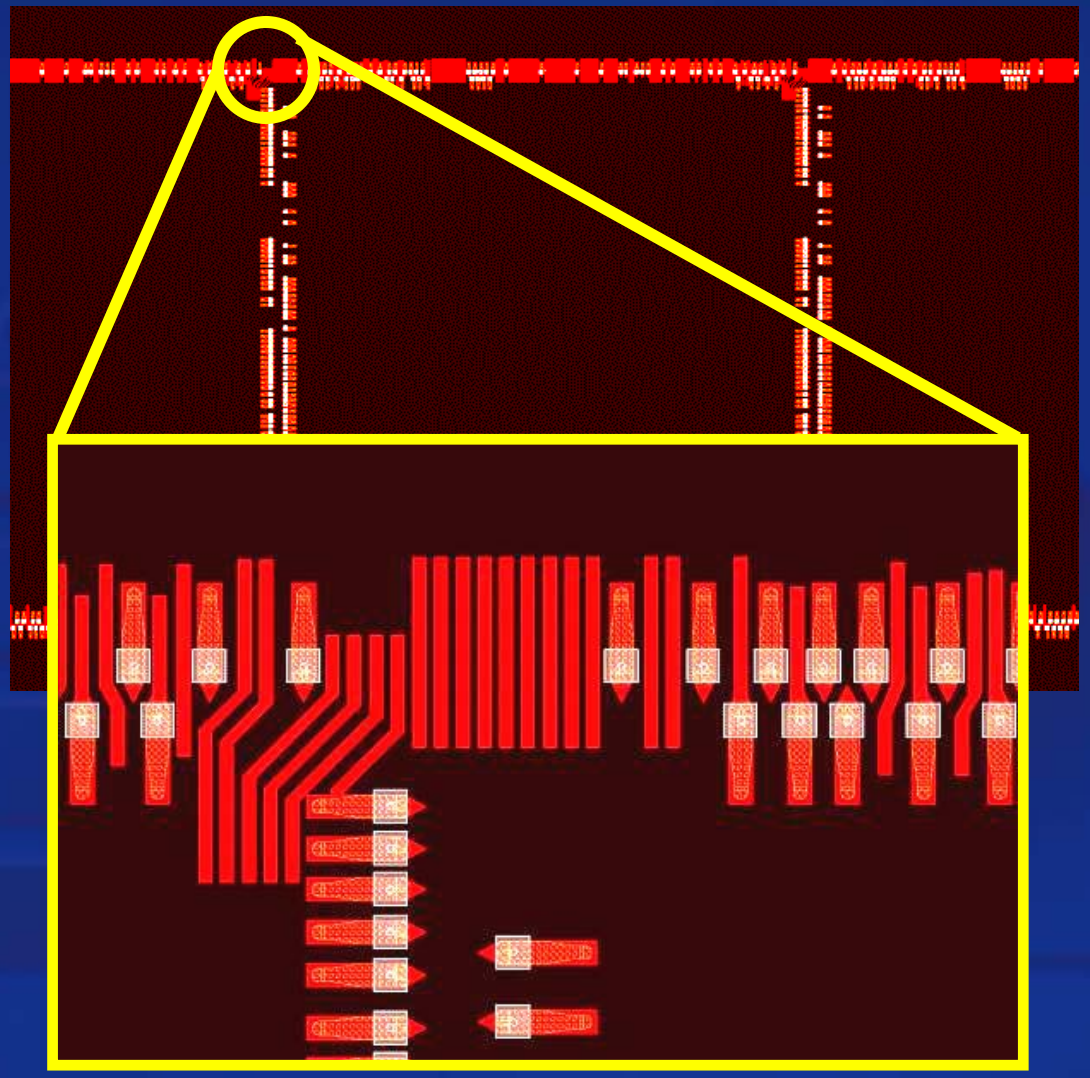


1. Routing Study Example

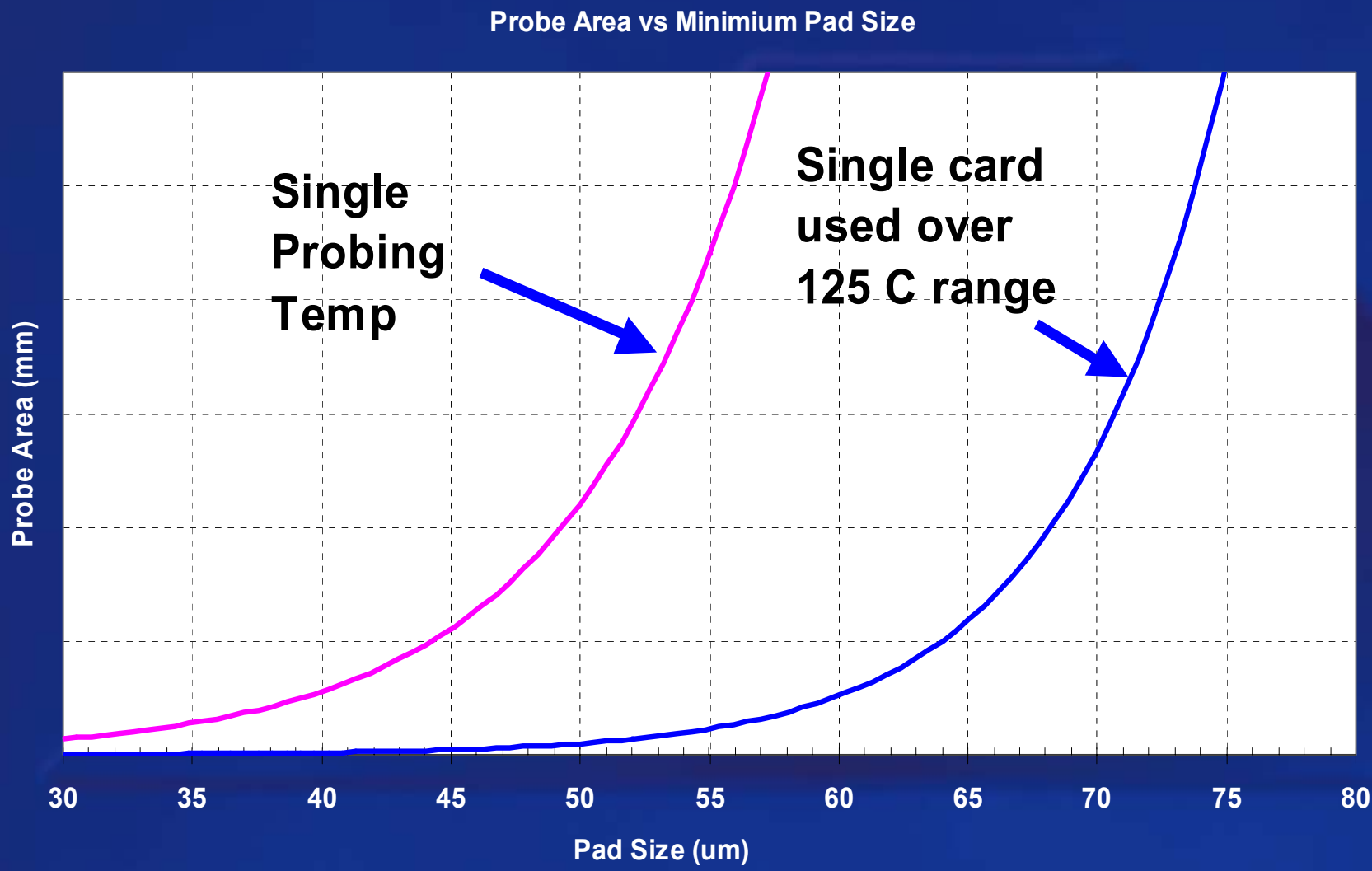
Die Size:	~5900um
Multi-DUT layout:	2x4 (pref)
How Many Power Supplies?	6
Can Power Supplies be grouped?	Yes
Distance between furthest probes	23374

Number of each Line Type:	
Powers =	48
AC =	0
DC =	608
GND's =	72
RF =	0

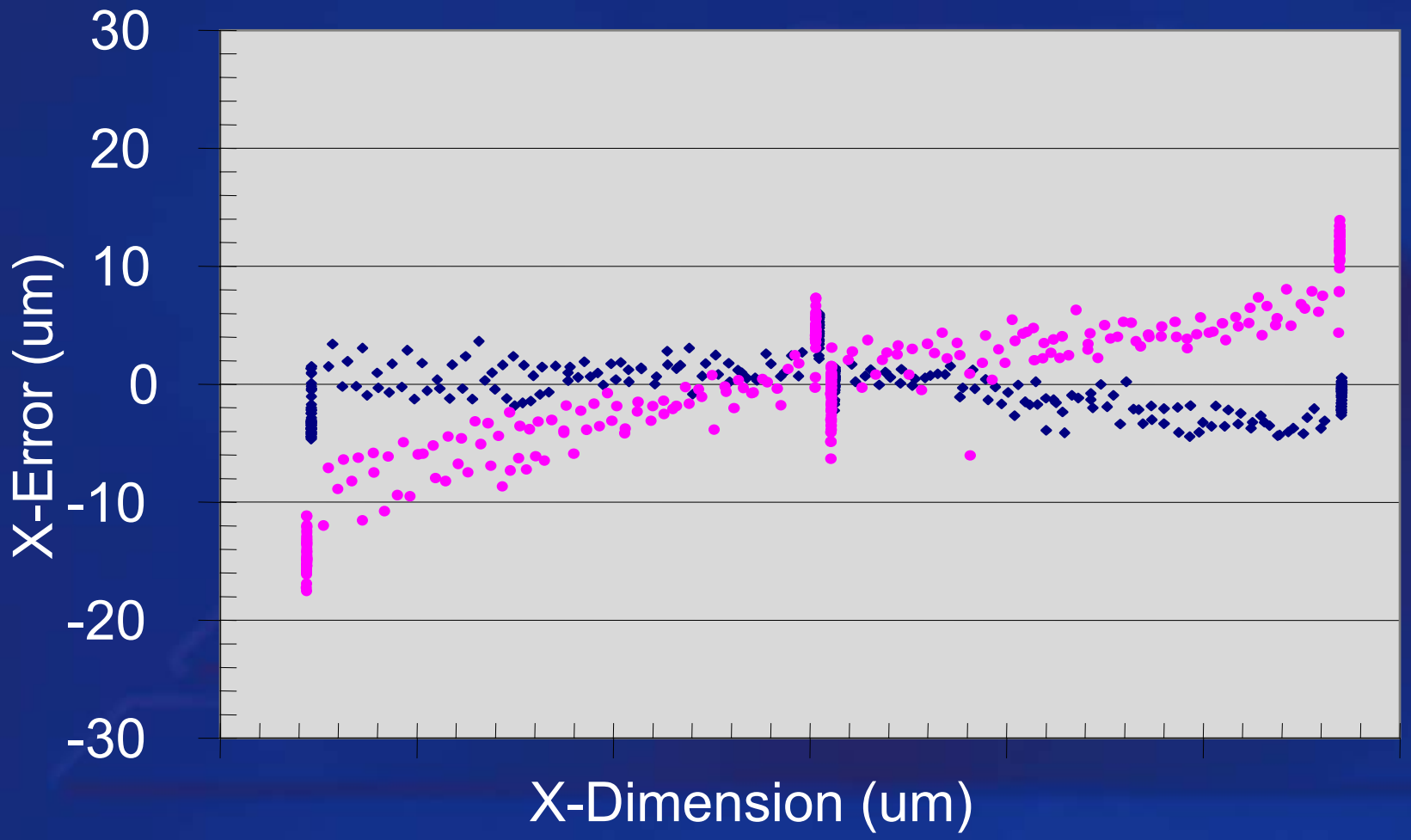
Total No. of Probes	808
Total Sense Lines	48
Total IO Required	704



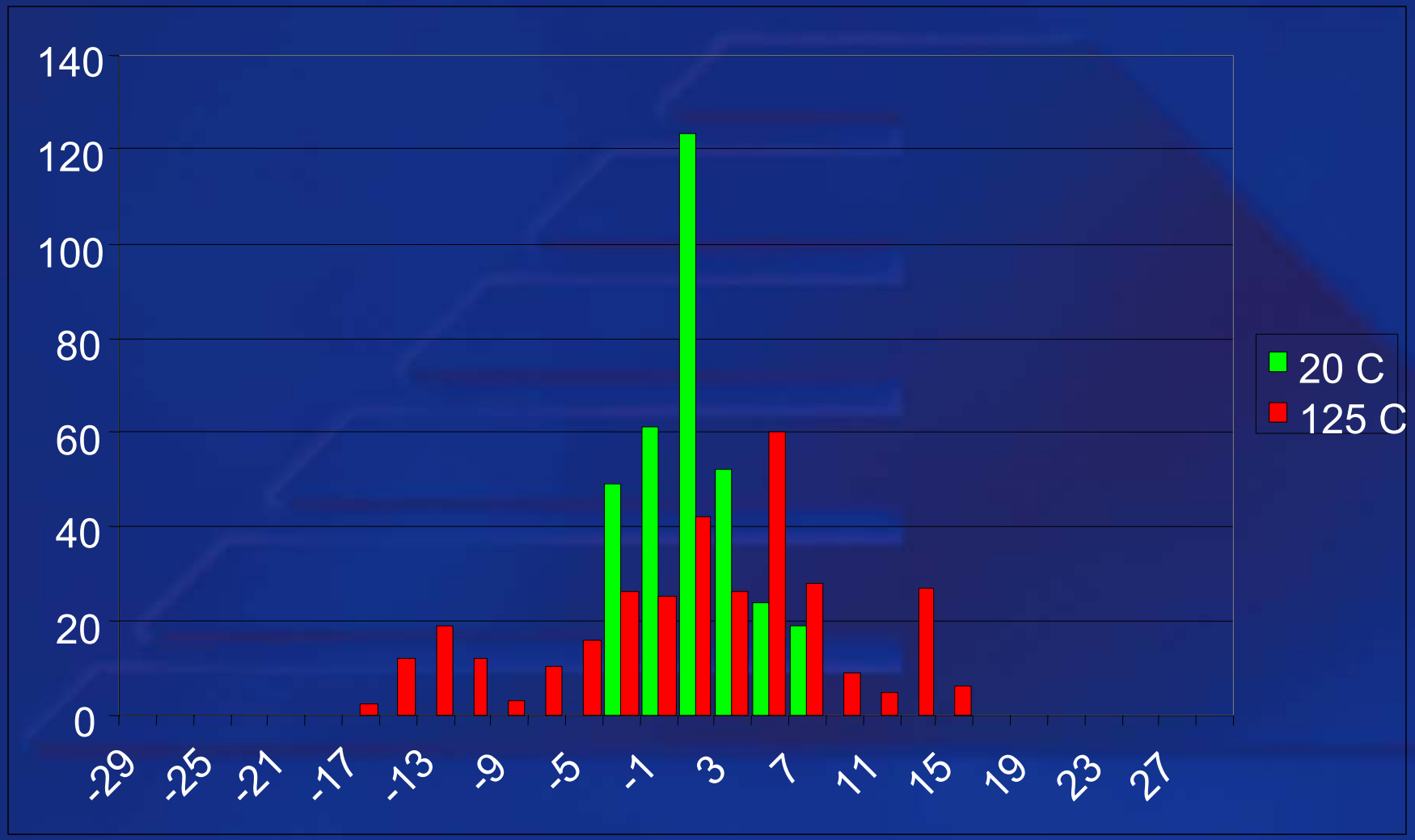
2. Probe Area vs. Pad Size & Temp Range



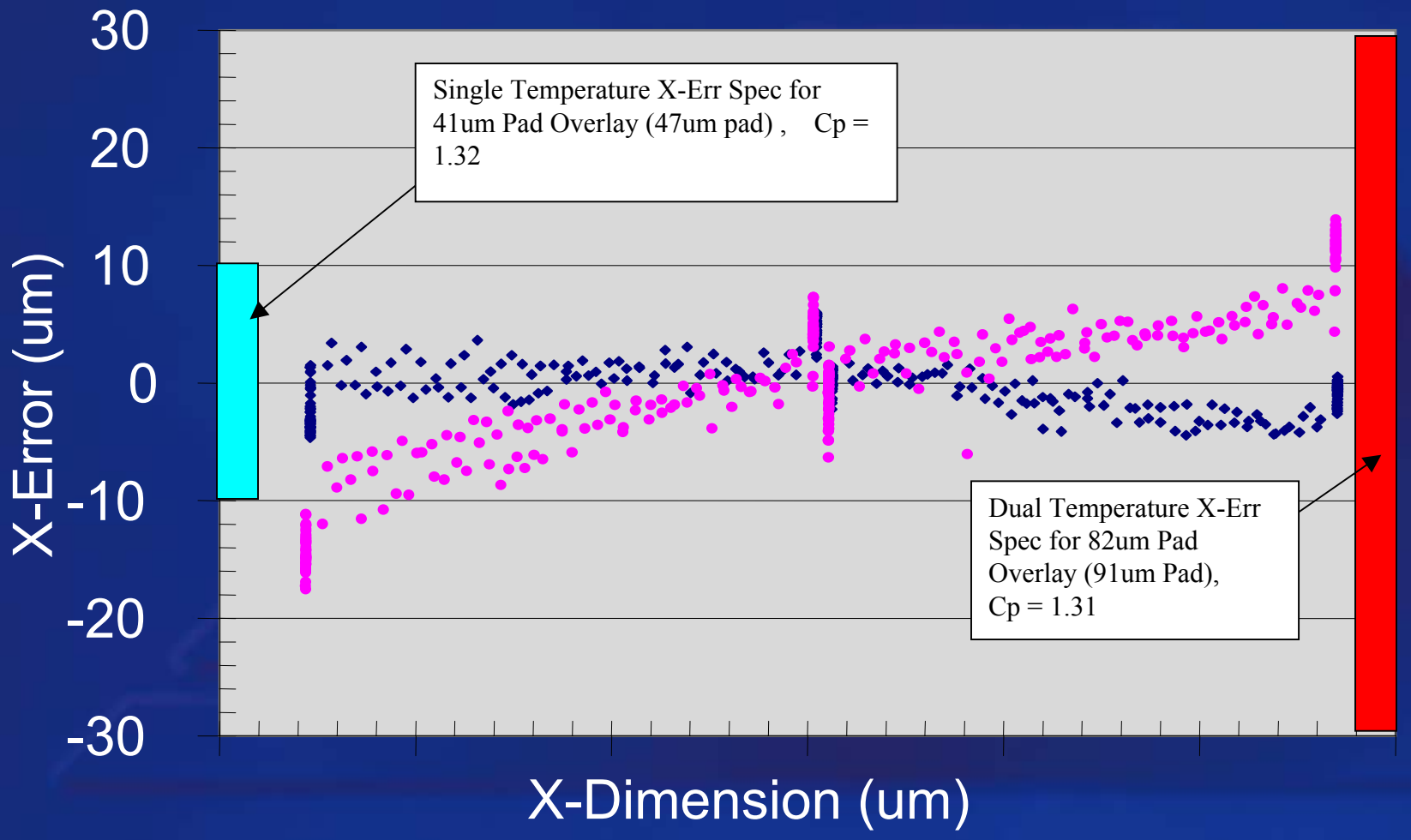
2. Probe Positions at 20 C & 125 C



Probe Position Change at Elevated Temperature (distribution)

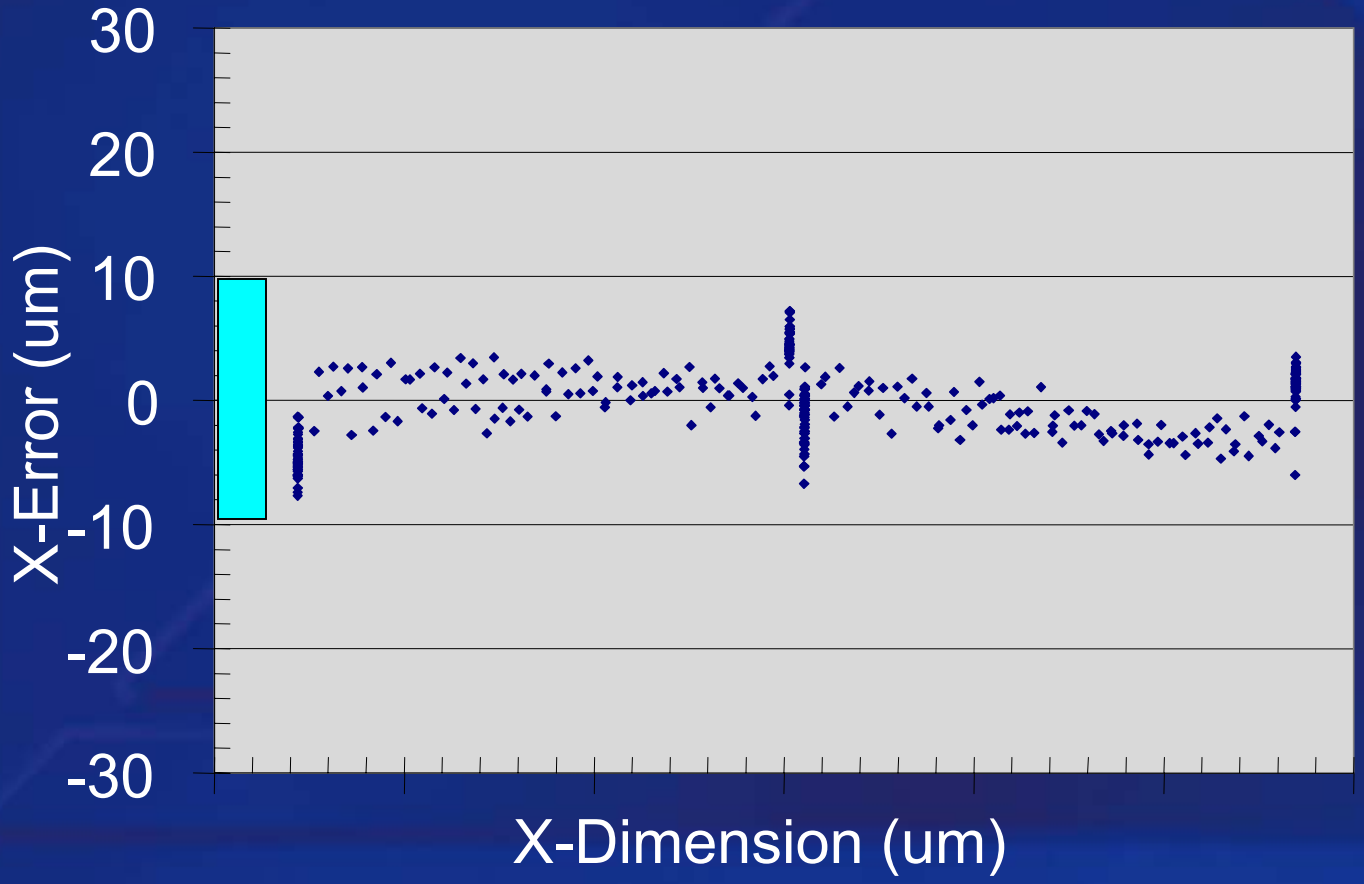


Probe Position Change at Elevated Temperature (Cp)

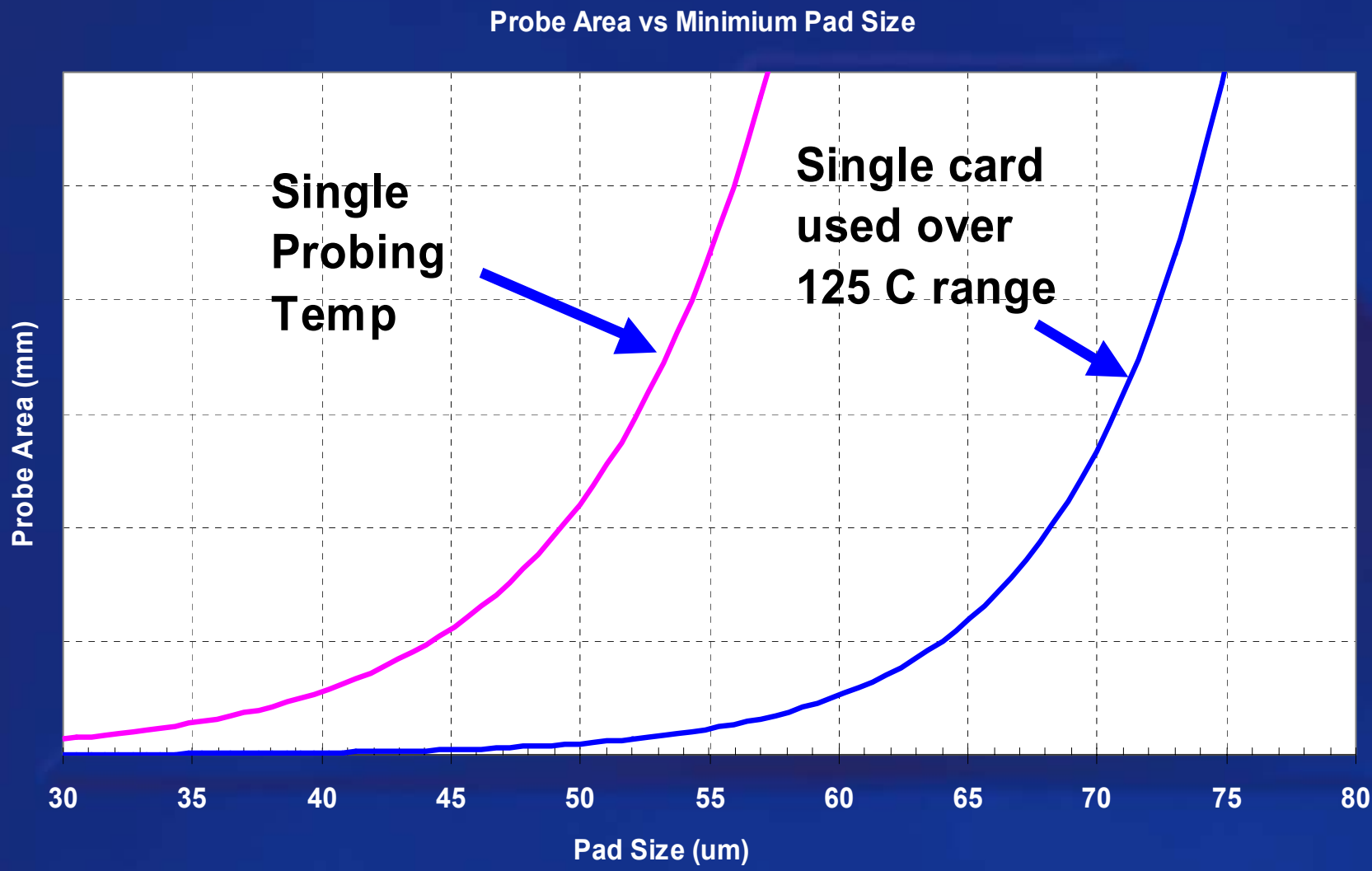


Probe Position Compensated for Elevated Temperature

- Cp = 1.3 for 47 um pads at 125 C only (dedicated core)

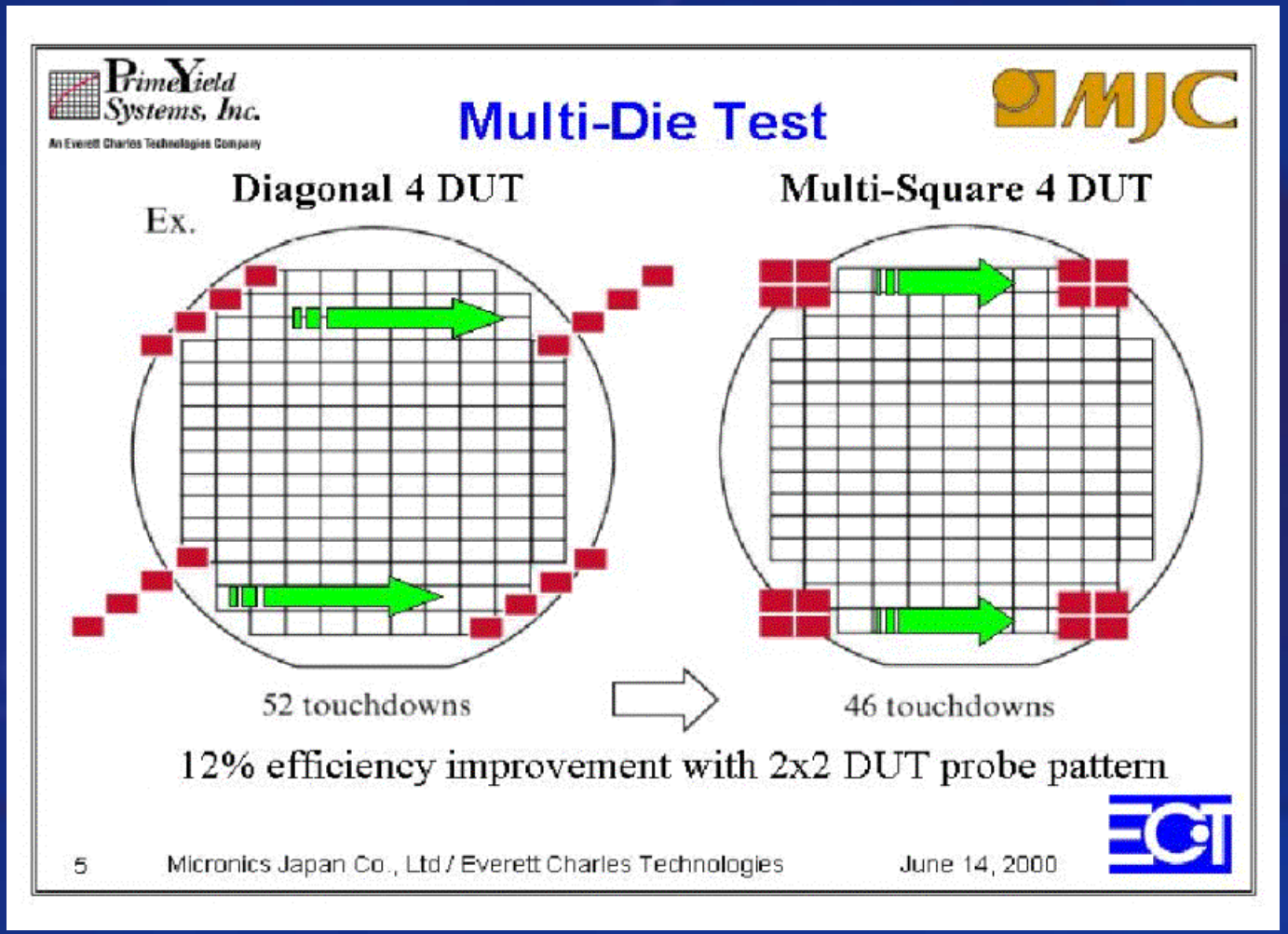


2. Probe Area vs. Pad Size & Temp Range



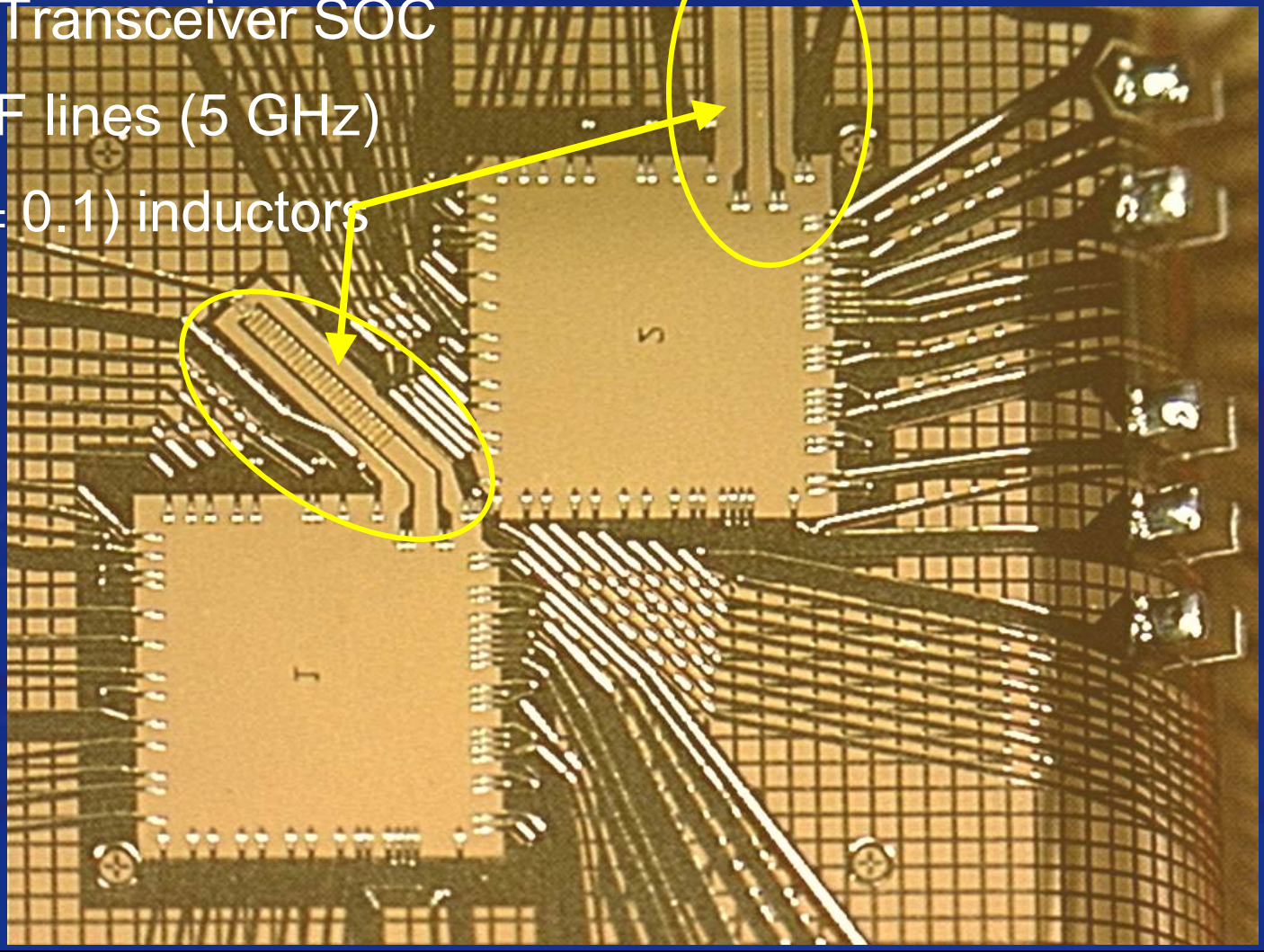
3. Wafer Map Efficiency

- MJC SWTW 2003 showed diagonal vs square efficiency



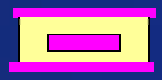
4. Critical RF Line / Component Placement

- Bluetooth Transceiver SOC
- Multiple RF lines (5 GHz)
- 1.95 nH (± 0.1) inductors



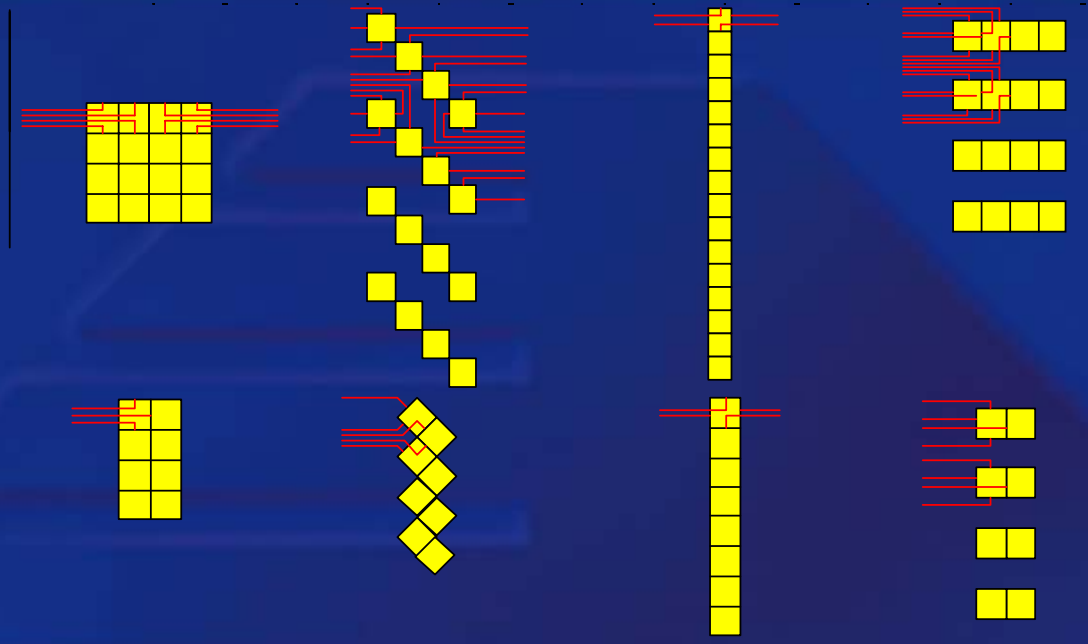
4. Critical Signals (Delay Matching)

- Delay depends on dielectric constant and architecture
- Systematic processes for delay matching are required

	Architecture	Polyimide Dielectric Constant = 3.5 (mm / ns)	Delay for 300 mm route (ns)	Alumina Dielectric Constant = 10 (mm / ns)	Delay for 300 mm route (ns)
	Stripline	160	1.9	95	3.2
	Microstrip (buried)	167	1.8	99	3.0
	Microstrip	175	1.7	104	2.9
	Coplanar waveguide	196	1.5	125	2.4
	Range (min:max)	82%	0.3	76%	0.8

DUT Pattern Selection Criteria

(1 = most capable, 4 = least capable)



	16 X Patterns			
	8 X Patterns			
Probe area vs pad size	1	3	4	2
Wafer map efficiency	1	4	2	3
Pitch / routing	4	3	2	1
Critical signal / component routing	4	3	1	2

Example: Microcontroller, 8 DUT

- Bond pad layout to avoid “corner crowding”
- Critical signals
  - Analog battery management signal, high speed lines
- Power distribution networks and voltage sensing
  - Voltage droop
- Array selection: routing vs thermal expansion
  - 2 x 4
  - 1 x 8

Routing Study Step 1a: Pad/Netlist

- Detailed, systematic process, electronic data transfer

Microsoft Excel - Example DesCap.xls

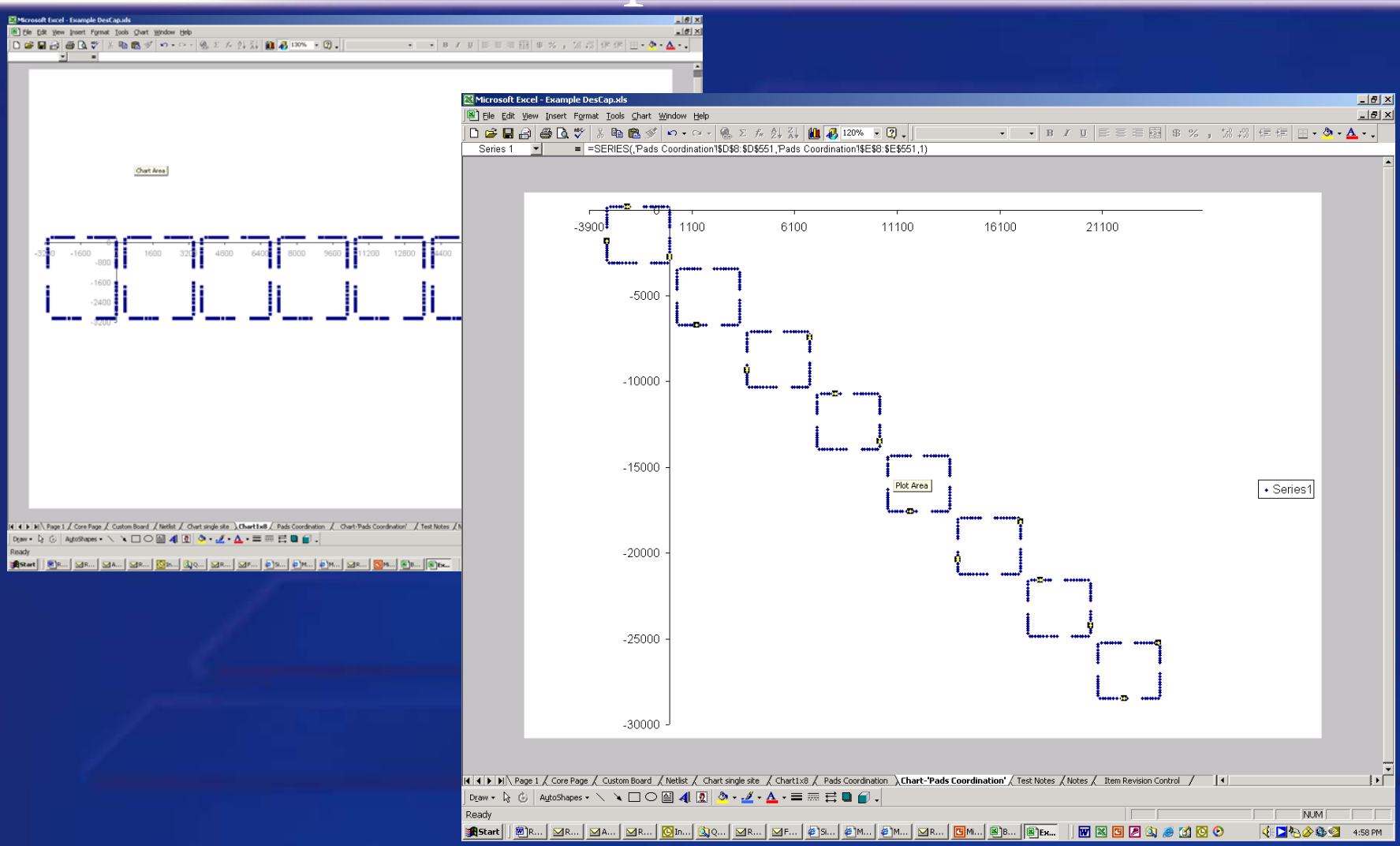
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
1	Pyramid Probe™																			
2	Probe Table -																			
3																				
4						As Measured BY CMI														
5	DUT	Pad	DUT &	Pad Center (customer Provided)		Pad Center		Pad	Line type:	Bandwidth	Maximum	Netlist generated by Design checker with corrected coordinate system (07/22/04)		PCB net name			PCB /	Pogo Pad	Other requirements / notes	
6	No.	No.	Pad No.	(0,0 =)		(0,0 =)		Name	AC, DC,	or Risetime	current if						Core	Number /	Explain on separate sheet, if ne	
7				X	Y	X	Y		P, GND	[MHz or nS]	> 0.1 Amp						Interface	Header#		
9	0	1	0_1	0	0	0	0	PTH0	DC			0_1PTH0	NC47	0_PTF6_H0	0	1	NC47	71		NC47_0_1_PTH0
10	0	2	0_2	0	-140	0	-137	PTD3	DC			0_2PTD3	NA125	0_PTD3	0	2	NA125	455		NA125_0_2_PTD3
11	0	3	0_3	0	-280	0	-273	PTD2	DC			0_3PTD2	ND49	0_PTD2_G2	0	3	ND49	199		ND49_0_3_PTD2
12	0	4	0_4	0	-435	0	-424	VSSADC/VREFL	GND			0_4VSSADC/VREFL	GR	GND	0	4	GR	GND		
13	0	5	0_5	0	-555	0	-550	VSSADC/VREFL	GND			0_5VSSADC/VREFL	GR	GND	0	5	GR	GND		
14	0	6	0_6	0	-715	0	-706	VDDADC	P			0_6VDDADC	NB47	0_VDD	0	6	NB47	P0		NB47_0_6_VDDADC
15	0	7	0_7	0	-855	0	-843	PTD1	DC			0_7PTD1	NC49	0_PTD1_G1	0	7	NC49	343		NC49_0_7_PTD1
16	0	8	0_8	0	-990	0	-979	PTD0	DC			0_8PTD0	NB49	0_PTD0_G0	0	8	NB49	87		NB49_0_8_PTD0
17	0	9	0_9	0	-1630	0	-1624	PTB7	DC			0_9PTB7	SC05	0_PTB7	0	9	SC05	471		SC05_0_9_PTB7
18	0	10	0_10	0	-1790	0	-1784	PTB6	DC			0_10PTB6	SB05	0_PTB6	0	10	SB05	215		SB05_0_10_PTB6
19	0	11	0_11	0	-1950	0	-1944	PTB5	DC			0_11PTB5	SA011	0_PTB5	0	11	SA011	326		SA011_0_11_PTB5
20	0	12	0_12	0	-2110	0	-2105	PTB4	DC			0_12PTB4	SA012	0_PTB4	0	12	SA012	70		SA012_0_12_PTB4
21	0	13	0_13	0	-2270	0	-2265	PTB3	DC			0_13PTB3	SD06	0_PTB3	0	13	SD06	454		SD06_0_13_PTB3
22	0	14	0_14	0	-2435	0	-2425	PTB2	DC			0_14PTB2	SC06	0_PTB2	0	14	SC06	198		SC06_0_14_PTB2
23	0	15	0_15	0	-2595	0	-2585	PTB1	DC			0_15PTB1	SB06	0_PTB1	0	15	SB06	342		SB06_0_15_PTB1
24	0	16	0_16	0	-2720	0	-2709	PTB0	DC			0_16PTB0	SA014	0_PTB0	0	16	SA014	SEE FIG. A		SA014_0_16_PTB0
25	0	17	0_17	0	-2885	0	-2871	PTA7	DC			0_17PTA7	SA015	0_PTA7	0	17	SA015	453		SA015_0_17_PTA7
518	7	50	7_50	20885	-35	20882.5	-32	IRQ1	DC			7_50IRQ1	NC08	7_IRQ1	7	50	NC08	437	R15/132	NC08_7_50_IRQ1
519	7	51	7_51	20885	110	20882.5	114	PTC4	DC			7_51PTC4	ND08	7_PTC4	7	51	ND08	293		ND08_7_51_PTC4
520	7	52	7_52	21060	195	21060.5	200	PTC5	DC			7_52PTC5	NA018	7_PTC5	7	52	NA018	317		NA018_7_52_PTC5
521	7	53	7_53	21220	195	21222.5	200	PTC3	DC			7_53PTC3	NA017	7_PTC3	7	53	NA017	44		NA017_7_53_PTC3
522	7	54	7_54	21350	195	21350.5	200	PTC2	DC			7_54PTC2	NA016	7_PTC2	7	54	NA016	300		NA016_7_54_PTC2
523	7	55	7_55	21475	195	21481	200	PTC1	DC			7_55PTC1	NC07	7_PTC1	7	55	NC07	189		NC07_7_55_PTC1
524	7	56	7_56	21605	195	21608	200	PTC0	DC			7_56PTC0	ND07	7_PTC0	7	56	ND07	445		ND07_7_56_PTC0
525	7	57	7_57	21735	195	21738.5	200	OSC1	DC			7_57OSC1	NB07	7_OSC1	7	57	NB07	172		NB07_7_57_OSC1
526	7	58	7_58	21865	195	21866	200	OSC2	DC			7_58OSC2	NA014	7_OSC2	7	58	NA014	428		NA014_7_58_OSC2
527	7	59	7_59	21995	195	22000.5	200	CGMXFC	DC			7_59CGMXFC	NC06	7_CGMXFC	7	59	NC06	316		NC06_7_59_CGMXF
528	7	60	7_60	22690	195	22690	200	AVSSADC/VSS	GND			7_60AVSSADC/VSS	GR	GND	7	60	GR	GND		
529	7	61	7_61	22815	195	22815.5	200	AVSSADC/VSS	GND			7_61AVSSADC/VSS	GR	GND	7	61	GR	GND		
530	7	62	7_62	22990	195	22995	200	VDDA	P			7_62VDDA	NB04	7_VDD	7	62	NB04	P7		NB04_7_62_VDDA
531	7	63	7_63	23125	195	23130.5	200	VREFH	DC			7_63VREFH	NB03	7_VREFH	7	63	NB03	CTO-7-VRA		NB03_7_63_VREFH
532	7	64	7_64	23255	195	23257.5	200	PTD7	DC			7_64PTD7	NC03	7_PTD7	7	64	NC03	299		NC03_7_64_PTD7
533	7	65	7_65	23390	195	23395	200	PTD6	DC			7_65PTD6	ND03	7_PTD6	7	65	ND03	171		ND03_7_65_PTD6
534	7	66	7_66	23525	195	23532.5	200	PTD5	DC			7_66PTD5	NA006	7_PTD5	7	66	NA006	427		NA006_7_66_PTD5
535	7	67	7_67	23665	195	23669.5	200	PTD4	DC			7_67PTD4	NA005	7_PTD4	7	67	NA005	59		NA005_7_67_PTD4
536	7	68	7_68	23820	195	23828	200	PTH1	DC			7_68PTH1	ND02	7_PTF7_H1	7	68	ND02	315		ND02_7_68_PTH1
537																				
538																				

Page 1 / Core Page / Custom Board / Netlist / Chart single site / Chart1x8 / Pads Coordination / Chart-'Pads Coordination' / Test Notes / Notes / Item Revision Control

Ready Sum=141606 NUM

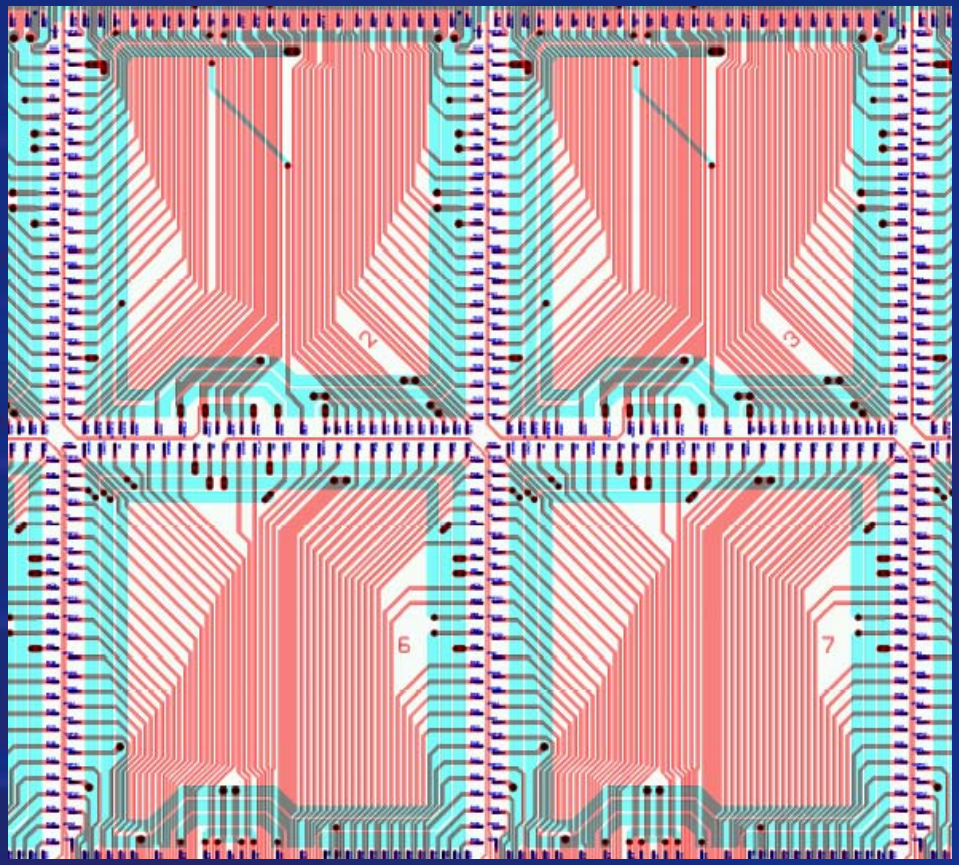
Start 4:54 PM

Routing Study Step 1b: Generate Pattern Options



Routing Study Step 1c: Route Critical Areas

- Practice symmetry
  - Uniformity die-die
  - Easier to edit / sustain
- Manage propagation delay matching
- Manage series resistance of critical lines



Temperature / Position Accuracy Calculation

Inputs:

Pad X dimension	55
Pad Y dimension	55
Passivation Thickness	0.8
Make/Model of Probe Station	xxx
Make/Model of Tester	xxx
Probe Tip Type	3
Probing Temperature Max	125
East West Die Size	24400
North South Die Size	12050
Customer Substrate Material	Si
Output: Single card capable?	No

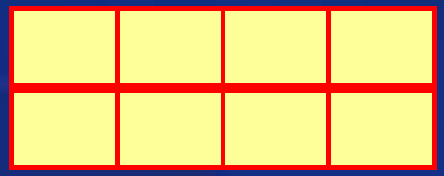
- Conclusion: Two cards required, 25 & 125 C

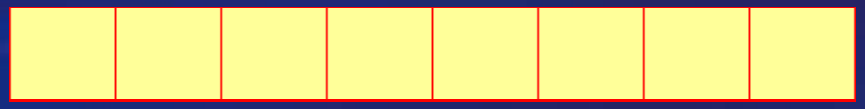
Critical Signals: Length Matching

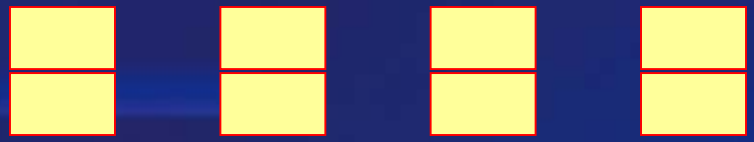
Line type: RF, AC, DC,P,GND	Bandwidth or Risetime [GHz or pS]	Ref Designator Header#	Other requirements (impedance match, delay match, - line(s) / tolerance, etc. Explain on separate sheet, if necessary)
N/C		NC	
AC	200MHz	12	Analog input 1-2 mV. Match pair +/- 10ps.
AC	200MHz	13	Analog input 1-2 mV. Match pair +/- 10ps.
AC	200 ps	14	Analog output Match pair +/- 10ps.
AC	200 ps	15	Analog output Match pair +/- 10ps.
AC	200 ps	16	Analog output Match pair +/- 10ps.
AC	200 ps	17	Analog output Match pair +/- 10ps.
AC	200MHz	18	Analog input 1-2 mV. Match pair +/- 10ps.
AC	200MHz	19	Analog input 1-2 mV. Match pair +/- 10ps.

Wafer Map

- Dense pack is possible in this case
  - Not limited by routing
  - Not limited by component placement
- Larger patterns / skips not required

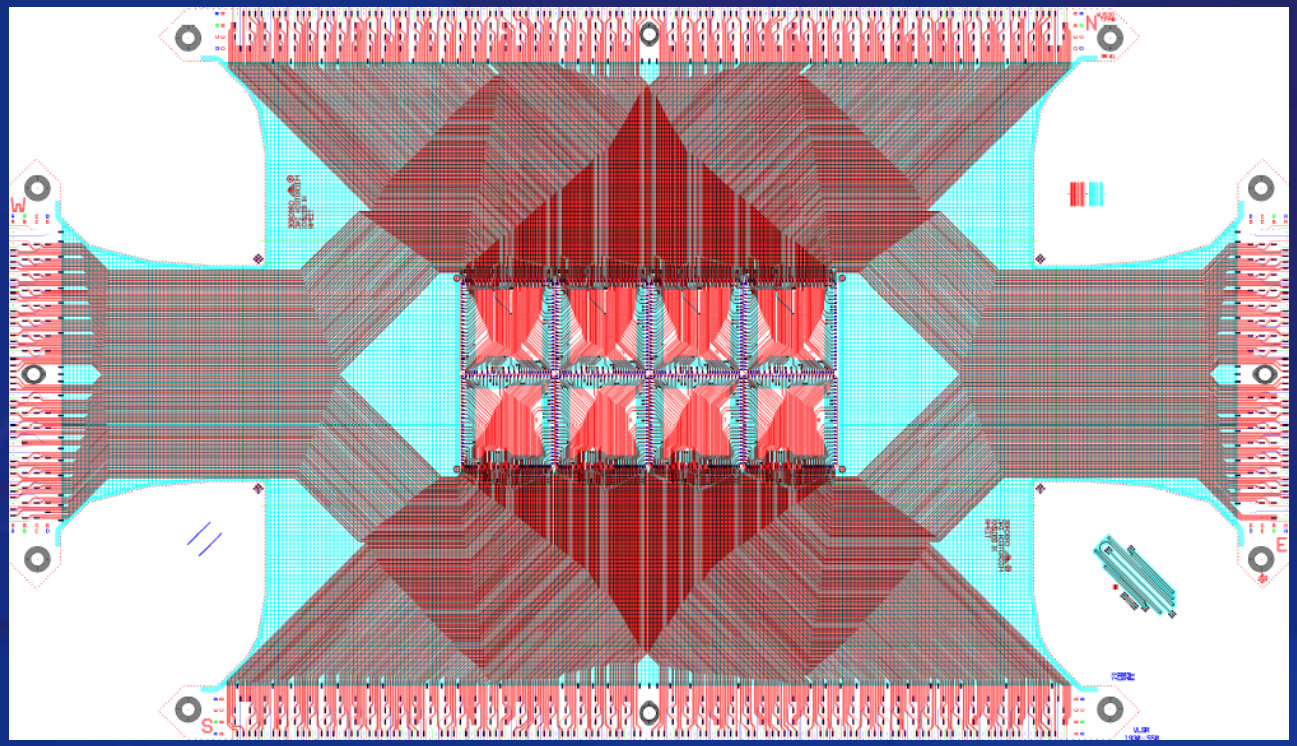






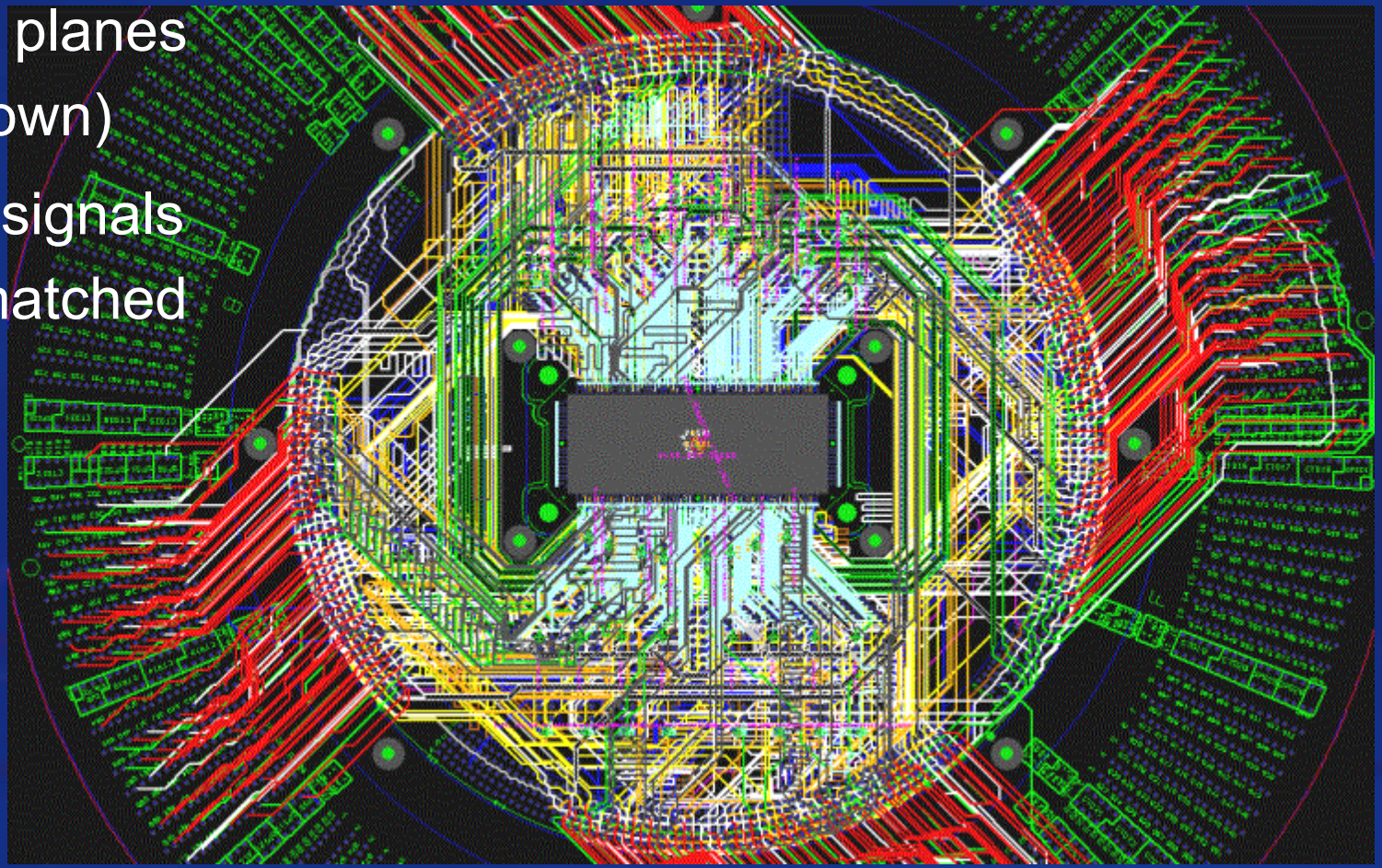
Core Layout 2 x 4 Array

- 12 x 24 mm area
- 55 um pad size
- 800 I/O (signals)
- Separate cores for 25, 125 C (one PCB)



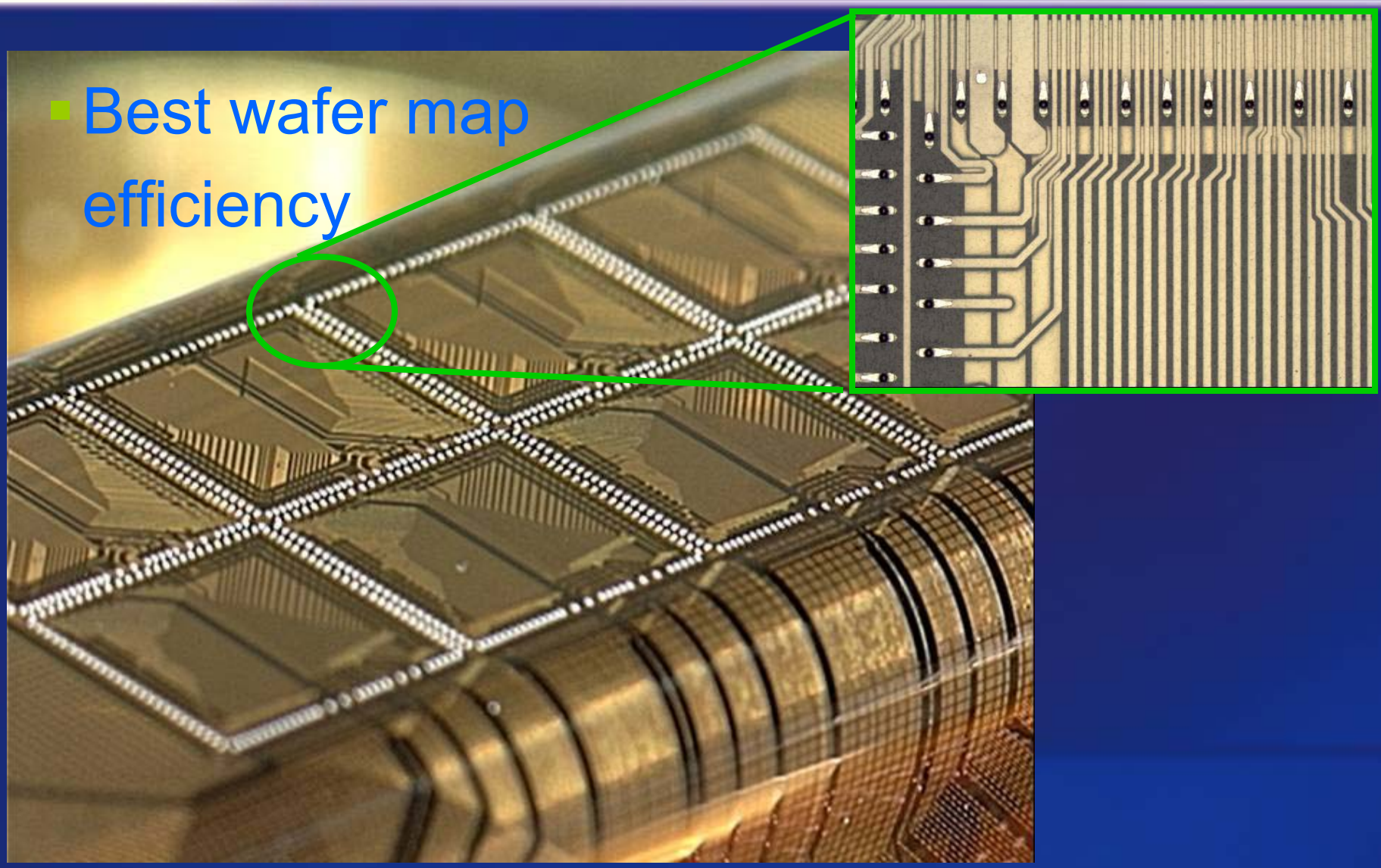
Board Layout

- Multiple ground / power planes (not shown)
- Critical signals delay matched



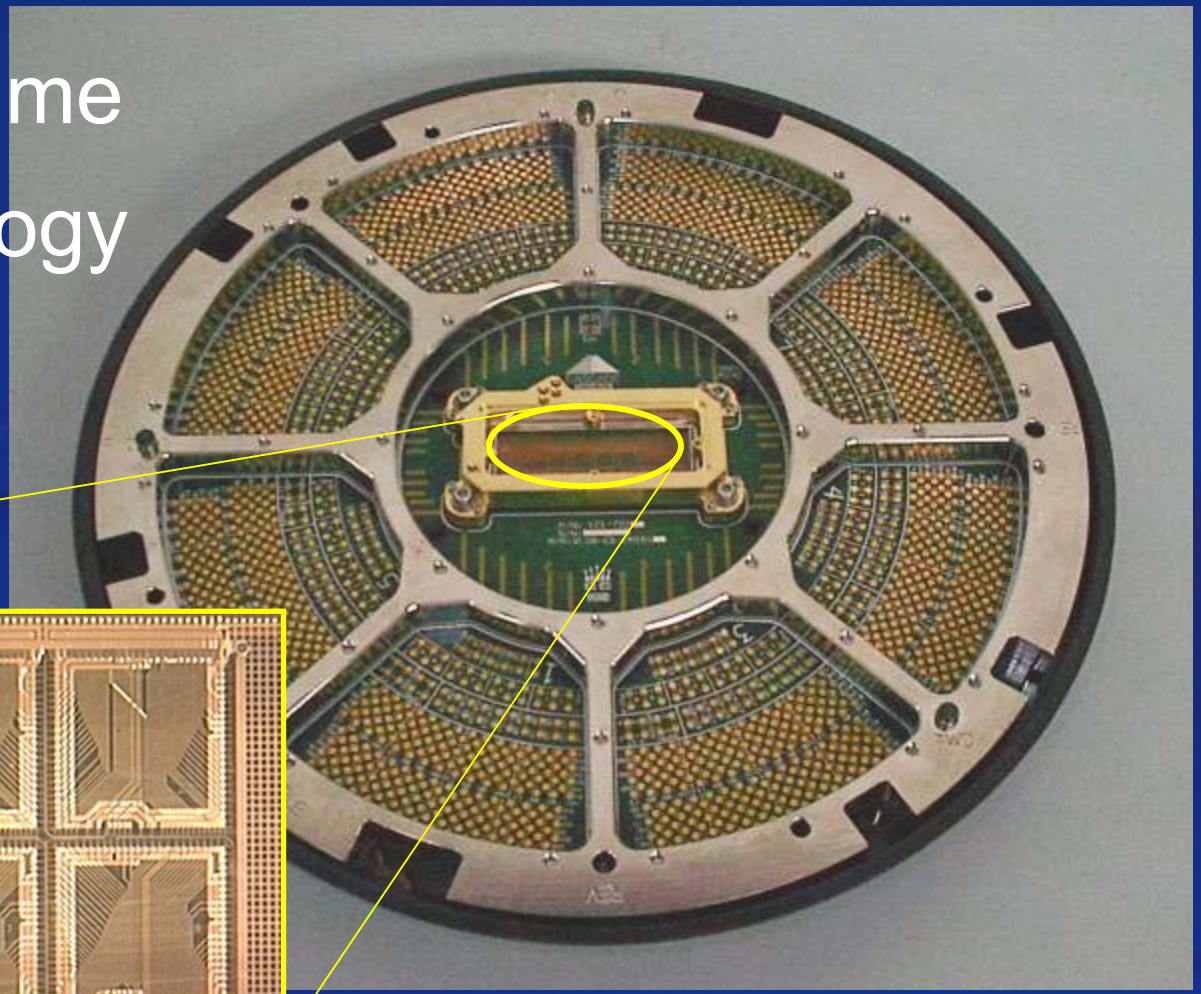
8-DUT Core (2 x 4 Array)

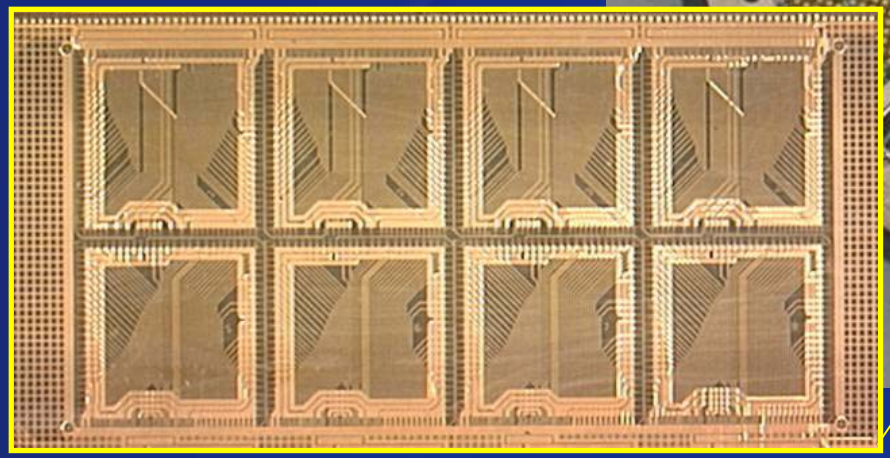
- Best wafer map efficiency



8-DUT Probe Card

- 8 week lead time
- Good technology fit





Other Considerations

- Street size / stepping distance may change at different fabs for the same device
  - Multi DUT cards may not be transferable between fabs
- Increased design complexity requires rapid response for design issues from both partners to minimize lead time
- Availability of a good Multi-DUT wafer map optimization algorithm
- Economic trade-offs among tester resources, load board components, on-chip test resources

Summary

- Multi-DUT probing is complicated and many details are critical, but manageable with a disciplined process
- A systematic collaborative process from IC design through installation is essential
- Multi-DUT test of advanced logic devices is increasing rapidly
- Cost reduction has been demonstrated (multiple test floors with HVM)

References

- Andrew C. Evans, “Applications of Semiconductor Test Economics, and Multisite Testing to Lower Cost of Test”, ITC 1999, pp.113-123
- Dominique Langlois and Patrick Buffel, “Let’s Skip and Win”, SWTW 2003