Full Wafer Test: Making Test More Cost-Effective

2005 SouthWest Test Workshop

June 5 - 8, 2005

AEHR TEST SYSTEMS

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Agenda

- Trends in multi-up probing
  - Total Test Time
  - Cost of Test
- Converging Technologies
  - Massively Parallel Test
  - Full Wafer Contact
  - Design For Test (DFT)
- Results of technology convergence
- Conclusions

Trends in Multi-Up Probing

- Trend over time has been to increase the number of DUTs tested per touchdown
- Leading edge probe cards are in the range of:
  - 32 to 250 DUTs *
  - 1000 to 5000 contacts *
- Goal is to move closer to single touchdown testing

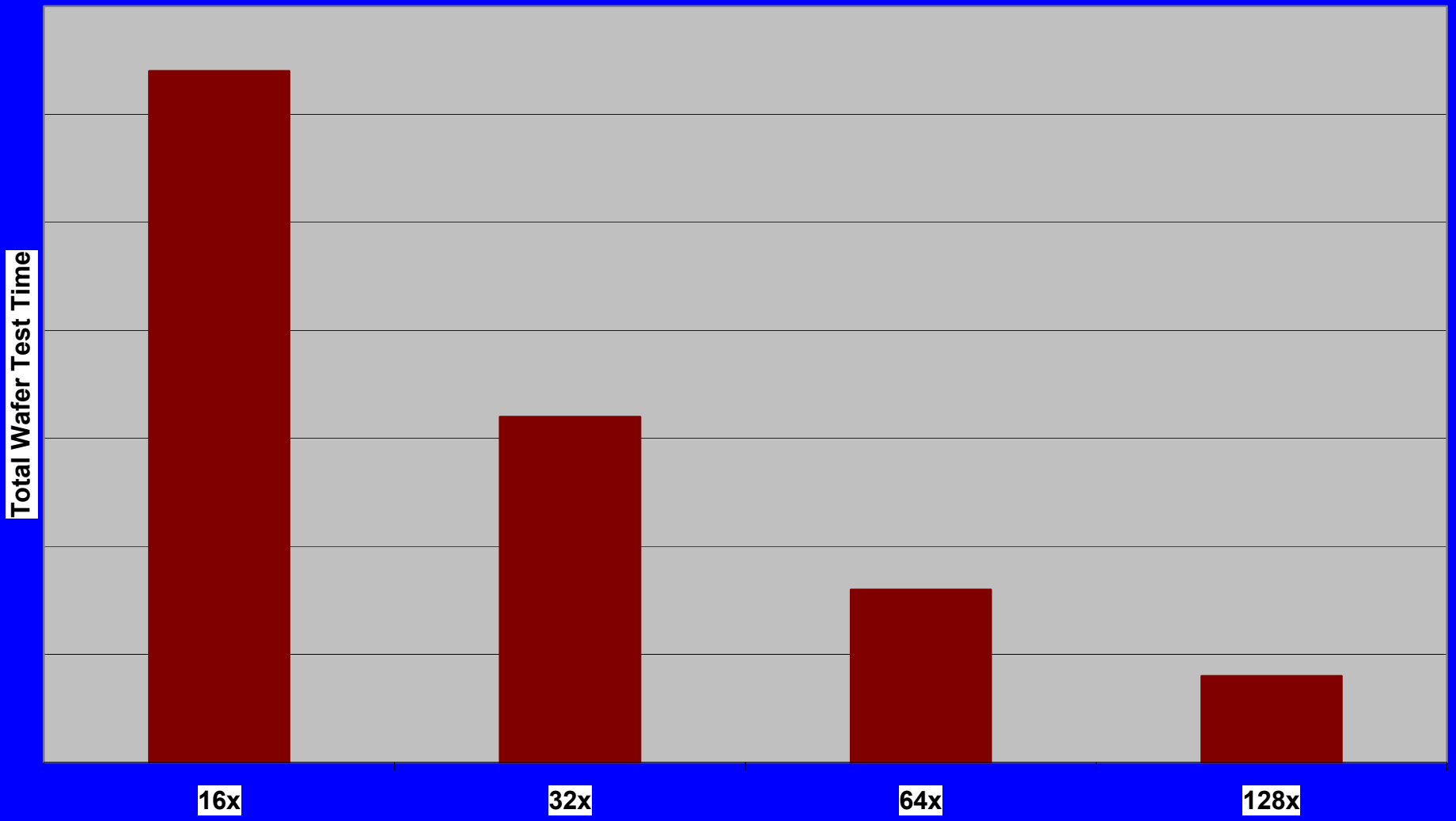
* Source: “Leading Edge” of Wafer Level Testing, Bill Mann, SWTW 2004

Total Test Time

- **Total time to test a wafer is:**
  - **Wafer exchange time (usually not significant)**
  - **Per step time * number of steps**
    - Step time
    - Test time per step

- **What if test time per step gets long?**

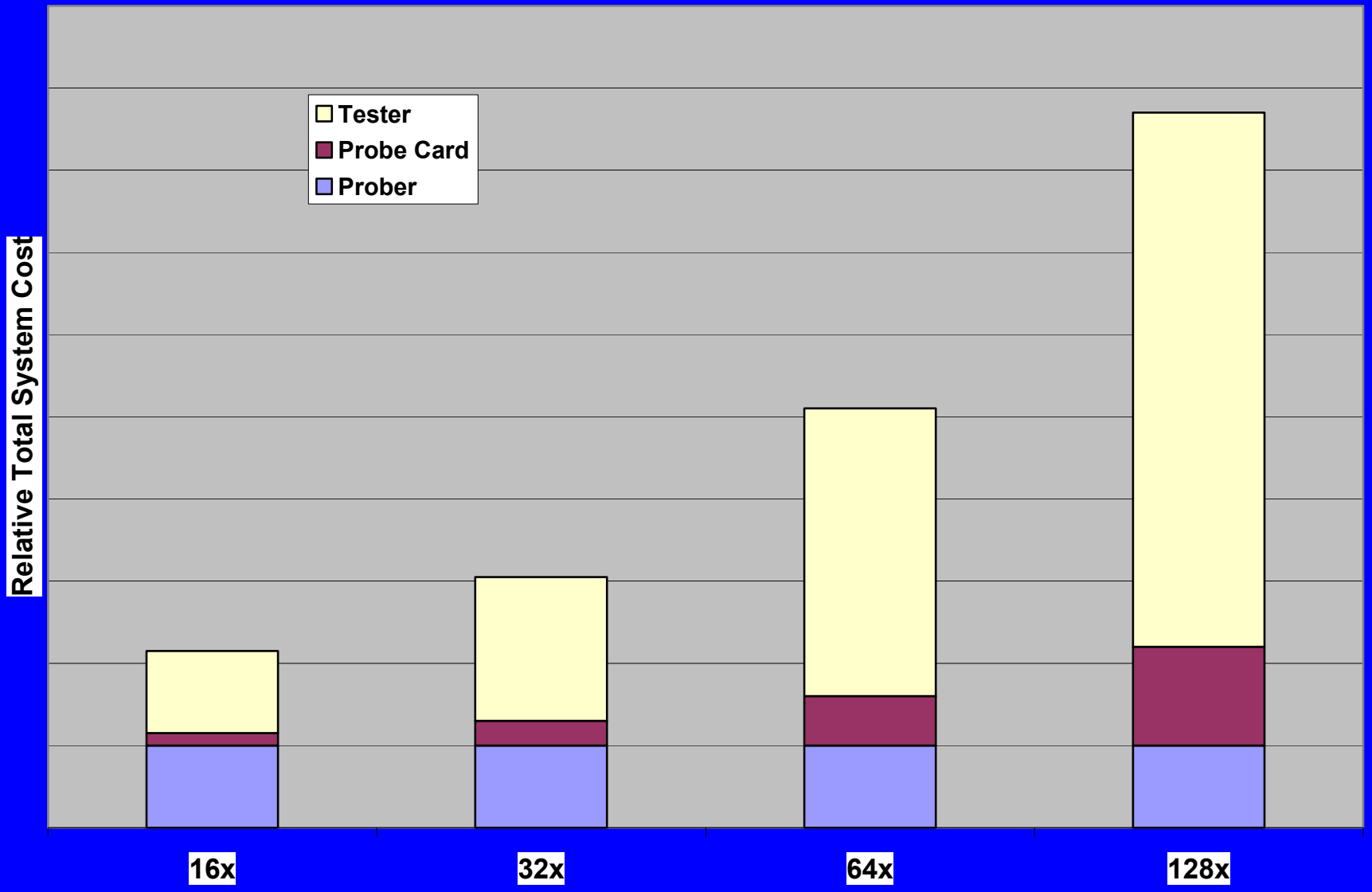
Wafer Test Time



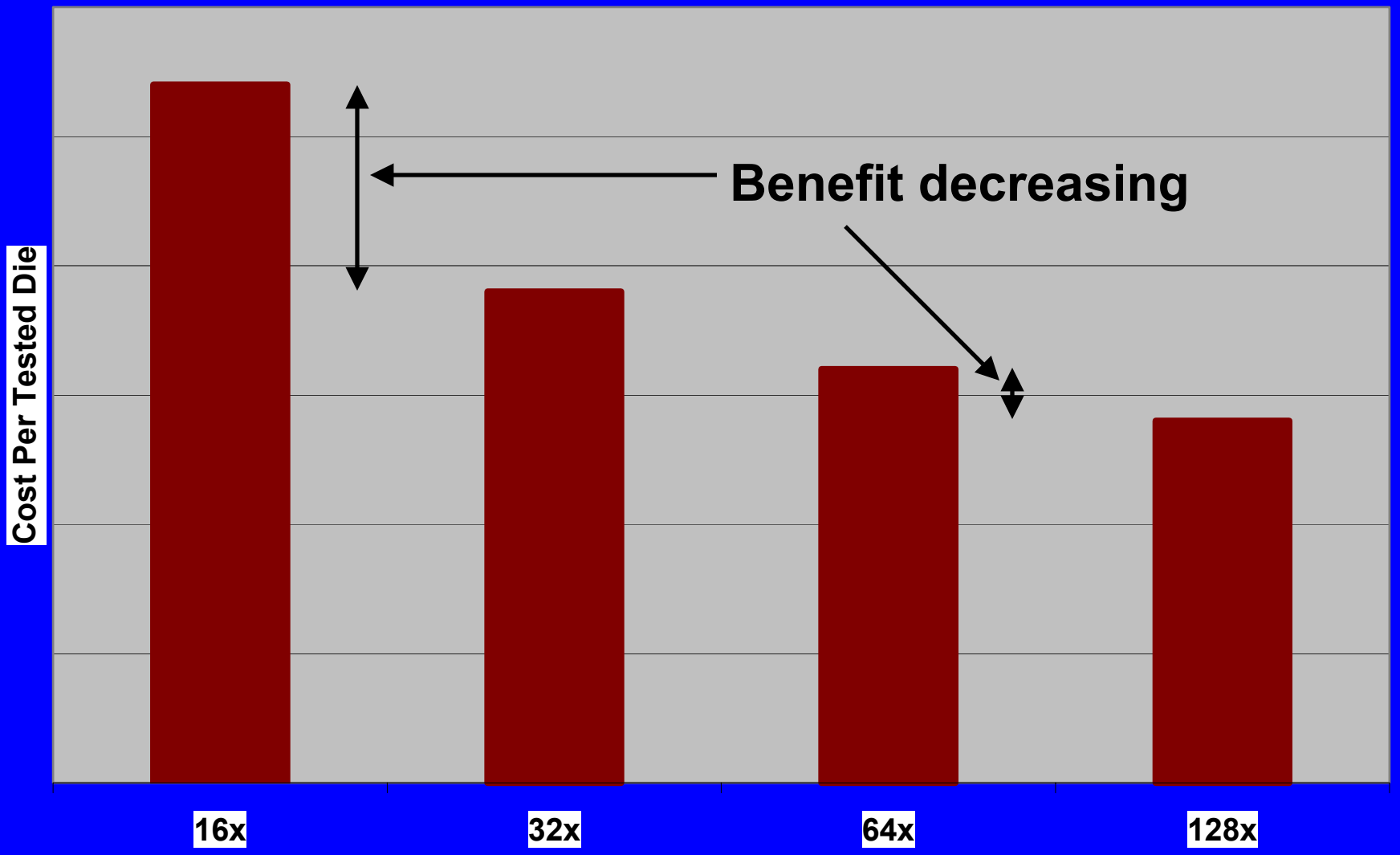
Cost of Test

- The primary costs are:
  - Prober
  - Probe Card
  - Tester
- As the number of die probed per step increases, the cost of
  - Prober remains mostly the same
  - Probe card gets more expensive (~linear)
  - Tester gets more expensive (~linear)
- Benefit of doubling the number of DUTs per touchdown decreases

Cost of Test

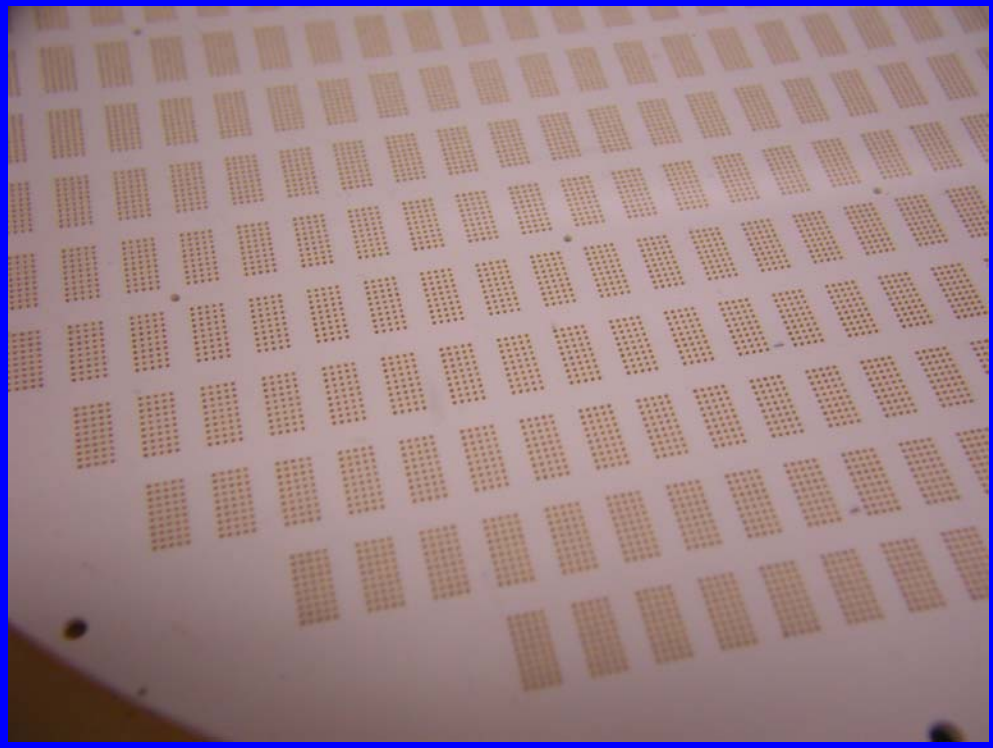

Tester
Probe Card
Prober
Relative Total System Cost
16x
32x
64x
128x

Cost Per Tested Die

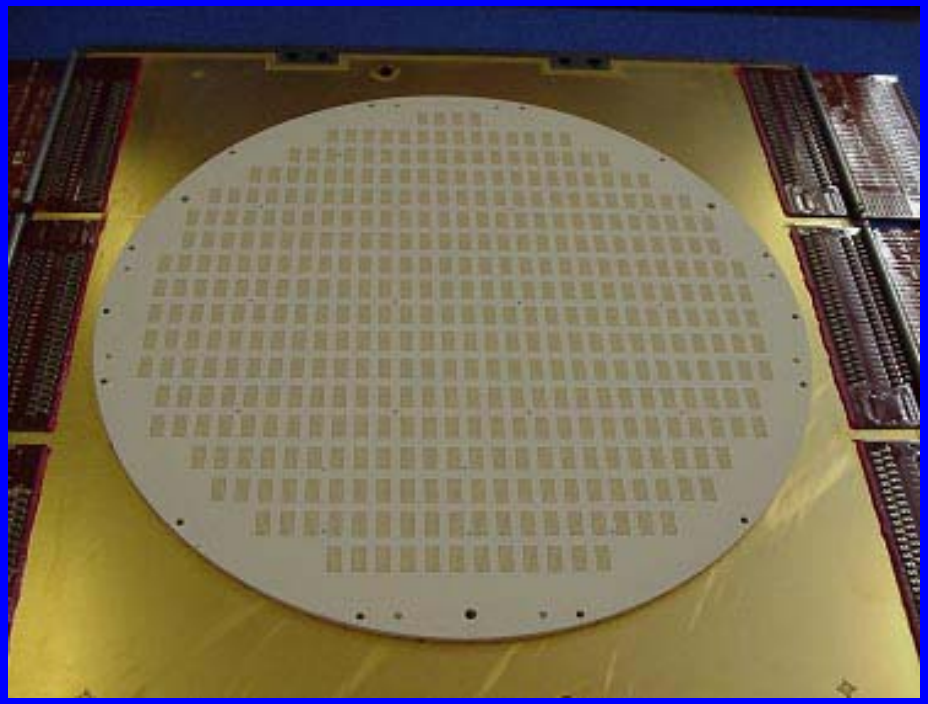


Converging Technologies

- Full Wafer Contact
- Massively Parallel Test
- Design For Test



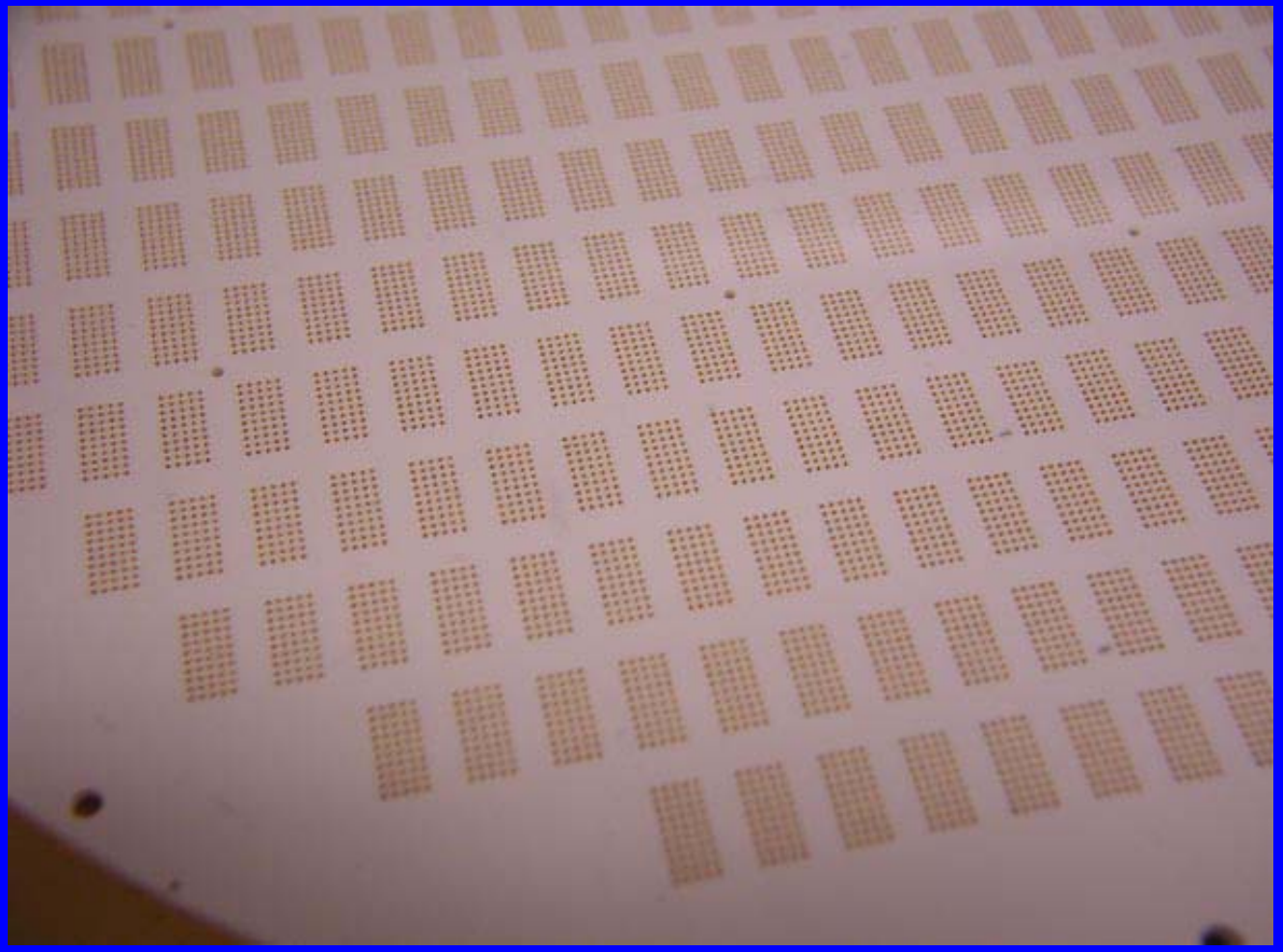
Micro Spring Contactor



- High touchdown life
- High compliance
- Works with most pad metallurgies
- Multiple pitches available

Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

Micro Spring Close-up (750u Pitch)

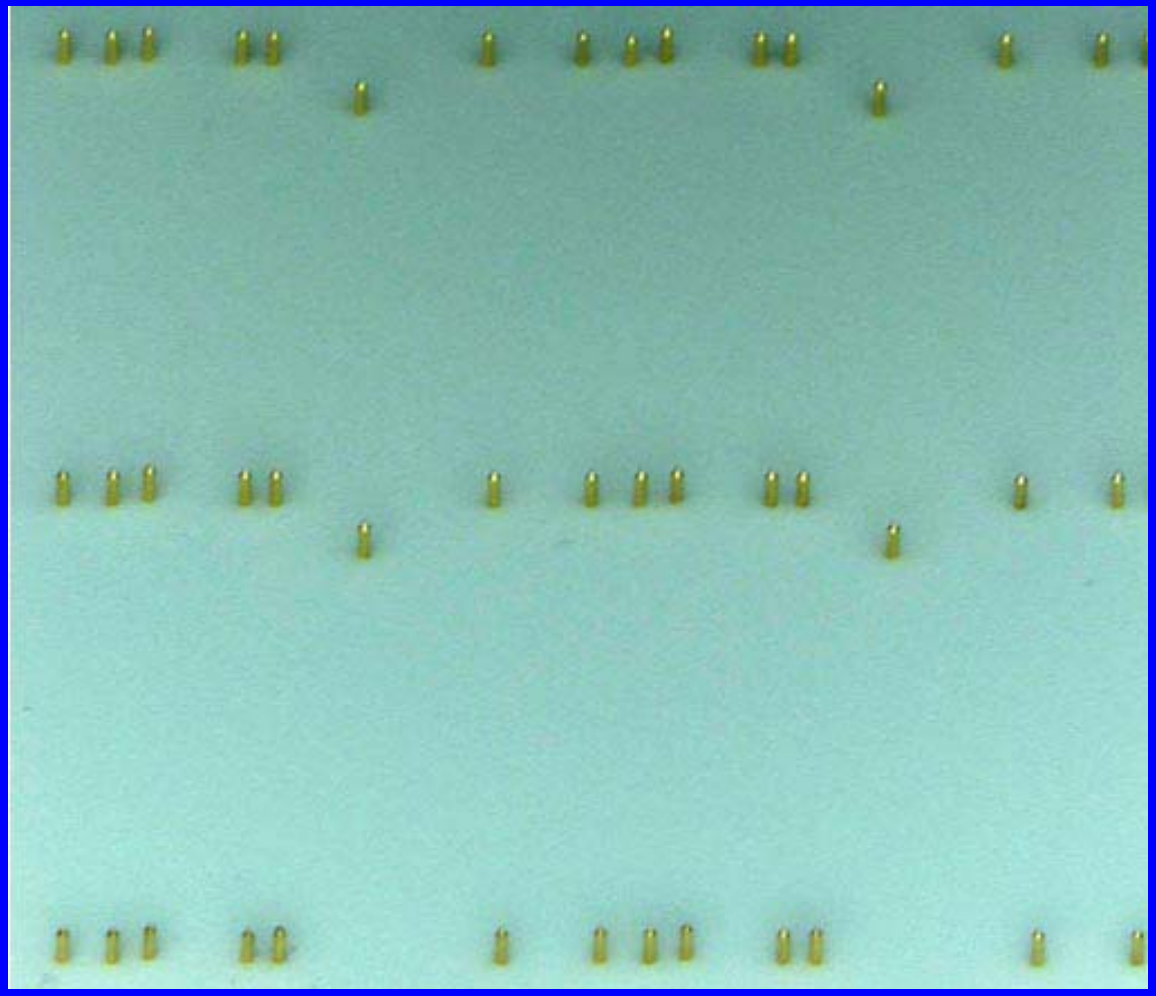


Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

Full Wafer Contactor

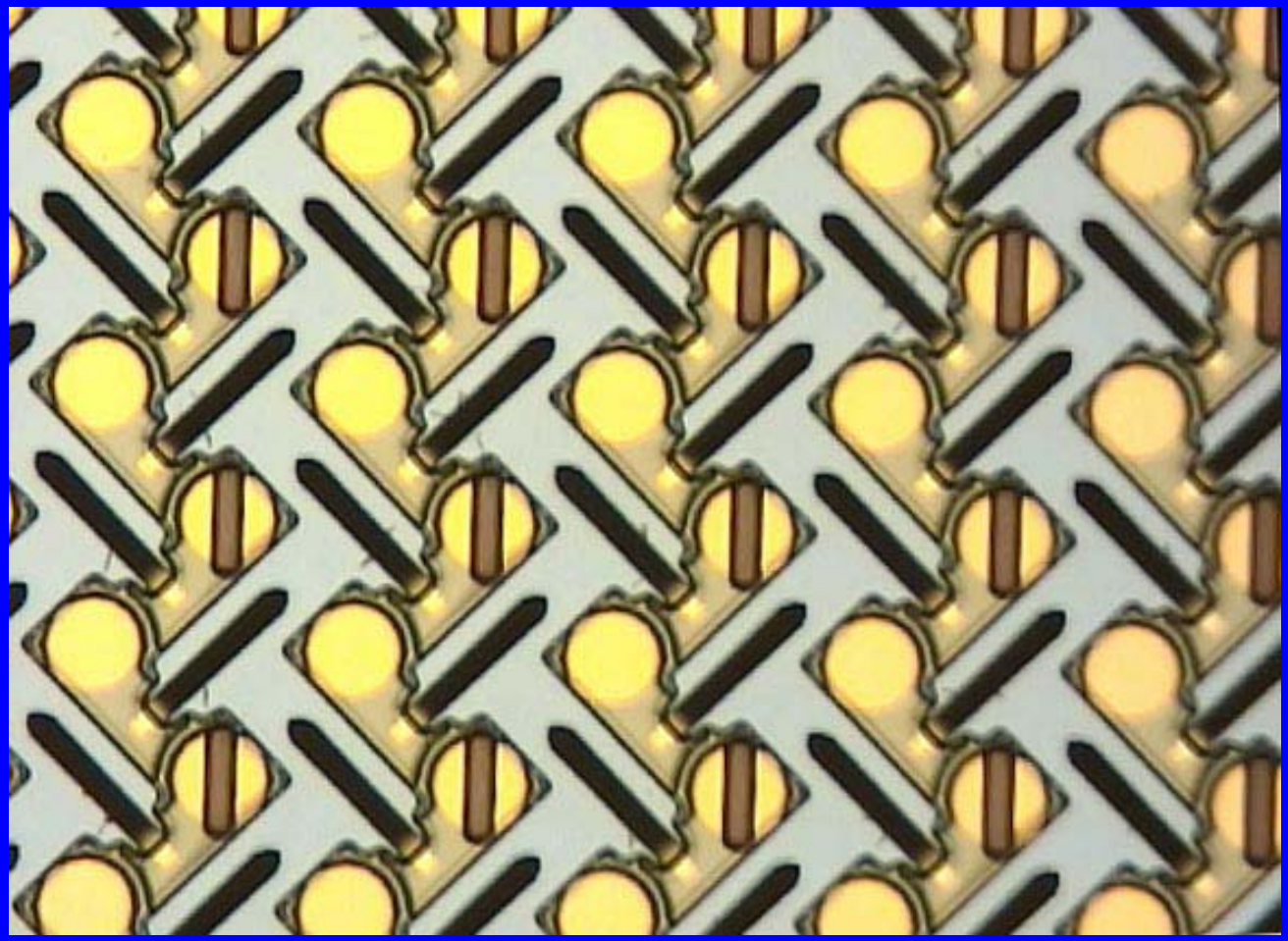
Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

Micro Spring Close-up (200u Pitch)



Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

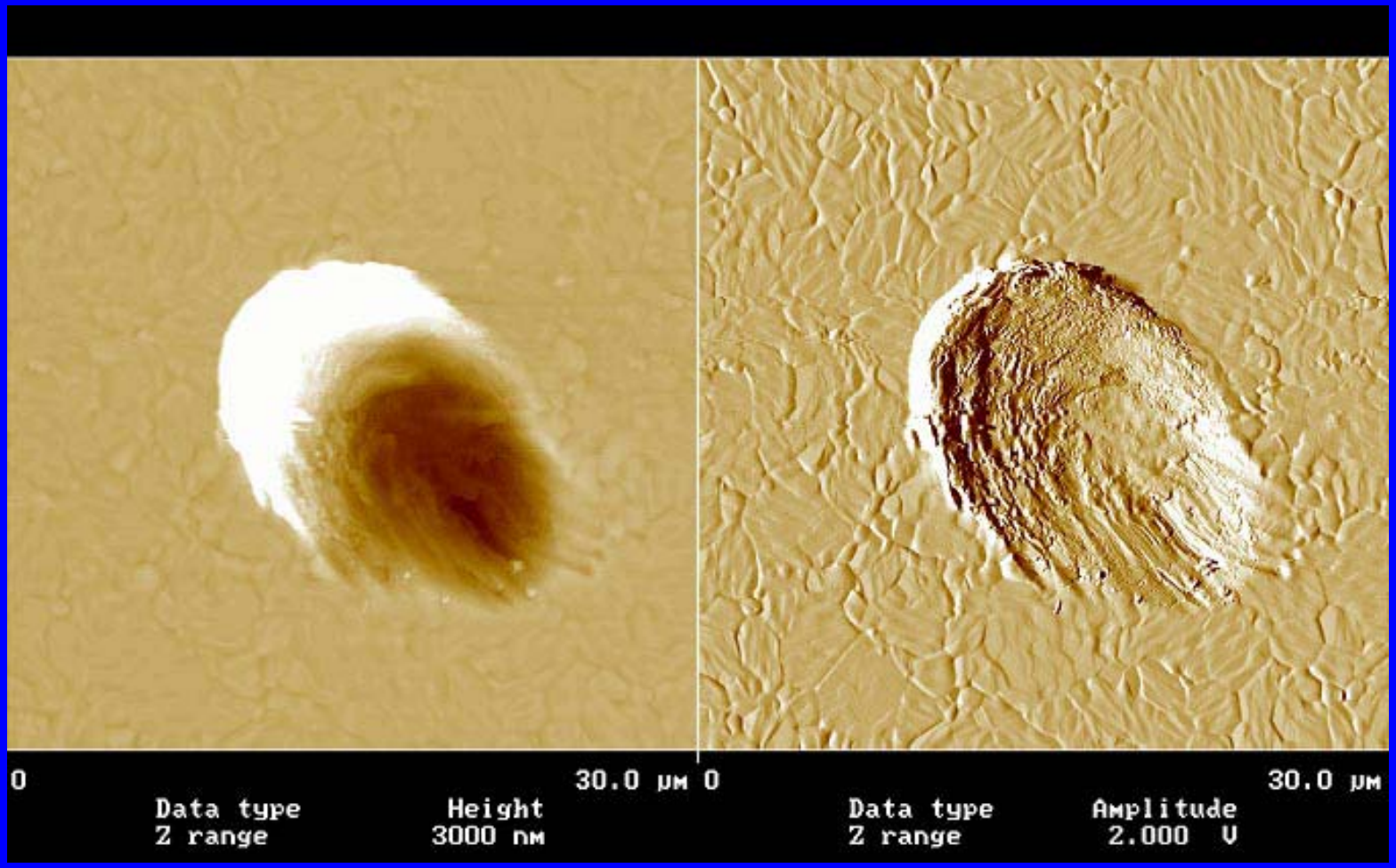
Nano Spring Contactor



Contactor Array
80 micron pads

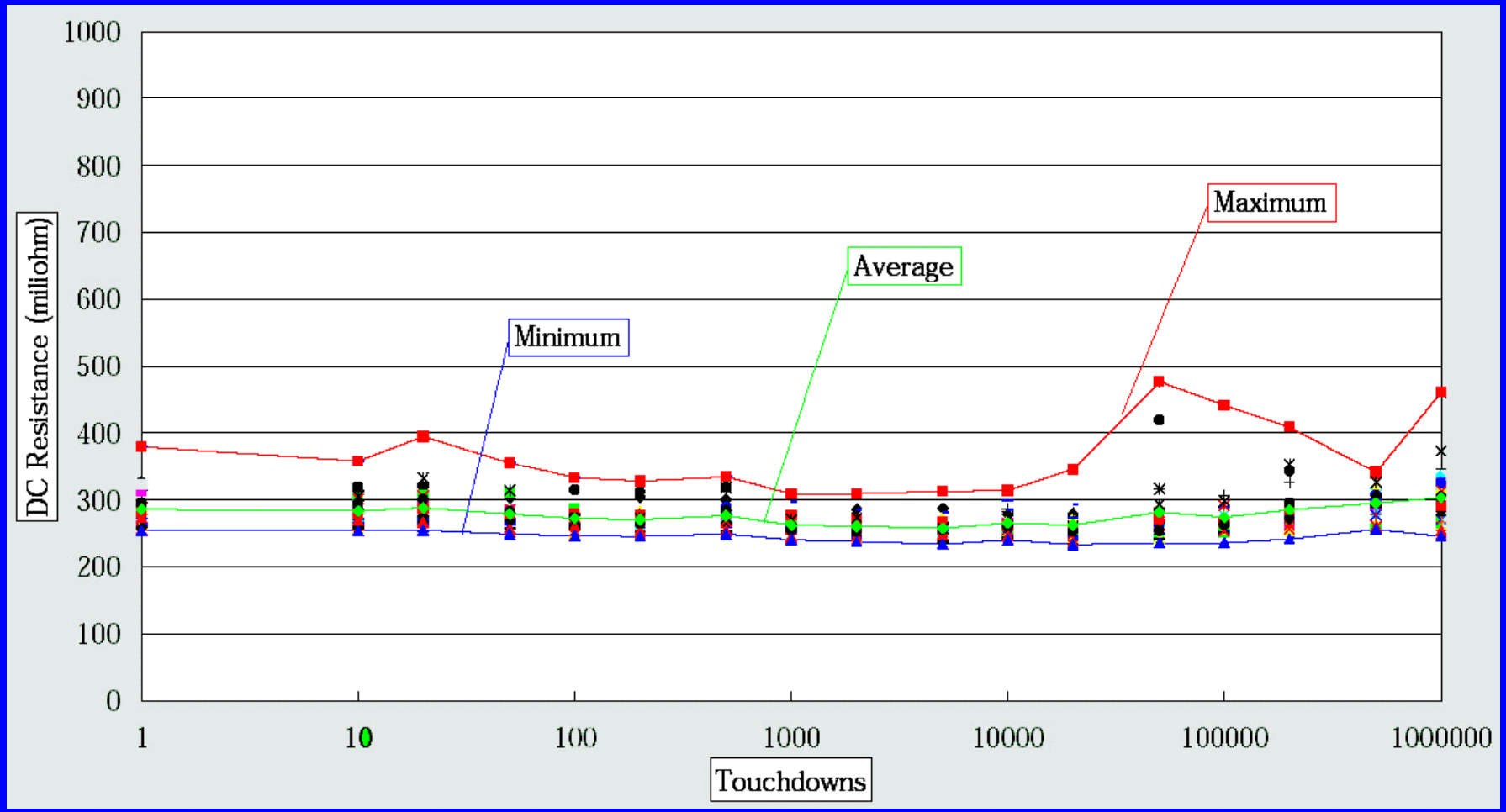
Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

Probe Marks



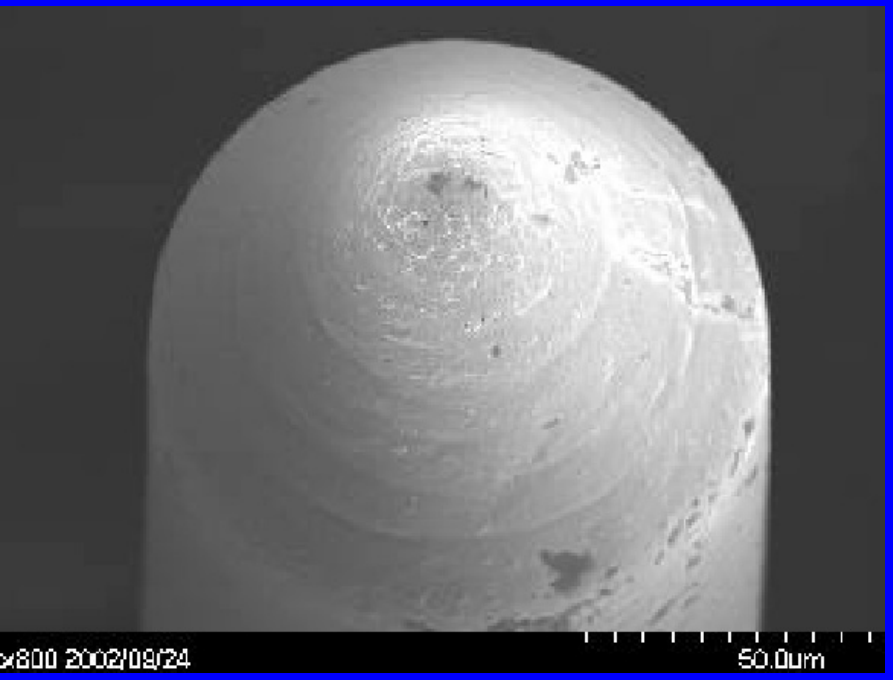
Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

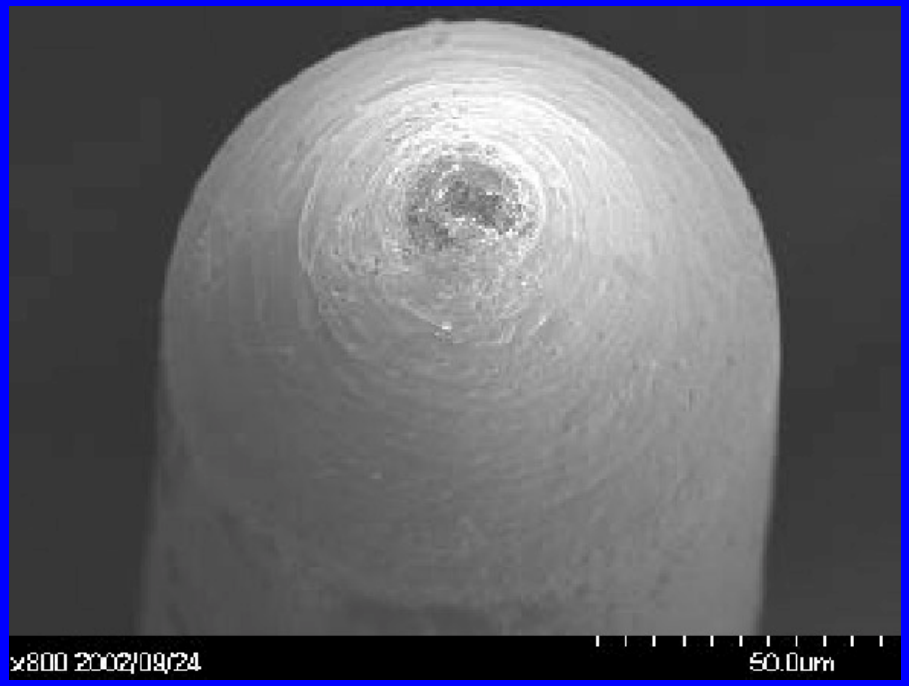
One Million Touchdowns



Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

Micro Spring Before and After

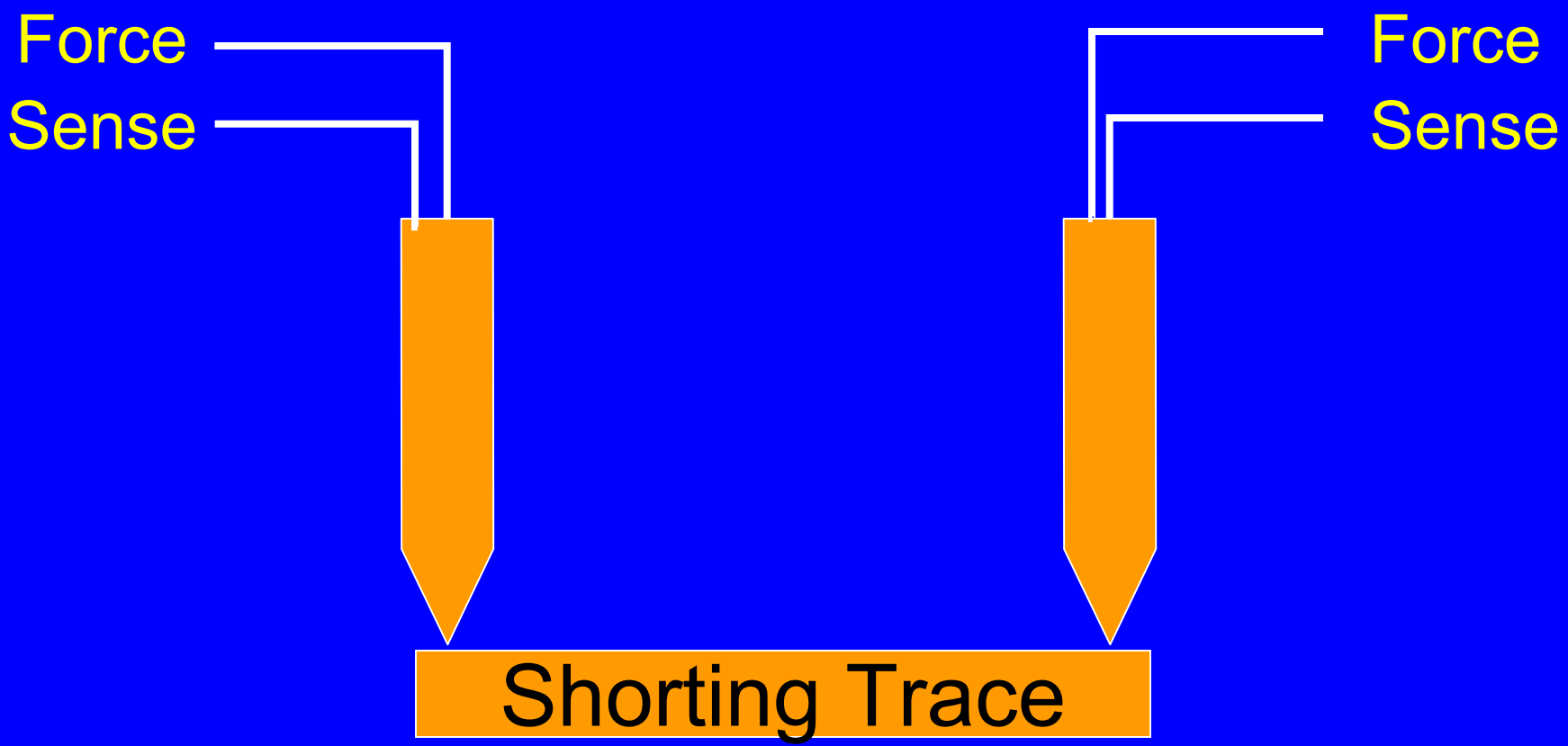




Pin Tip before and after 1 million touchdowns

Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

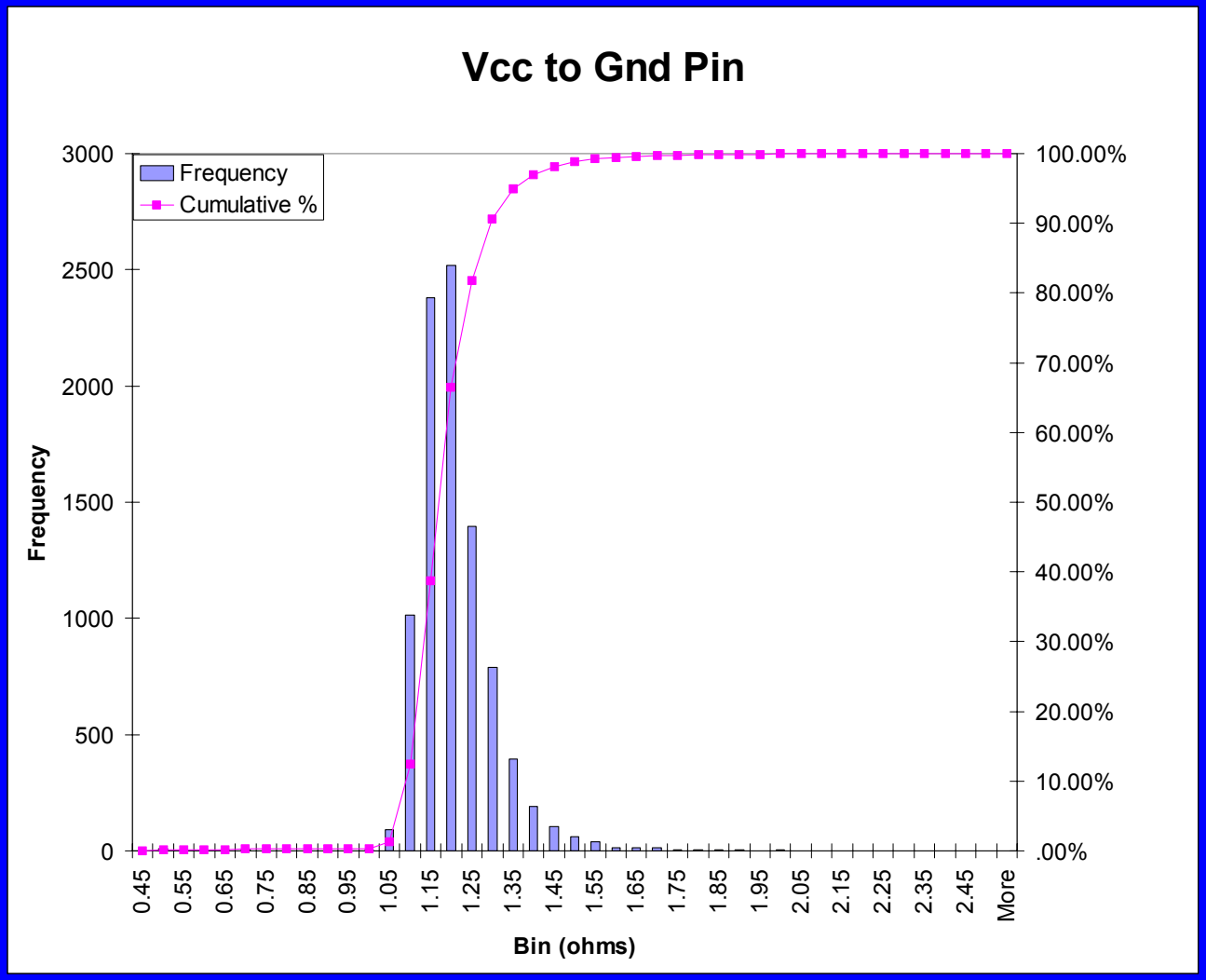
Loop Resistance Diagram



Loop Resistance = Two contacts plus trace resistance

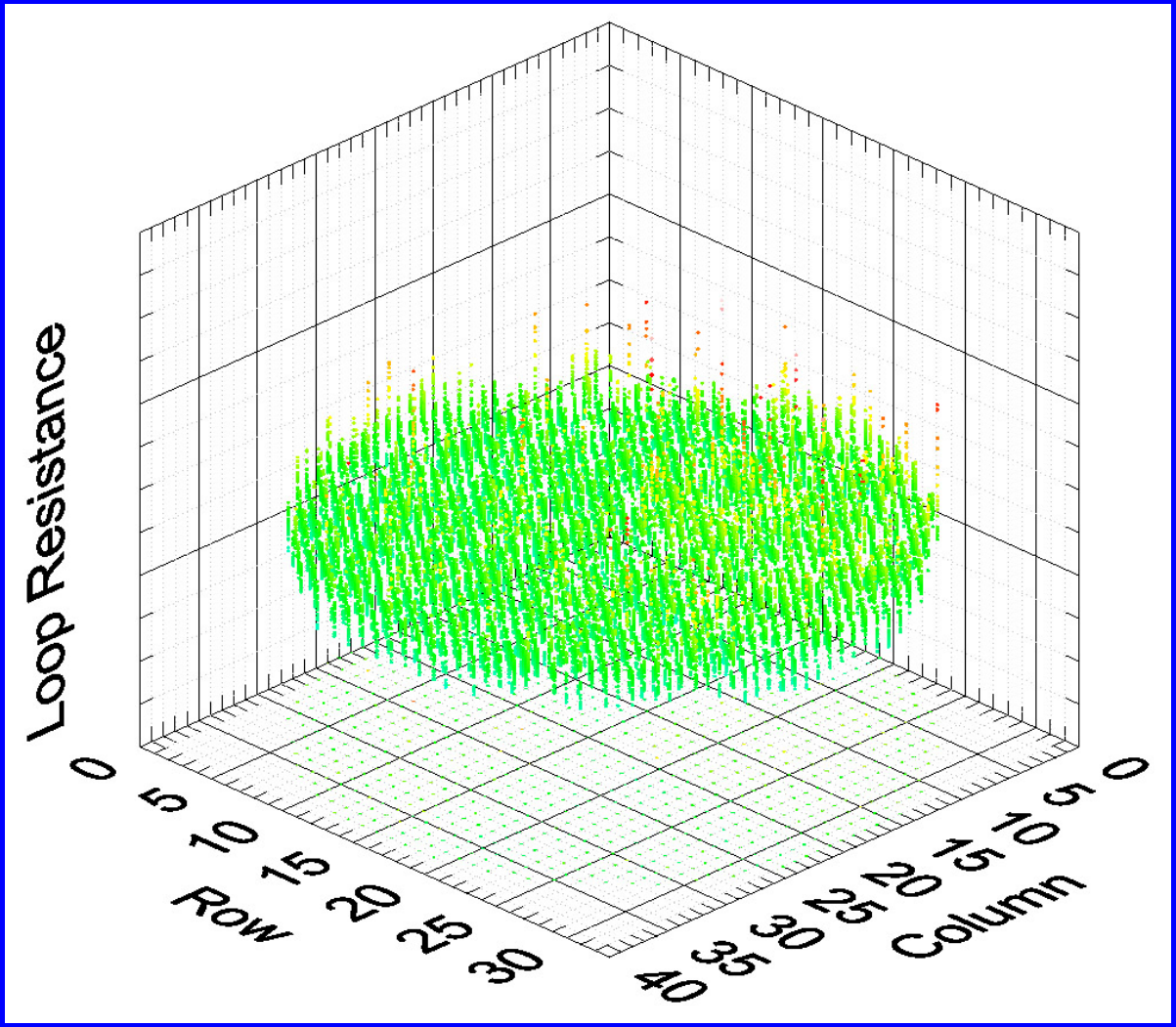
Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

Loop Resistance Histogram



Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

Full Wafer Contact Uniformity



Source: Full Wafer Contact Reliability and Repeatability, Steps/Lindsey, SWTW 2003

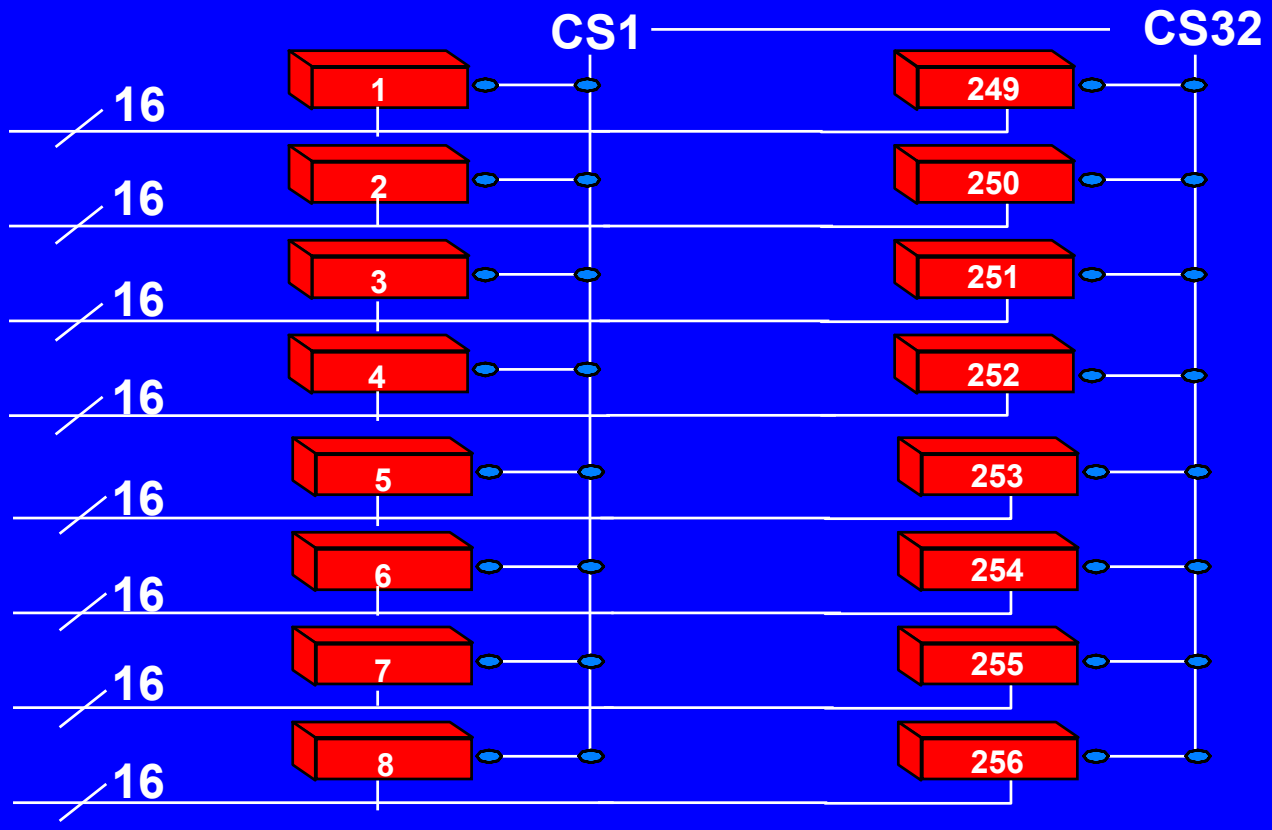
Massively Parallel Test

- Massively Parallel testing spreads the channel cost across many device I/O pins
- Parallel testing speeds are lower
  - Capacitive loading reduces the maximum frequency
  - No need for ultra high speed channels
  - Cost per channel is lower
- Combination of:
  - Multiple device I/O pins per channel
  - Lower per channel cost

→ Much lower cost per device I/O pin

Parallel Testing

128 Tester I/O Channels X 32 CS = 4096 Total Device I/O Pins



Source: Full Wafer Contact Burn-In and Test -- The Ultimate in Parallelism?, Steps, BiTS 2003

Standard Testing

- Full I/O speed
  - Cost per channel very high ($Ks/channel)
  - Signal cables must be very short
  - GHz testing very difficult
- Full I/O width
  - One channel per device pin
  - Total device count per test very limited

Test Evolution – Structural Test

- Typically scan chain based
- External clock rate needed vastly reduced
- On chip ATPG
  - I/O width significantly reduced
  - Still can have edge timing constraints
- Design For Test (DFT)
  - Device I/O pin clock rate << Internal clock rate
  - Very narrow I/O (e.g., 5 pin IEEE 1149.1)
  - Channel cost reduced (<$100/channel)
  - Parallel testing possible (<$5/device I/O)

Today's Testing Process

Using 32 site probe card:

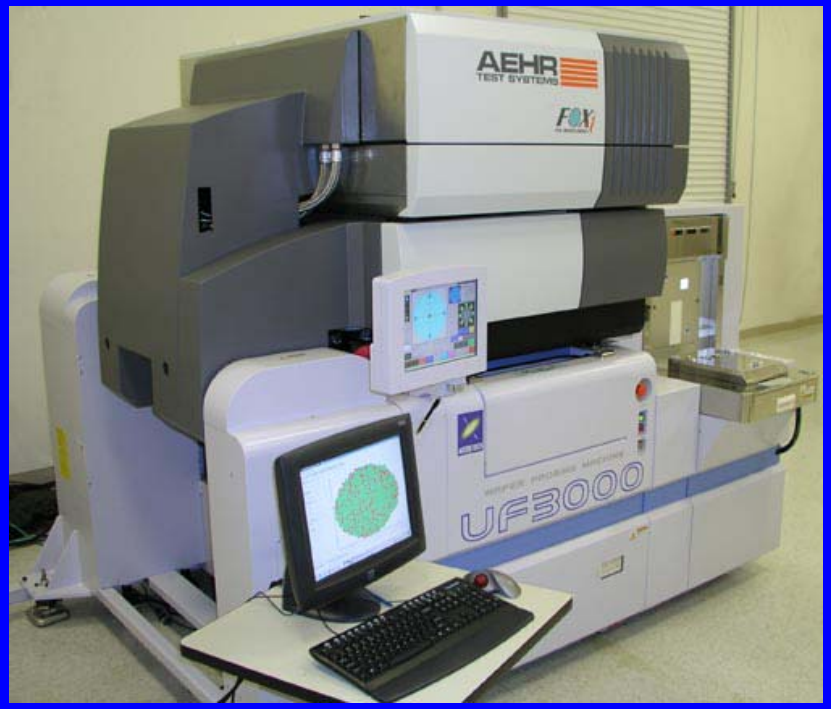
Load Wafer	Test	Step	Test	Step	Test	. . . .	Test

For 500 die wafer, about 20 cycles

Full-wafer Approach

Load Wafer | Test

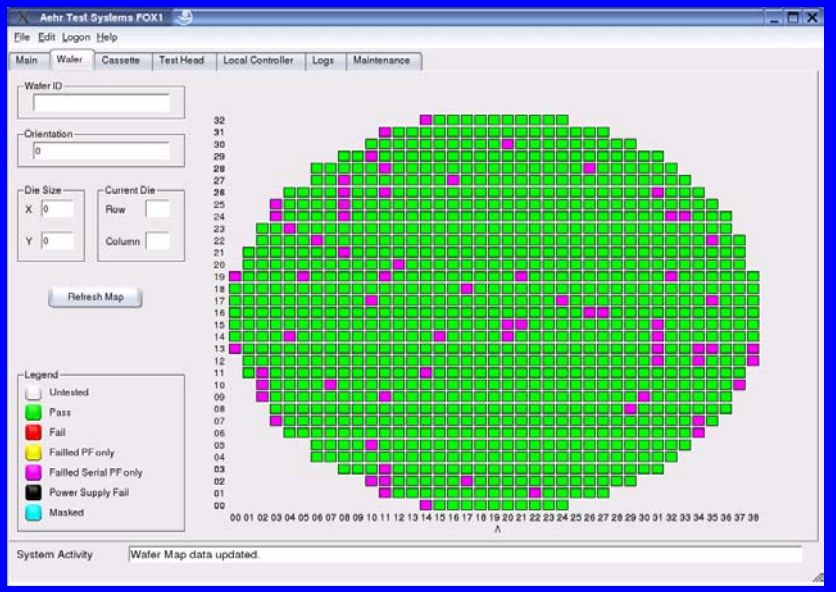
Only one cycle required



10-20X Time Reduction!

Results of Technology Convergence

- Correlation > 99% versus normal prober approach
- Massive reduction in:
  - Total wafer test time
  - Product inventory on test floor
  - Capital equipment
  - Cost per tested die



Conclusions

- **Full wafer testing has arrived!**