Pintail Technologies, Inc.

Dynamic Parts Average Testing in Real-time

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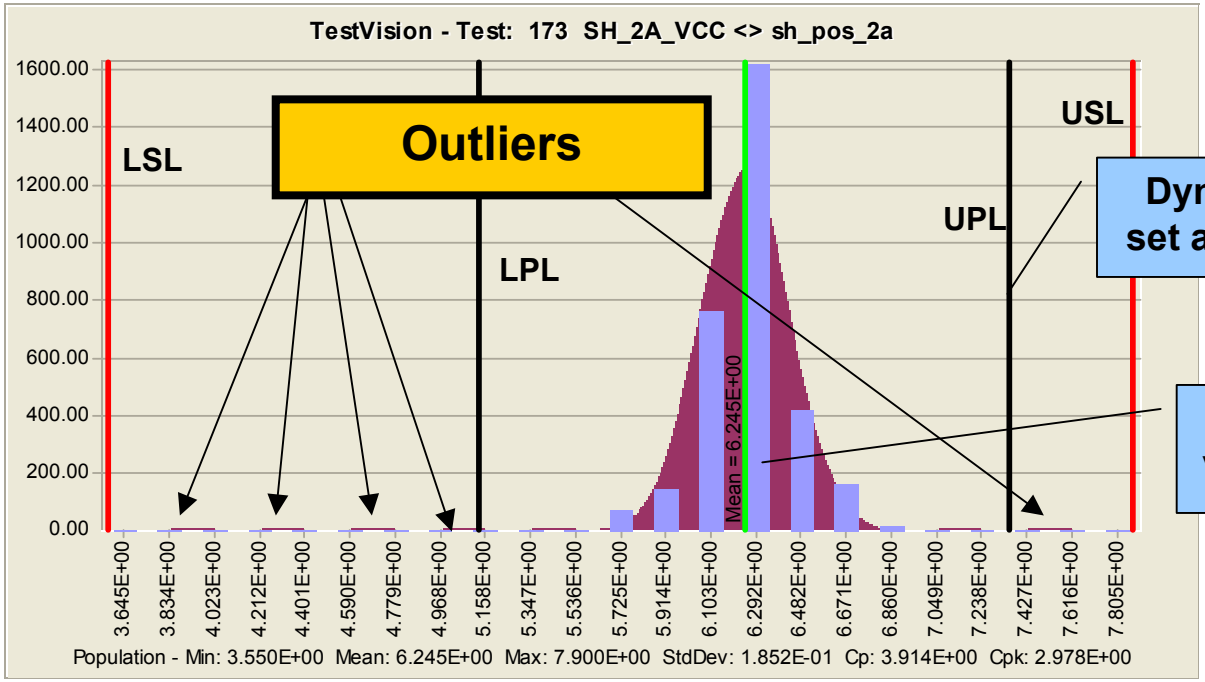
What is PAT, anyway?

Reject any parts that behave differently than their siblings

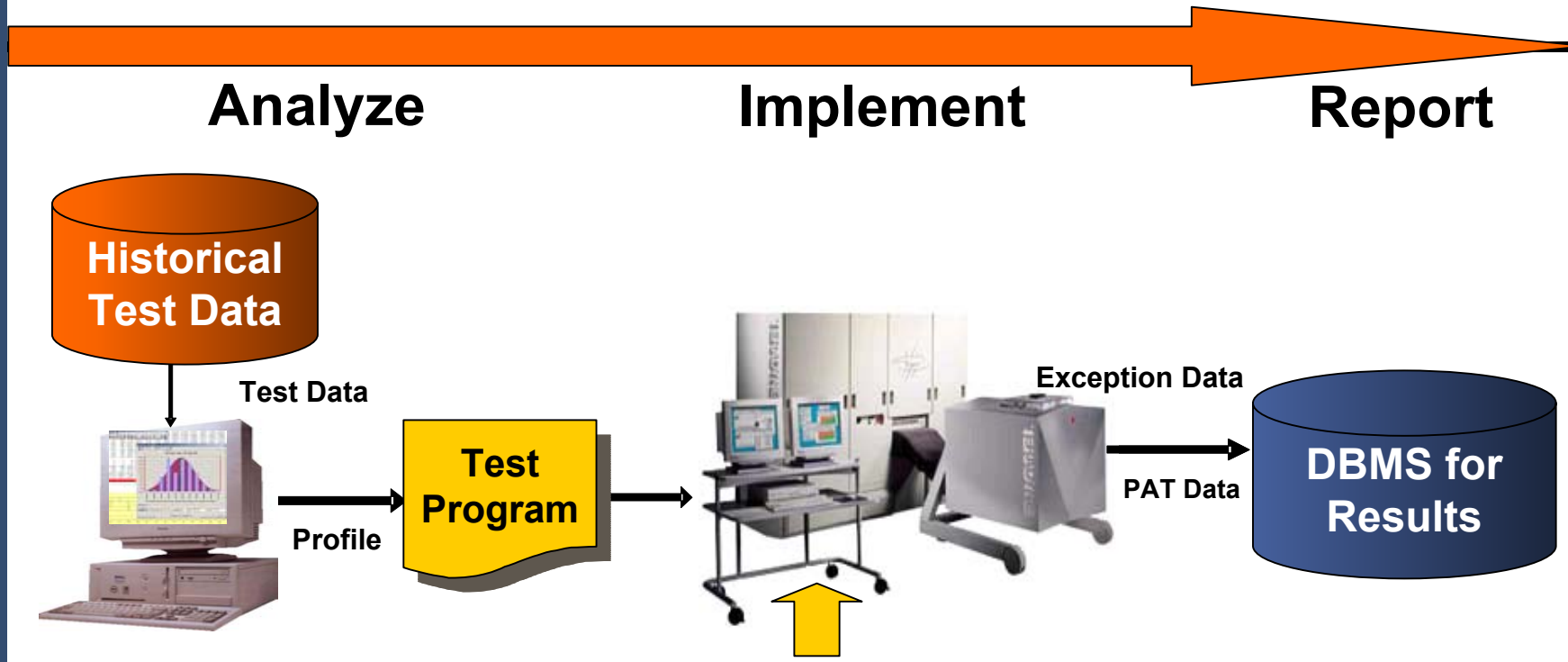


Dynamic PAT limit set as Nσ from mean

Distribution varies by lot

Fail Bin in Test Program | **PAT Bin** | **Pass Bin in Test Program** | **PAT Bin** | **Fail Bin in Test Program**

Steps for Real-Time PAT



- Off-tester Analysis
- Static & Dynamic PAT
- Simulate production
- Tweak recipe

- On-tester solution
- Real-time Dynamic PAT bins devices as testing occurs
- Works for probe and final/package test

- Web-based dashboard
- Exception data
- Data warehouse

PAT Analysis

- Import tester data into analysis tool
- Select tests or all tests for calculations
  - Static PAT limits
  - Dynamic PAT limits
- Select tests or all tests for simulation and reporting
  - Dynamic PAT outliers shown and reported
  - Tweak recipe for production to maximize coverage and minimize yield loss
- Use graphical tools to display dynamic PAT limits and make intelligent decisions about setup

Example PAT Simulation Results

Test #	Test Description	LoLimit	HiLimit	Scal	Unit	Cp	Cpk	Sigma	Mean	PAT Outliers
38.0000	1_BIAS_PWDW <> iq	0.0001	0.0015	m	a	68.548	51.516	3.40393E-06	0.000626073	0
39.0000	2_IVCC1_PWD <> iq	-2.50E-04	0.0015	m	a	39.711	39.711	7.34391E-06	0.000625097	1
40.0000	3_BIAS_TRI <> iq_on	0.0001	0.0018	m	a	51.345	47.762	5.51825E-06	0.000890682	0
41.0000	4_VCC_TRI <> iq_on	0.012	0.029	m	a	5.953	5.925	0.000475924	0.02054009	0
42.0000	L_LEAK_P17 <> iq_on	-0.000001	0.000045	u	a	22.672	1.178	3.38155E-07	1.95525E-07	1
43.0000	L_LEAK_P10 <> iq_on	-0.000001	0.000045	u	a	4.375	0.250	1.75219E-06	3.14088E-07	1
44.0000	L_LEAK_P2 <> iq_on	-0.000001	0.000045	u	a	124.713	6.046	6.14746E-08	1.15082E-07	0
45.0000	L_LEAK_P8 <> iq_on	-0.000001	0.000045	u	a	10.518	0.529	7.2893E-07	1.57887E-07	1
46.0000	H_LEAK_P17 <> iq_on	-0.000045	0.000001	u	a	243.565	11.093	3.14769E-08	-4.75314E-08	1
47.0000	H_LEAK_P10 <> iq_on	-0.000045	0.000001	u	a	1556.325	70.204	4.92614E-09	-3.75034E-08	0
50.0000	5_VCC_ON <> iq_on	0.012	0.037	m	a	7.292	6.881	0.00057142	0.025204595	0
51.0000	6_BIAS_ON <> iq_on	0.0001	0.0018	m	a	50.546	46.898	5.60545E-06	0.000888657	0
52.0000	IQ40V <> over_v	0.016	0.054	m	a	4.418	2.213	0.001433398	0.025517135	0
53.0000	FAUL_CUR_38V <> over_v	-1.02E-04	0.0001	m	a	24.874	24.874	1.35562E-06	-1.15772E-06	0
54.0000	UNDERVOLTAGE <> over_v	5.8	10		V	7.264	4.750	0.096366859	7.173235934	0
55.0000	FAULT_CURR_U <> over_v	0.0005	0.003	m	a	156.027	28.837	2.67048E-06	0.000731028	0
56.0000	7_VO1A_H <> rdson_1a	14.5	15.5		v	23.642	16.487	0.007049546	14.84868546	3
57.0000	9_RDSON_1A_P <> rdson_1a	0.11	0.38	m	ohm	12.483	9.939	0.003604955	0.272515603	0
58.0000	10_RDSON_1A_N <> rdson_1a	0.11	0.38	m	ohm	16.781	16.582	0.002681644	0.243402867	0
59.0000	11_VO1B_H <> rdson_1b	14.5	15.5		v	68.517	57.817	0.002432495	14.92192217	9
60.0000	12_RDSON_1B_P <> rdson_1b	0.11	0.38	m	ohm	14.847	11.723	0.003030851	0.273404734	0
61.0000	13_RDSON_1B_N <> rdson_1b	0.11	0.38	m	ohm	17.275	16.987	0.002604885	0.242748273	0
62.0000	14_VO2A_H <> rdson_2a	14.5	15.5		v	34.985	28.055	0.004763946	14.90095466	4
63.0000	15_RDSON_2A_P <> rdson_2a	0.11	0.38	m	ohm	15.298	11.296	0.002941584	0.280312054	0
64.0000	16_RDSON_2A_N <> rdson_2a	0.11	0.38	m	ohm	17.152	16.935	0.002623648	0.243296778	0
65.0000	17_VO2B_H <> rdson_2b	14.5	15.5		v	74.693	61.330	0.00223137	14.910549	1
66.0000	18_RDSON_2B_P <> rdson_2b	0.11	0.38	m	ohm	15.651	11.579	0.002875272	0.280124005	0
67.0000	19_RDSON_2B_N <> rdson_2b	0.11	0.38	m	ohm	17.026	16.765	0.002643068	0.242933541	0
68.0000	19_MAT_CH1_P <> rdson_2b	0.955	1.045	%	%	2.021	1.875	0.007421154	0.996749345	0
69.0000	19_MAT_CH1_N <> rdson_2b	0.955	1.045	%	%	11.880	11.169	0.001262627	1.002694218	0
70.0000	19_MAT_CH2_P <> rdson_2b	0.955	1.045	%	%	6.369	6.273	0.002355335	1.00067163	3
71.0000	19_MAT_CH2_N <> rdson_2b	0.955	1.045	%	%	12.317	11.907	0.001217826	1.001496997	3
72.0000	IQ_OP_20V <> time_1	0.045	0.088	m	a	3.830	3.330	0.00187126	0.069305493	0
73.0000	IQ_OP_30V <> time_1	0.055	0.125	m	a	8.534	7.989	0.00136703	0.092237623	0
74.0000	PULSE_CH1A <> time_1	7.30E-08	1.20E-07	n	S	5.783	4.121	1.35448E-09	8.97437E-08	0

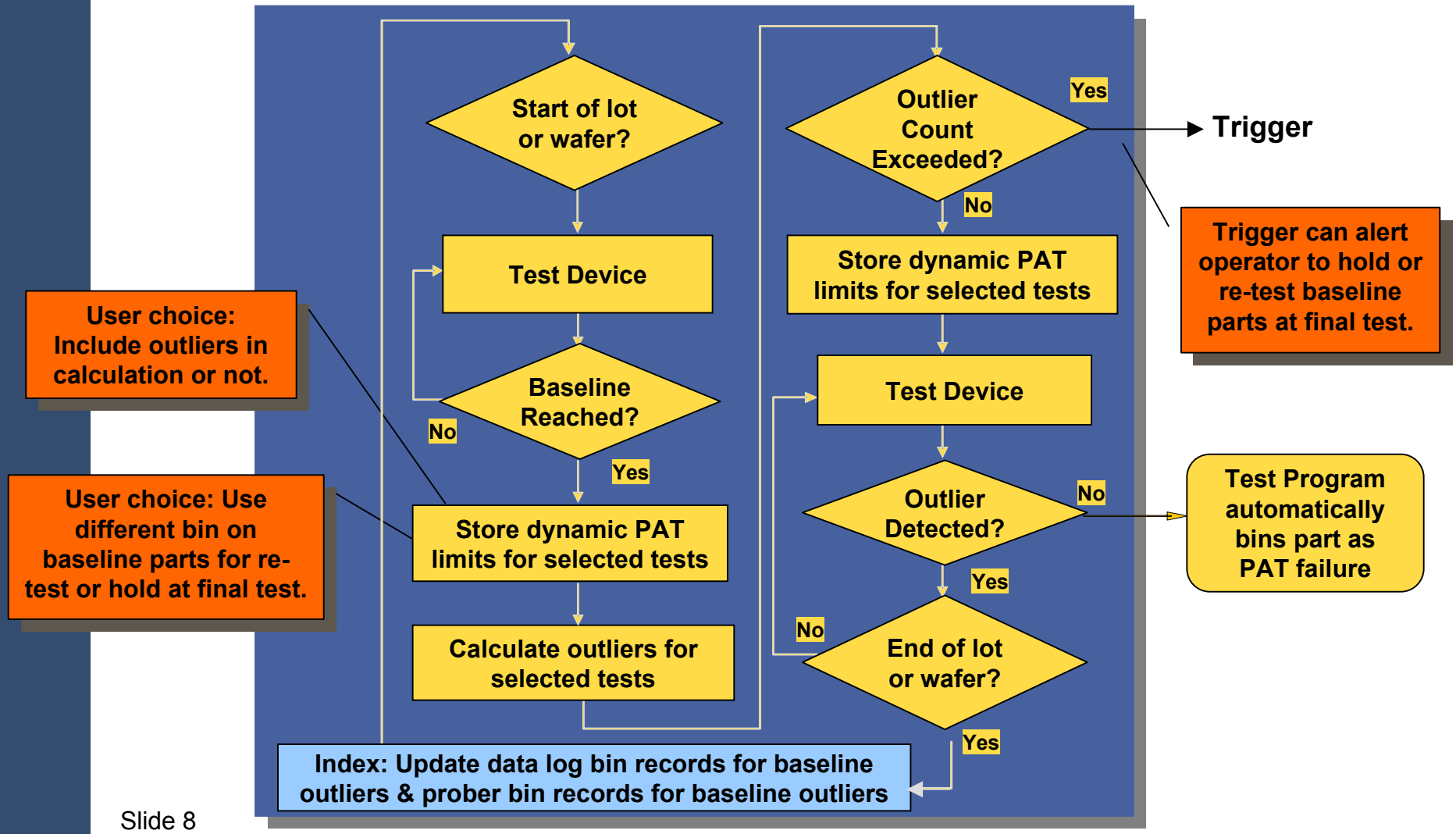
Real-time, dynamic PAT Implementation

- Follow AEC – Q001 rev C specification
- Must offer great flexibility in setup
- Dynamic PAT limits calculated at baseline using Mean +/- (n * Sigma)
- Offer simple test program preparation
- PAT binning applied in real-time
  - Unique “outlier” software and hardware bin
  - Tester data log file will include outlier binning
  - Works at probe or package test
  - No test time overhead
- Outlier count trigger and summary reporting for traceabilility

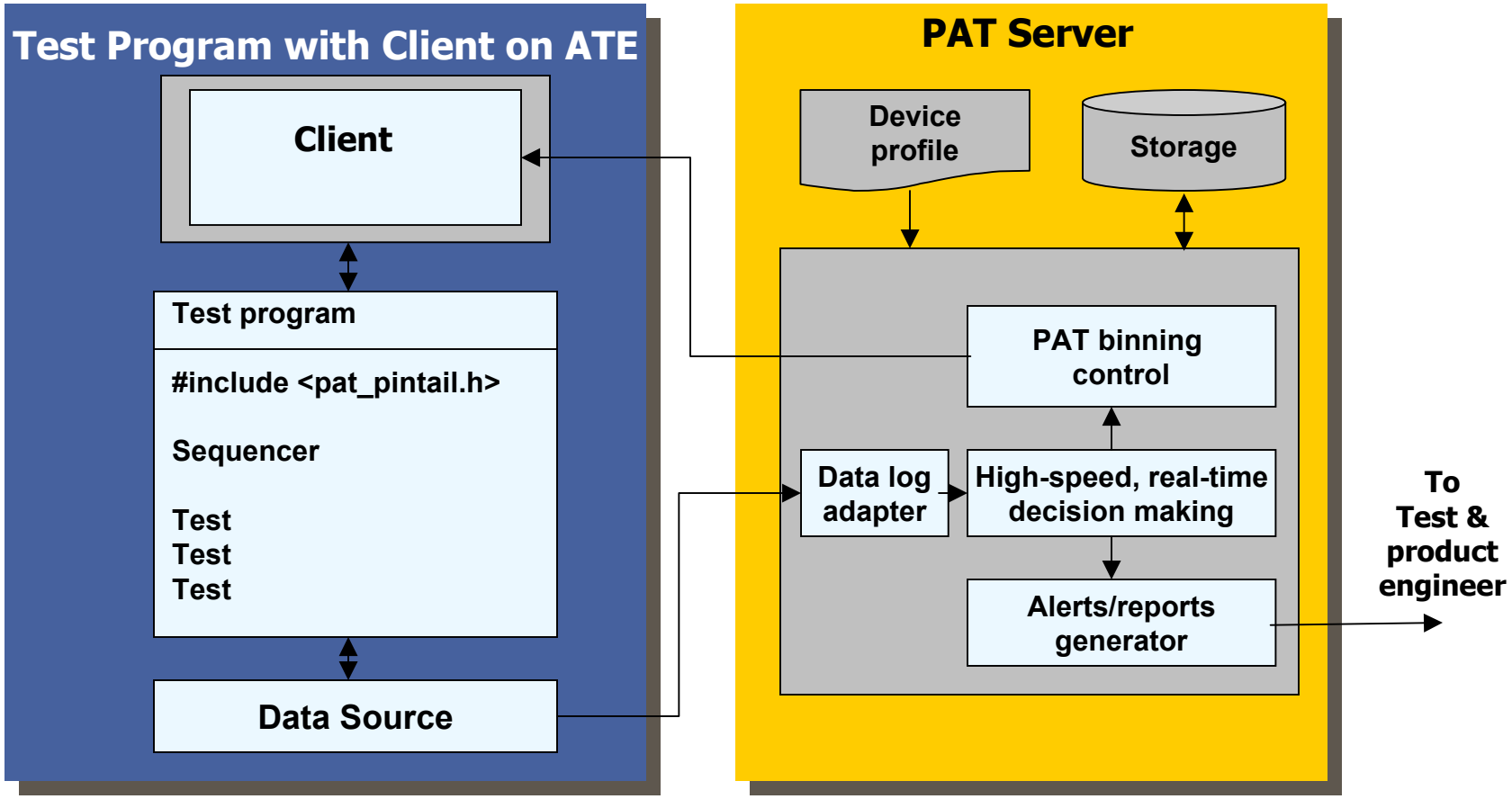
Implementation Configuration

- Select tests for dynamic PAT
- Establish number of standard deviations for PAT limits
- Set PAT baseline for statistical soundness
  - Individual test must reach baseline before dynamic PAT limits are applied
  - Use or eliminate baseline outliers in dynamic PAT calculation
  - Perform normalcy check at baseline
  - Optionally use robust or Johnson method if distribution is not normal
- Setup threshold for number of outliers at baseline
- Set PAT outlier hardware and software bins
  - Baseline parts can be binned out differently

Example Real-Time Process Flow



Example Real-Time Architecture



Test Program Modifications

Simple PAT test limit and binning entries

```
SEQUENCER voltage_tests()
{
  seq test_one()    $10  > 4.500v      < 6.000v      "5v@50ma"      f(2);
  seq test_two()    $20  > 4.500v      < 6.000v      "5v@50ma"      f(3);
  seq test_three()
  {
                    $30  > 4.500v      < 6.000v      "5v@50ma"      f(4);
                    > (patLSL(30))  < (patUSL(30))  "5v@50ma"      f(40);
  }
  seq test_four()   $40  > 4.500v      < 6.000v      "5v@50ma"      f(5);
  seq test_five()
  {
                    $50  > 4.500v      < 6.000v      "5v@50ma"      f(6);
                    > (patLSL(50))  < (patUSL(50))  "5v@50ma"      f(60);
  }
  seq test_six()    $60  > 4.500v      < 6.000v      "5v@50ma"      f(7) p(patPassBin(1,100));
}
```

Simple PAT test result entries

```
TESTF test_three()
{
                set  meter input : src = 2 : v;
                result = read_meter();
                patTest(result);
)
```

- **No test flow changes**
- **No correlation required**

Example Reporting Requirements

PAT Report

- Lot summary
- PAT summary
- Trigger activity
- Device profile summary
- Hardware bin summary
- Software bin summary

Header Information

Detail

PAT-Enabled Tests

T#	sT#	Units	Description	Baseline Device	% Yield Loss	Baseline Outlier Count	Total Outlier Count	LSL	USL	Lower PAT Limit	Upper PAT Limit	Baseline Mean	Baseline STDev	Robust Sigma Used
150	0	a	4_VCC_TRI <> iq_on	83	0.00%	0	0	0.0125a	0.0280a	-8.1434E-3a	0.0509a	0.0214	0.0045	FALSE
120	0	a	1_BIAS_PWDW <> iq	79	0.20%	0	2	0.0001a	0.0014a	0.0006a	0.0007a	0.0006	2.85E-06	FALSE
420	0	v	17_VO2B_H <> rdson_2b	84	0.49%	0	5	14.6000v	15.40v	14.9734v	14.9808v	14.9771	0.0006	FALSE
330	0	v	7_VO1A_H <> rdson_1a	84	0.00%	0	0	14.6000v	15.40v	14.9564v	14.9686v	14.9625	0.0009	FALSE
350	0	ohm	10_RDSON_1A_N <> rdson_1a	84	0.20%	0	2	0.1150ohm	0.3600ohm	0.1788ohm	0.1933ohm	0.1861	0.0011	FALSE
440	0	ohm	19_RDSON_2B_N <> rdson_2b	84	0.20%	0	2	0.1150ohm	0.3600ohm	0.1779ohm	0.1923ohm	0.1851	0.0011	FALSE
460	0	%	19_MAT_CH1_N <> rdson_2b	84	0.30%	0	3	0.96%	1.04%	0.98%	1.02%	1.0006	0.0027	FALSE
470	0	%	19_MAT_CH2_P <> rdson_2b	84	0.10%	0	1	0.96%	1.04%	1.00%	1.03%	1.0124	0.0021	FALSE
480	0	%	19_MAT_CH2_N <> rdson_2b	84	0.20%	0	2	0.96%	1.04%	0.99%	1.01%	0.9973	0.0016	FALSE

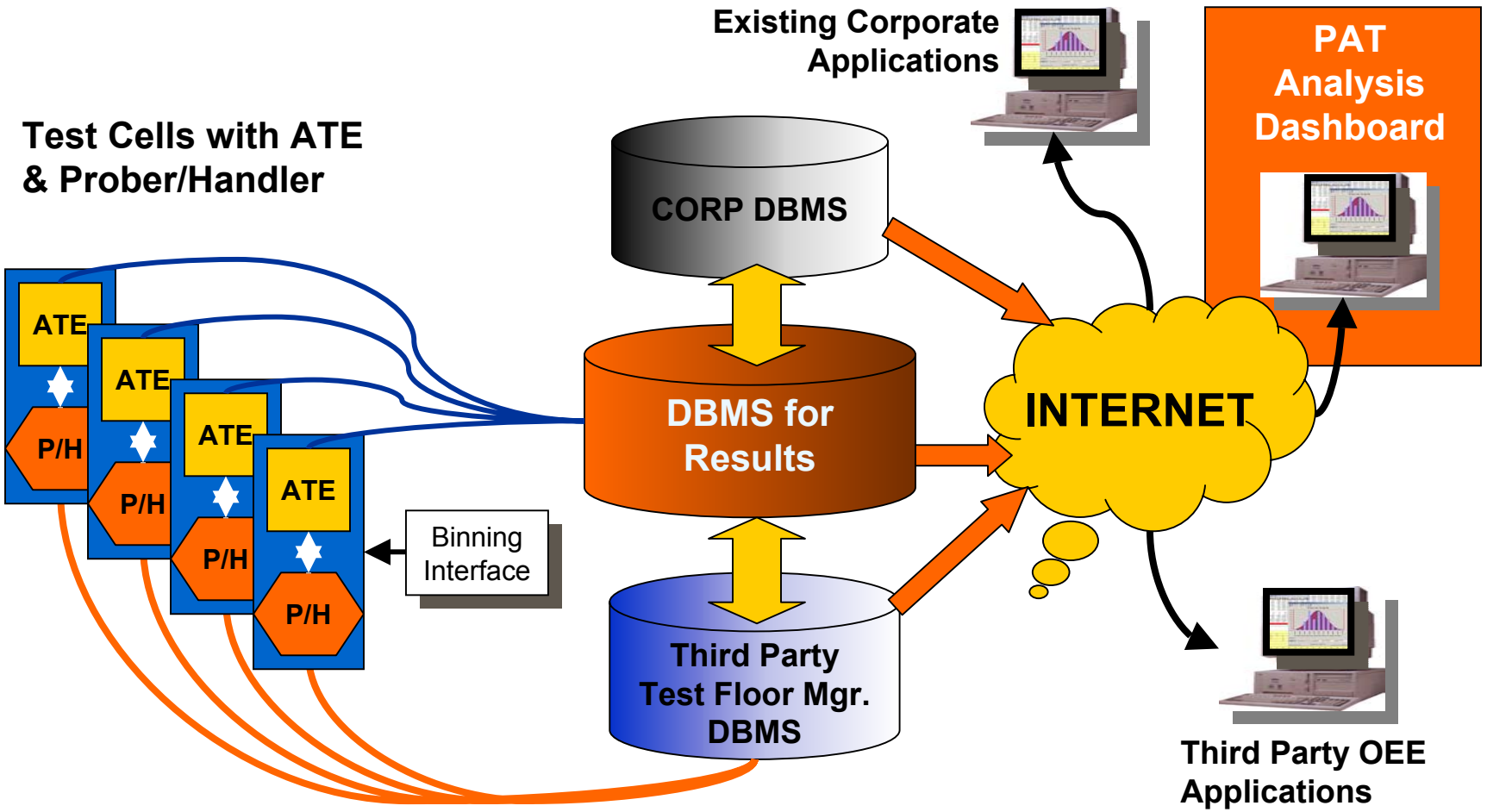
Advantages of Real-Time PAT

- **No post processing is necessary for PAT outliers.**
  - **No reduction in tester throughput.** Post processing requires 100% data logging which can **double** the test time
  - **No expensive DBMS** and IT structure for storing and processing huge data files – this can cost **MILLIONS!**
  - Existing tools for yield analysis and Fab process feedback can still be used.
  - No complicated algorithms, additional software or setup.
- **Real-time monitoring of each PAT test result produces alerts and exception reporting.**
  - Catastrophic problems alert immediately, e.g. bad probe card.
  - Alert product engineers to problem tests or maverick lots and pinpoints the problem area.
  - Exception data is 10,000 times smaller than normal data log.

Advantages of Real-Time PAT

- **Devices having PAT failures are binned out on-the-fly to a user settable "outlier" bin.**
  - Parametric data goes directly to real-time statistical engine
  - Tester data log files automatically contain the correct dynamic PAT binning
  - Tester data log can be sampled or eventually turned off
  - Prober binning map is automatically updated during testing
- **Single solution for both probe and package test**
  - Consistent dynamic PAT process at probe and package test
  - Real-time is the ONLY solution for PAT at package test!

Integrating Dynamic PAT Into Your IT



Dynamic PAT Benefits

- Predictive analysis and simulation make setting up test list and recipe for PAT easy
- Works in real-time at probe and package test
  - Tester data log file contains PAT binning
  - Unique “outlier” software and hardware bin
- Independent of tester platform
- Simple test program preparation
- No increase in test time
- **Complete PAT solution**

Questions to ponder…

- What about post processing?
- Could a real-time process be adapted to post processing?
- What about regional PAT?
- What about system overhead?
- What about coverage versus yield loss, and can I intelligently make test selections?