OPTIMUM

Wafer to Thermal Chuck

INTERFACE

SWTW 2005

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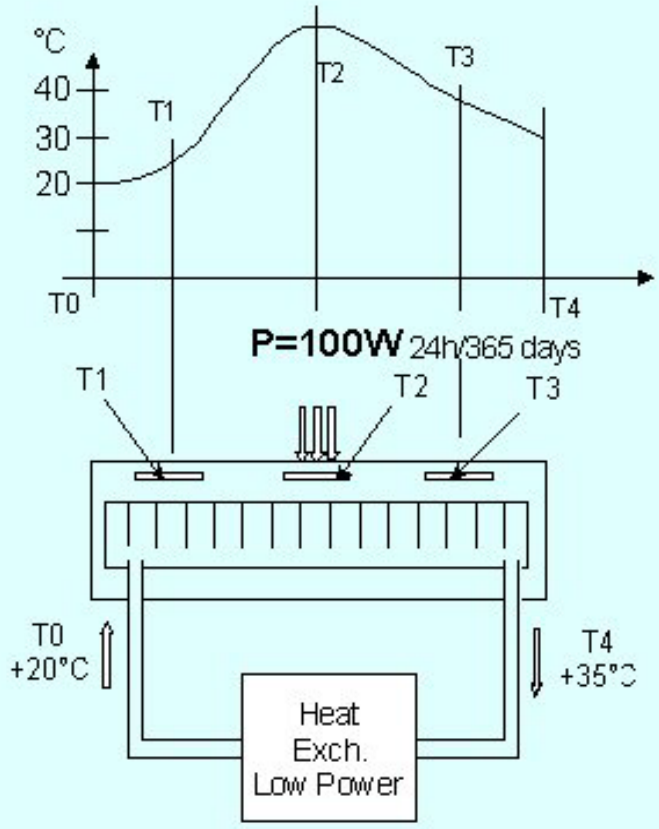
Klemens Reitinger ERS GmbH

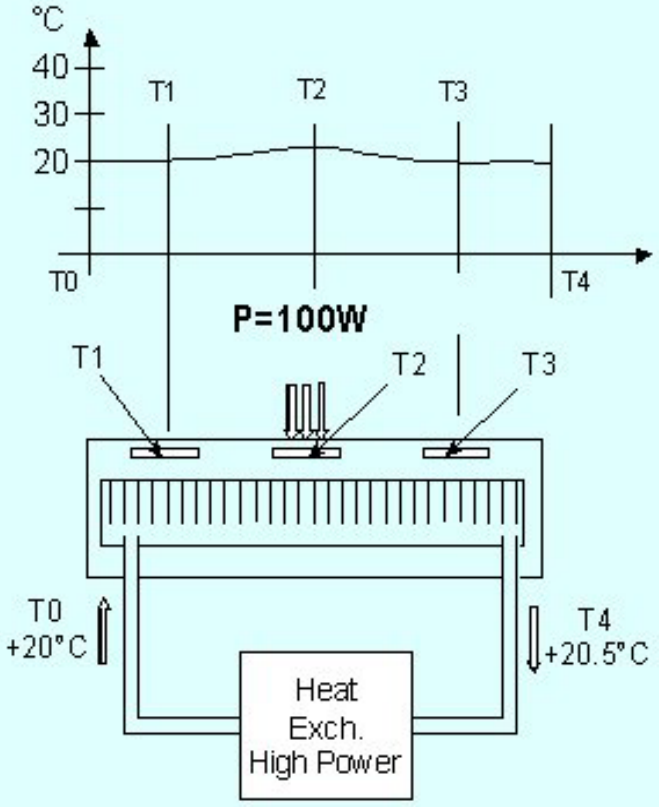

DANGER
HIGH POWER

Standard Chuck Design



0.15°C/W

High Power ERS Chuck Design



0.0054°C/W

Outline

- Challenge
- Mission
- Theoretical Background
- Methods used in the past and their limitations
- Current Capabilities
- Summary
- Alternate Future Trends
- Reference

The Challenge

- **High Power measurements with the goal of keeping Chip temperature constant**
- **The developed heat needs to be dissipated instantaneously for accurate measurements and to prevent damage to the structures involved**
- **Thermal Resistance between Wafer and Chuck needs to be kept at a minimum**

The Mission

Rt k=0

Theoretical Background

(from a chuck manufacturers perspective)

- **For accurate measurements the Thermal Resistance value between Wafer and Chuck needs to be:**

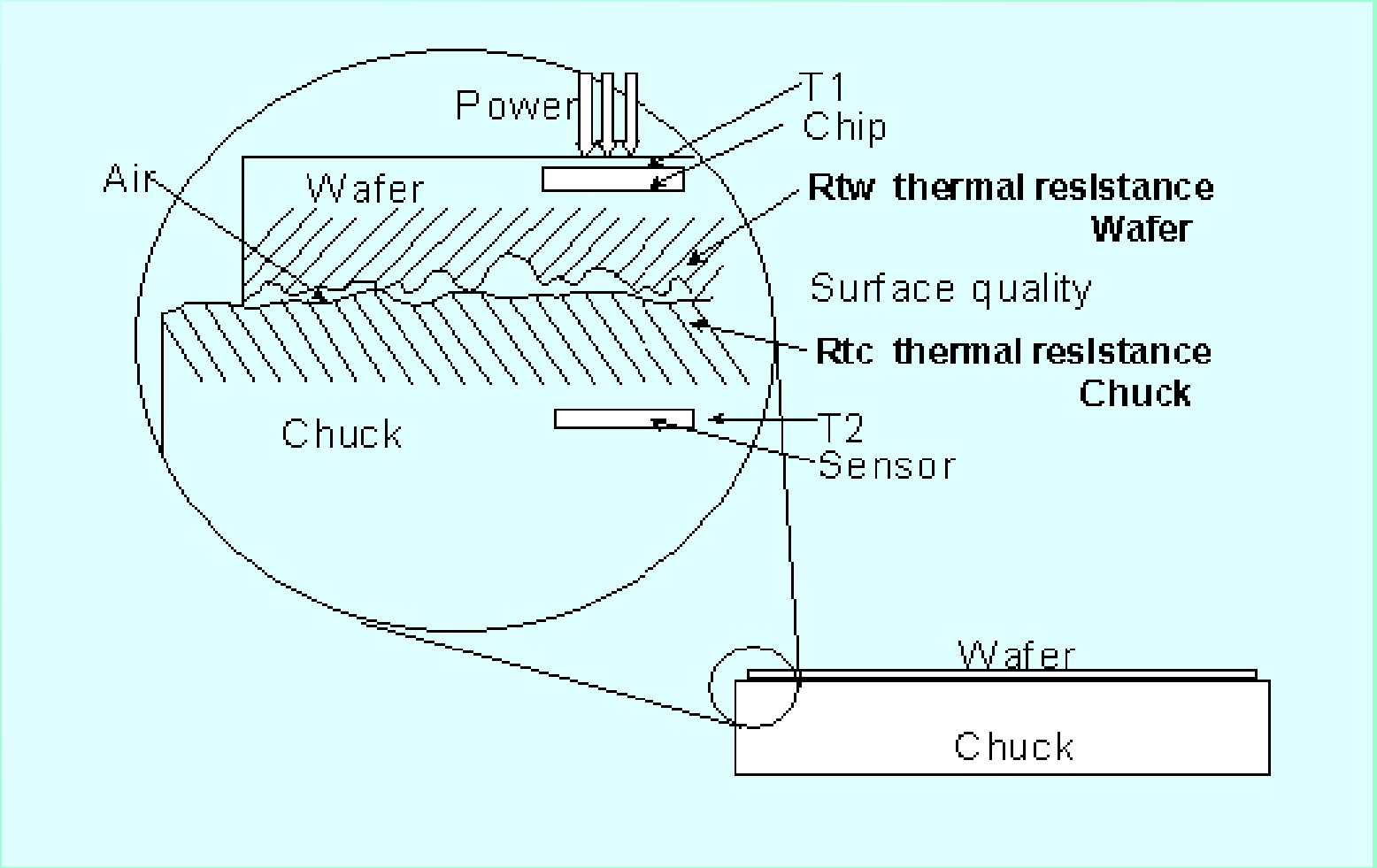
  k=0 °C/W.

- **This is not attainable, therefore a Rt value k<0.1 °C/W is desirable**

- **Main Influence on Thermal Resistance IS Surface Quality of BOTH Wafer Backside and Chuck Top**

- **HIGH POWER applications need the best surface quality!**

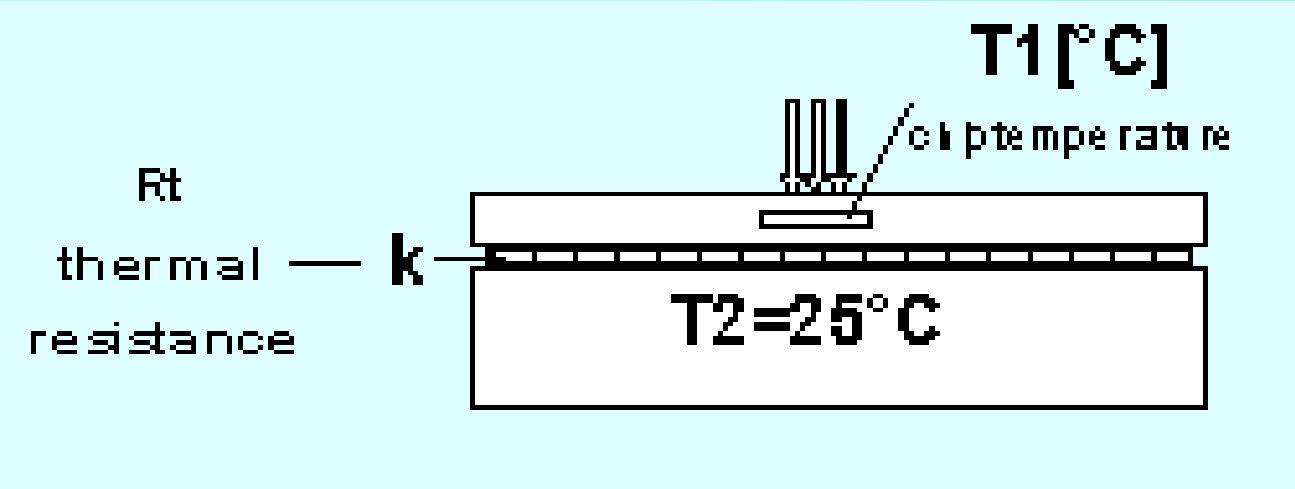
Rt = Rtw + Rtc


Power
T1
Chip
Air
Wafer
Rtw thermal resistance
Wafer
Surface quality
Rtc thermal resistance
Chuck
Chuck
T2
Sensor
Wafer
Chuck

Calculating Chip Temperature from Applied Power

under ideal conditions:

(T1-T2) / Power = k (°C/W)



Therefore: Chip Temperature (T1) =
Chuck Temperature (T2) + (Chip Power X Thermal Resistance k)

Other Influences:

- Probecard also dissipates power
- Chip Size and Power input are related
- Vacuum is generally a negative though necessary influence – best results have been obtained with a probe force of >3kg per 10mm x 10mm
- Formula is based on ideal conditions – Environment matters

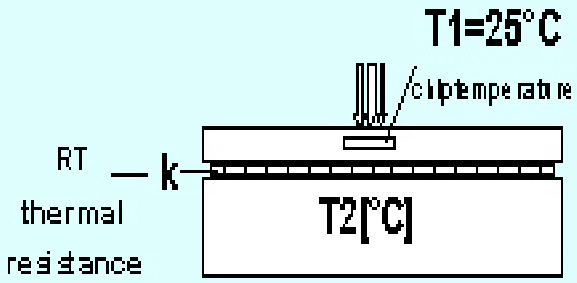
Keeping Chip Temperature Constant

a) Bad Thermal Contact (k=1)
Very low Chuck temperature is necessary

b) Good Thermal Contact (k<0.1)
Higher Chuck temperature is possible

Typical values:

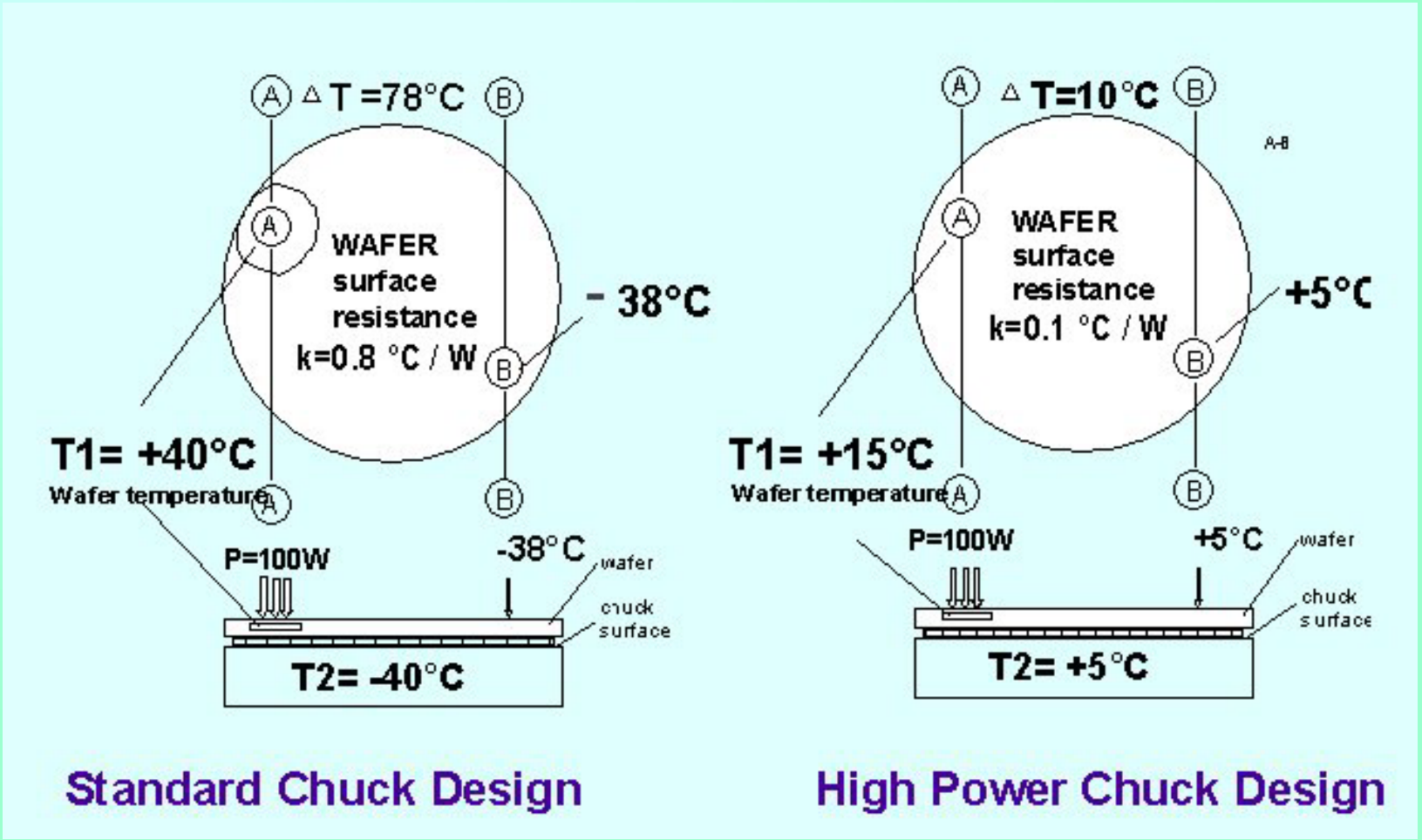
Standard Wafer k~0.3 °C/W
ERS Chuck k~0.08 °C/W



Thermal resistance factor k*	Chip temperature constant T1	at P100W Chucktemp T2	at P 200W Chucktemp T2
0.1	+25°C	+15°C	+5°C
0.3	+25°C	-5°C	-35°C
0.5	+25°C	-25°C	-75°C

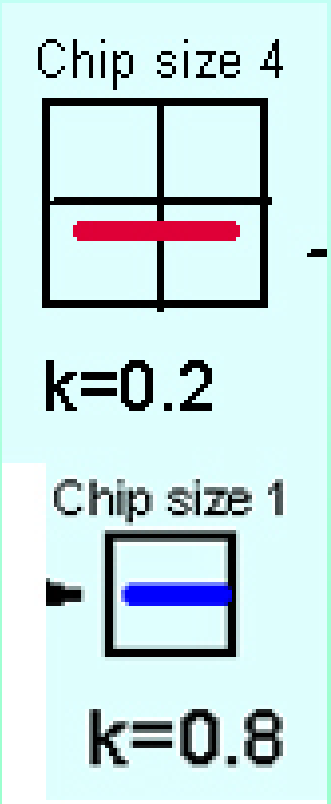
*Chip size = constant

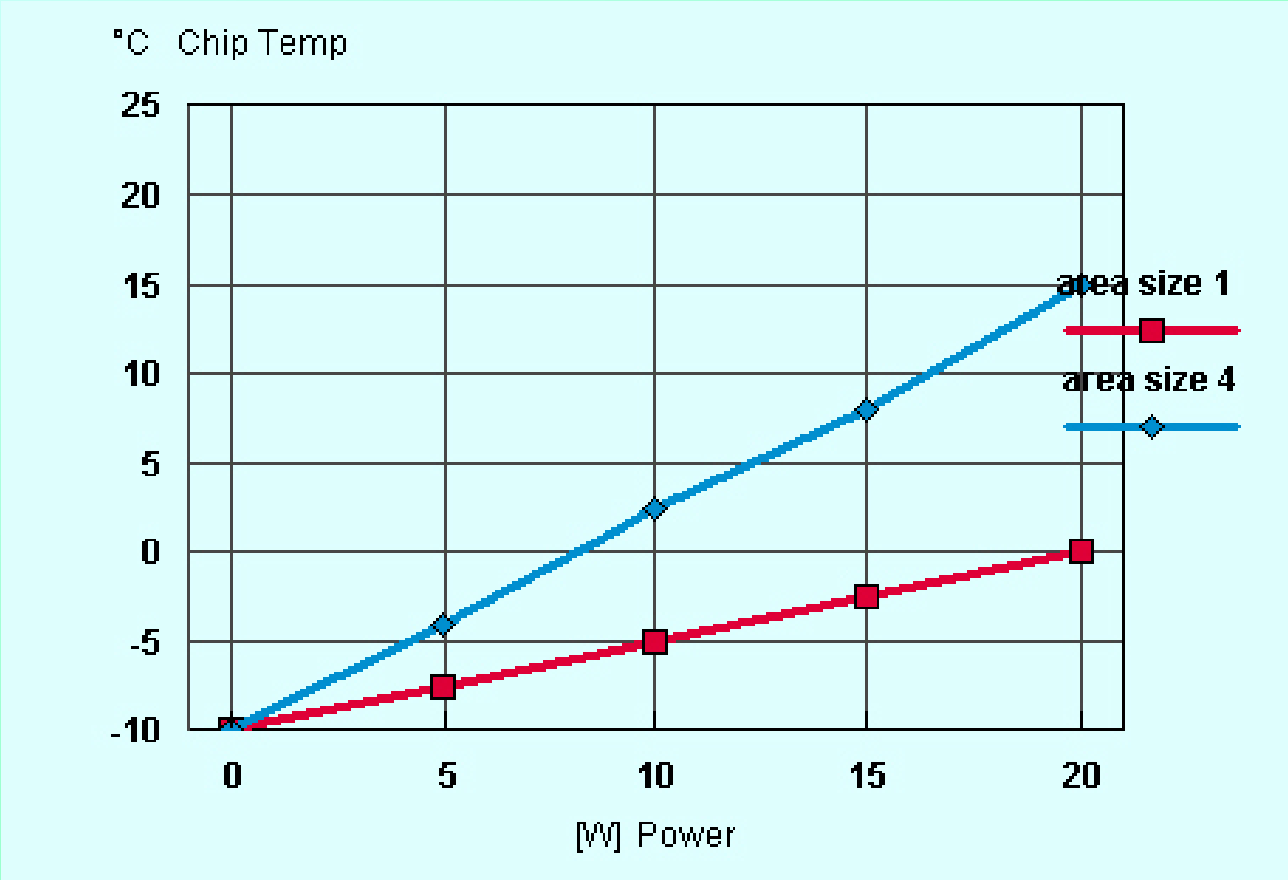
Wafer Backside Surface Influence



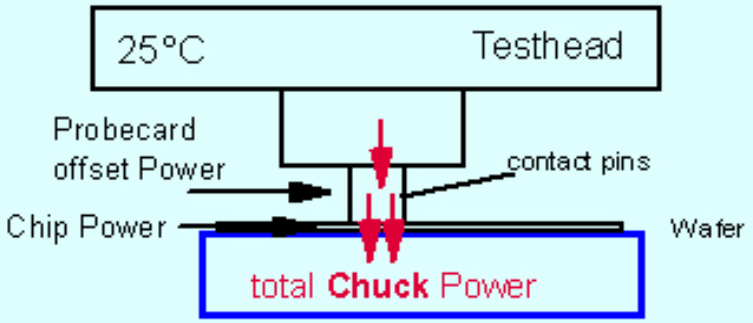
Influence of Chip Size

with Constant Surface Thermal Quality





typical values for total power input at different test temperatures and the resulting chip temperatures



Chip ** Temp [°C]	Chip Power [W]	Probecard* Power [W]	CHUCK Total Power [W]	CHUCK Temp [°C]	dT[°C] Chip/Chuk	total k Chip [K/W]
40	200	-7!	193	35.0	7.0	0.035
25	200	0	200	14.5	10.5	0.053
10	200	7	207	-4.5	14.5	0.075
0	200	12	212	-17.0	17.0	0.085
-10	200	17	217	-30.0	20.0	0.100
-20	200	21	221	-42.0	22.0	0.110
-30	200	26	226	-55.0	25.0	0.125

**chip size=constant *Probecard type constant K dT Chip/Chuck to Chuck power = constant (K=0.53)

Ancient Solutions for low Rt

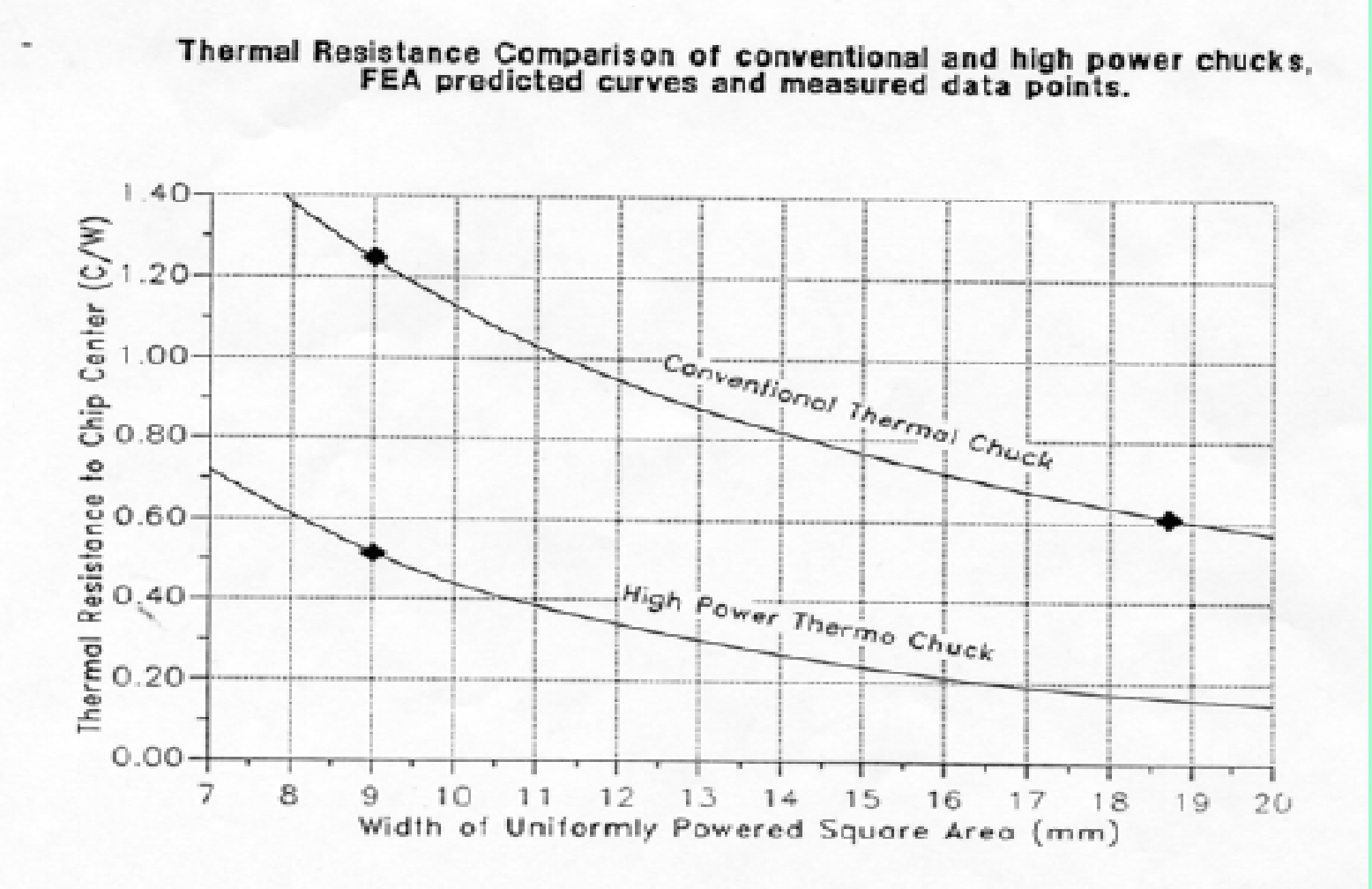
- **Have shown an improvement in decreasing the thermal resistance but at the same time added another layer of resistance between Chuck top and Wafer (though preferable over a void)**
- **Media included helium, liquids and similar**
- **Rtw + (Rtm) + Rtc = Rt**
- **This is not the ideal way to increase conductivity / decrease resistance**

Helium

- Added in the cavity between Chuck and wafer has shown a 20% increase in conductivity

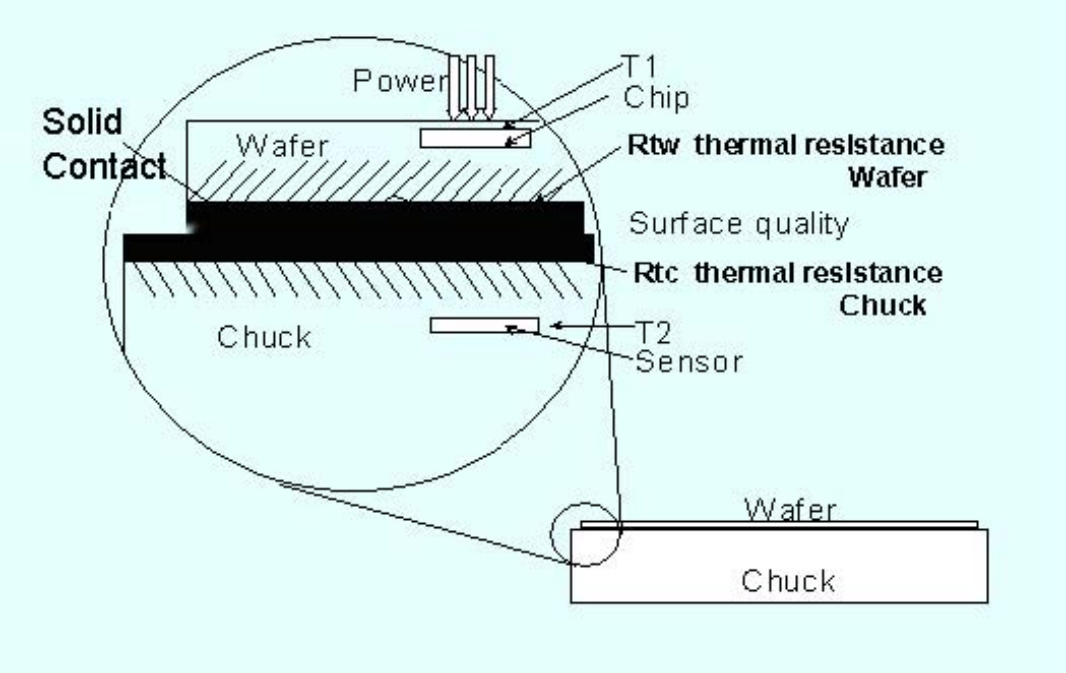
Picture Source:
Thermo Chuck by Temptronic. “Scotty, I need more Power”
Dale Slaby, Cray Research
9/12/1998

SWTW 1997 "Wafer Temperature Control for Testing High Power Chips: Measured Thermal Performance" by Dave Gardell, IBM Corp, 963G



WE PROPOSE:

- **HIGH POWER applications NEED the BEST surface quality!**



ERS Test Chip

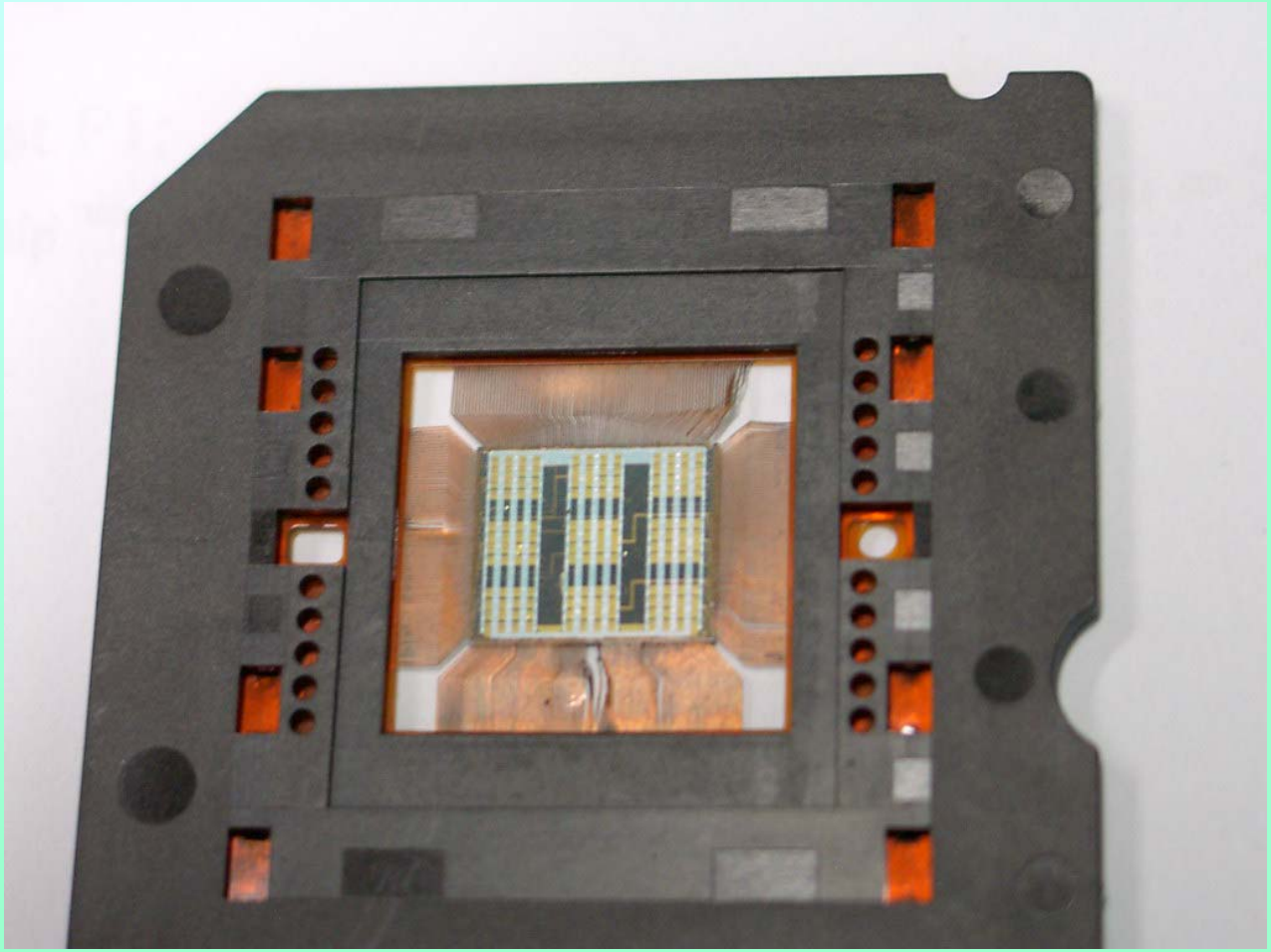
10mm x 10mm

subdivided in 9 segments

Individual Thermal load resistors and diodes for temperature sensing

Segments can be queried individually for measuring temperature on the outside and center of chip

ERS Test Chip



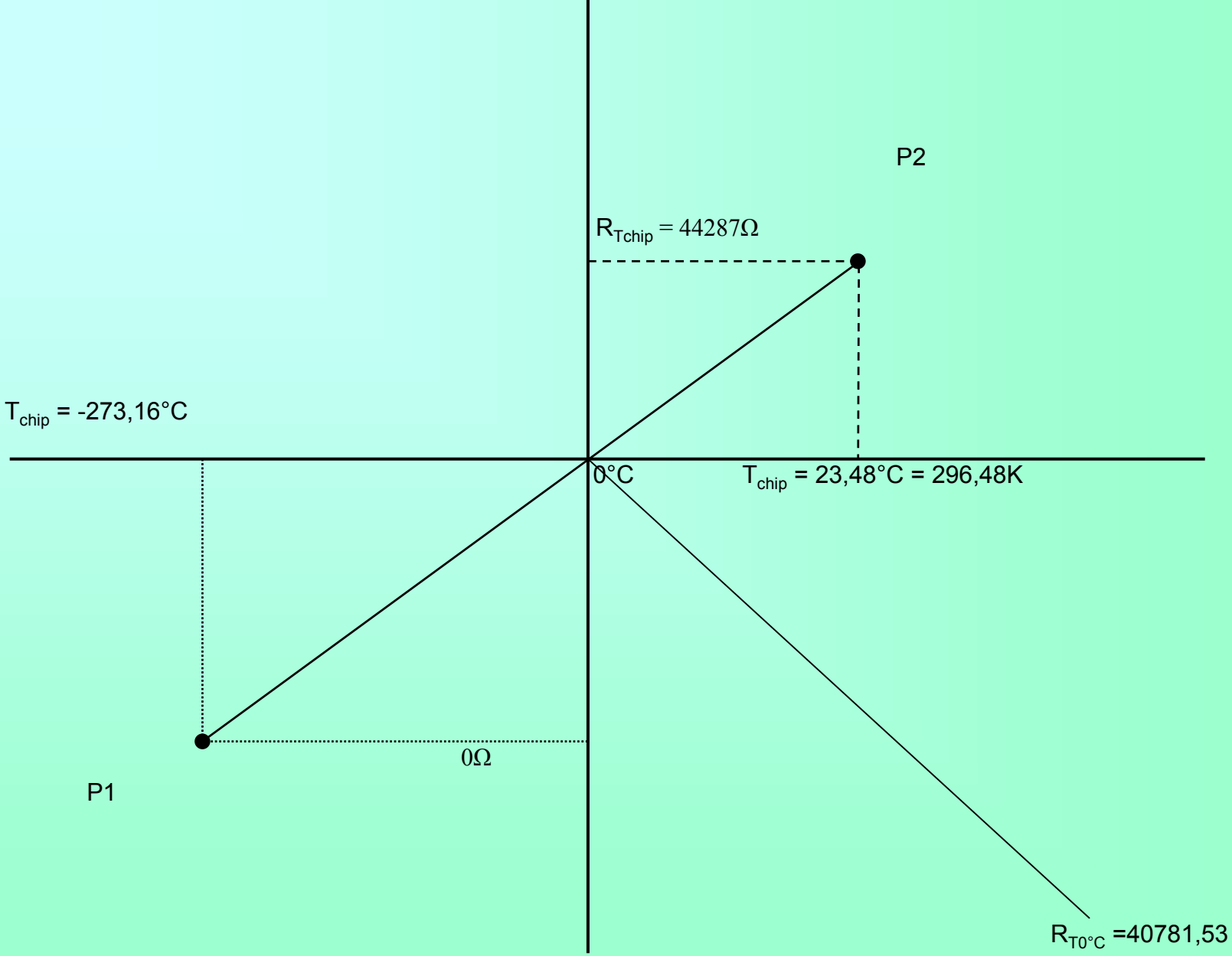
Calculating Chip Temperature

- **Determine resistance of the temperature dependent Rt Chip.**

- **Cross reference Rt Chip with temperature value**
- **Determine RTchip through 2-point procedure**

- **P1: RTchip absolute 0 = -273,16°C = 0Ω = R0**
- **P2: RTchip with ambient* T2= 23,48°C = 44287Ω**

***(arrived at on a copper block with temperature sensor at room temperature =T2)**


P2
R_{Tchip} = 44287Ω
T_{chip} = -273,16°C
0°C
T_{chip} = 23,48°C = 296,48K
0Ω
P1
$R_{T0°C}$ =40781,53

In Kelvin

P1: $T_0 = -273{,}16\text{K}$

$R_0 = 0\ \Omega$

P2: $T_{Rt} = 296{,}48\text{K}$

$R_t = 44287\ \Omega$

$$a = \frac{\Delta R}{\Delta T} = \frac{R_0 - R_t}{T_0 - T_{Rt}} = \frac{0 - 44287}{0 - 296{,}48} = 149{,}2954$$

In Degree Celsius

$R_{T0°C} = 0°C - a * T_0$

$R_{T0°C} = 0 - 149{,}2954 * -273{,}16 = 40781{,}53\ \Omega$ bei 0°C

R_{TChip} bei 0°C = 40781,53 Ω = R_{T0}

$T_{Chip} = (R_{Chip} - R_{T0}) / a$

Test P1:

$T_{Chip} = (44287 - 40781{,}53) / 149{,}2954 = 23{,}48°C$

Measurements with ERS Test Chip 10mm x 10mm

- Measured Chip Temperature no Power: **0Watt T1 = 25,5°C** (=Chuck temperature)
- Measure Chip Temperature with Power **60Watt T1 = 47,1°C**
- **Δt 47,1°C –25,5°C = 21,6°C**
- K = Δt /W = 21,6°C / 60W **= 0,36 °C/W** for a Chip with an area of **100mm²**
- Chip Powered Square Area **10mm**

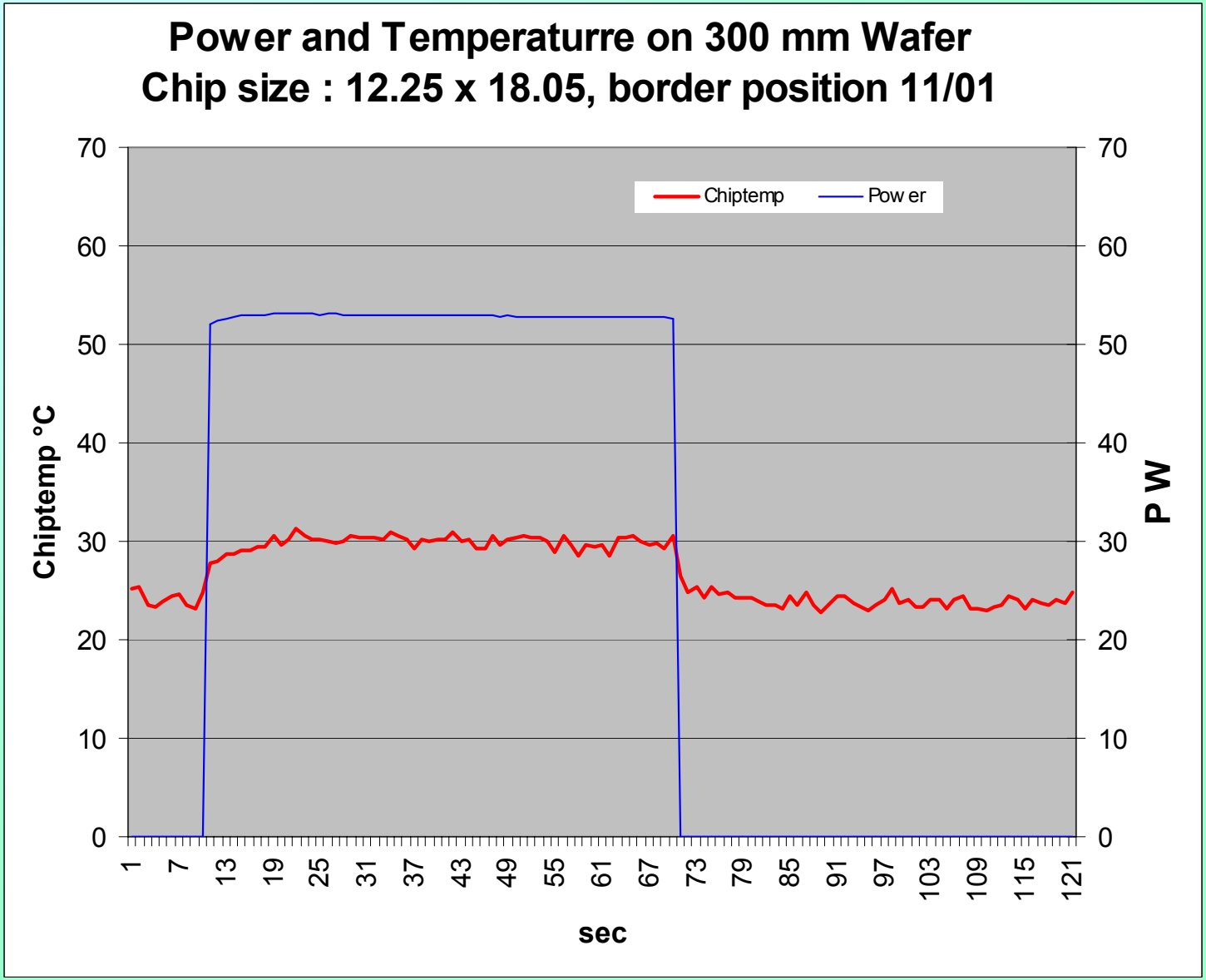
K=0,36 °C/W

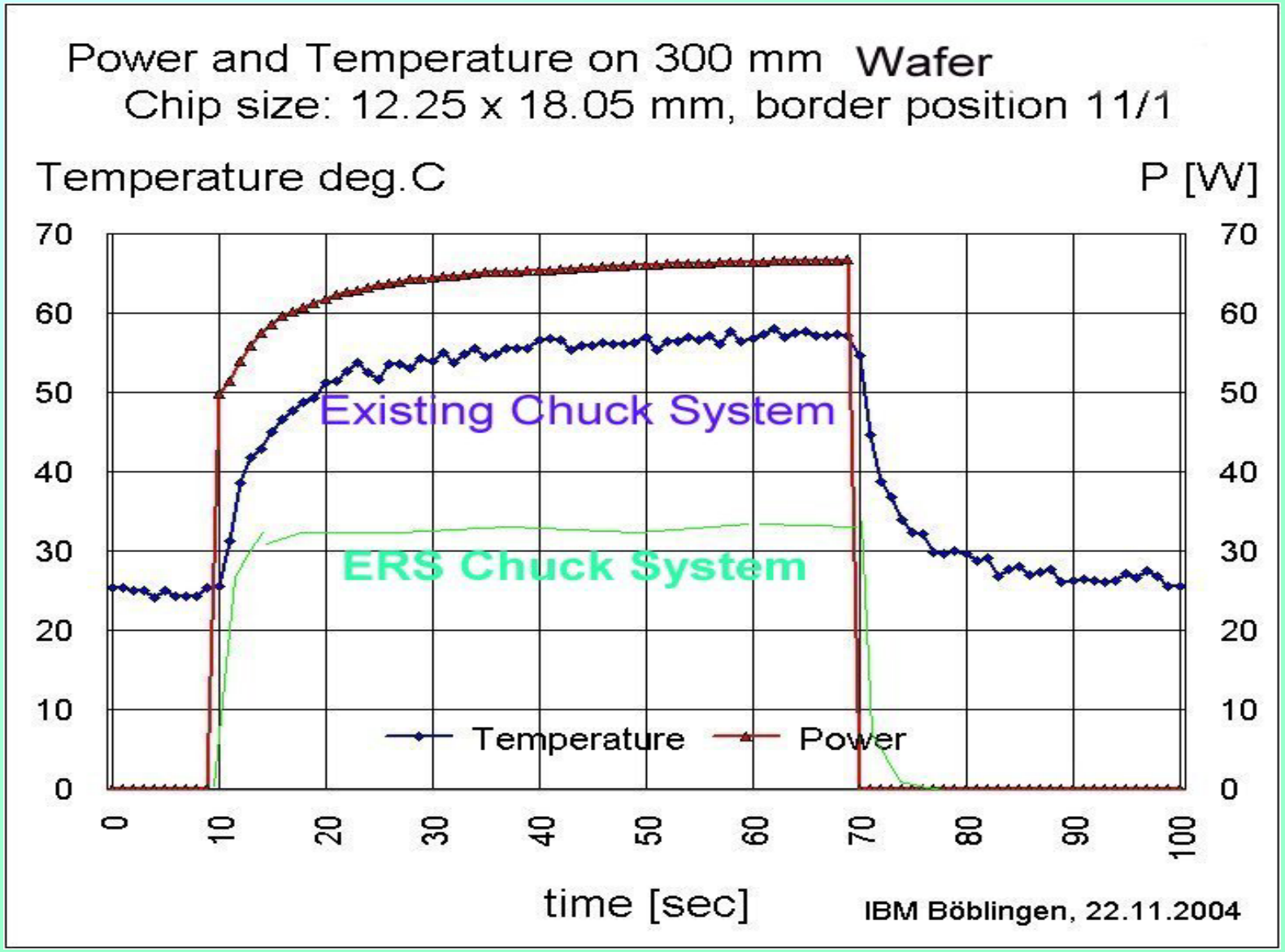
Measurement on 300mm Wafer, Chip Size 12.25mm x 18.05mm

- Measured Chip Temperature no Power: **0Watt T1 = 25,5°C**
- Measured Chip Temperated with Power: **54,6Watt T1 = 31,6°C**
- **Δt 31,6°C –25,5°C = 6,1°C**
- K = Δt /W = 6,1°C / 54,6W **= 0,11 °C/W**

  for a Chip with an area of **221 mm²**
- Chip Powered Square Area **14,8 mm**

K=0,11 °C/W


Power and Temperaturre on 300 mm Wafer
Chip size : 12.25 x 18.05, border position 11/01
Chiptemp
Pow er
Chiptemp °C
P W
sec
0
10
20
30
40
50
60
70
1
7
13
19
25
31
37
43
49
55
61
67
73
79
85
91
97
103
109
115
121


Power and Temperature on 300 mm Wafer
Chip size: 12.25 x 18.05 mm, border position 11/1
Temperature deg.C
P [W]
70
60
50
40
30
20
10
0
Existing Chuck System
ERS Chuck System
Temperature
Power
0
10
20
30
40
50
60
70
80
90
100
time [sec]
IBM Böblingen, 22.11.2004

Chip size 300mm²

=

K<0.1 °C/W

- **Chip Size 17mm x 20mm (320mm²)**
- **Chip powered square area 17.8 mm**

K= 0.07 °C/W

Current Capabilities

Summary

- **Rt = Rtw + Rtc**
- **(T1-T2) / Power = k (°C/W)**
- **T1 = T2 + (Power x k)**
- **Good Thermal Contact is k < 0.1 °C/W**
- **Chuck interior needs to be laid out for best Heat dissipation**
- **SMOOTH SURFACES (of Wafer and Chuck) ARE PARAMOUNT!**

Alternate Future Trends:

References:

Page 14: Temptronic Thermo Chuck
"Scotty I need more Power" by Dale Slaby,
Cray Research 9/12/1998

Page 15: SWTW 1997 "Wafer Temperature
Control for High Power Chips: Measured Thermal Performance" by Dave Gardell, IBM Corp, 963G

Page 27: Test data by VSLC Test Development Laboratory, IBM Boeblingen / Schoenaich 11/22/2004