Liquid Interface at Wafer Test

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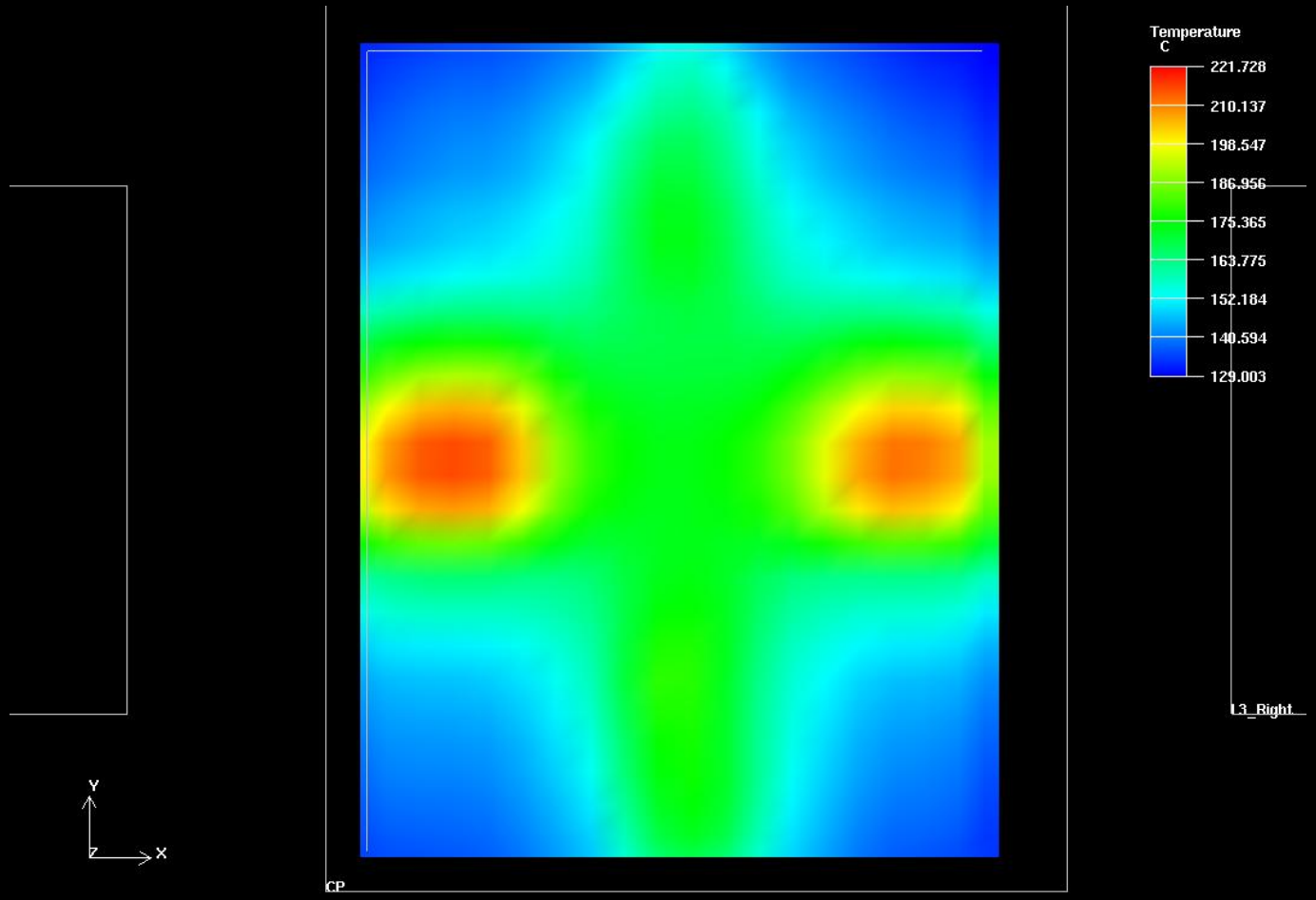
Agenda

- **Why liquid thermal interface?**
  - Existing thermal problems at module test
  - Thermal roadmap
  - Predicted thermal problems at wafer test
- **Proposed solution**
- **Predicted benefit from lower resistance**
- **Results of hardware development effort**

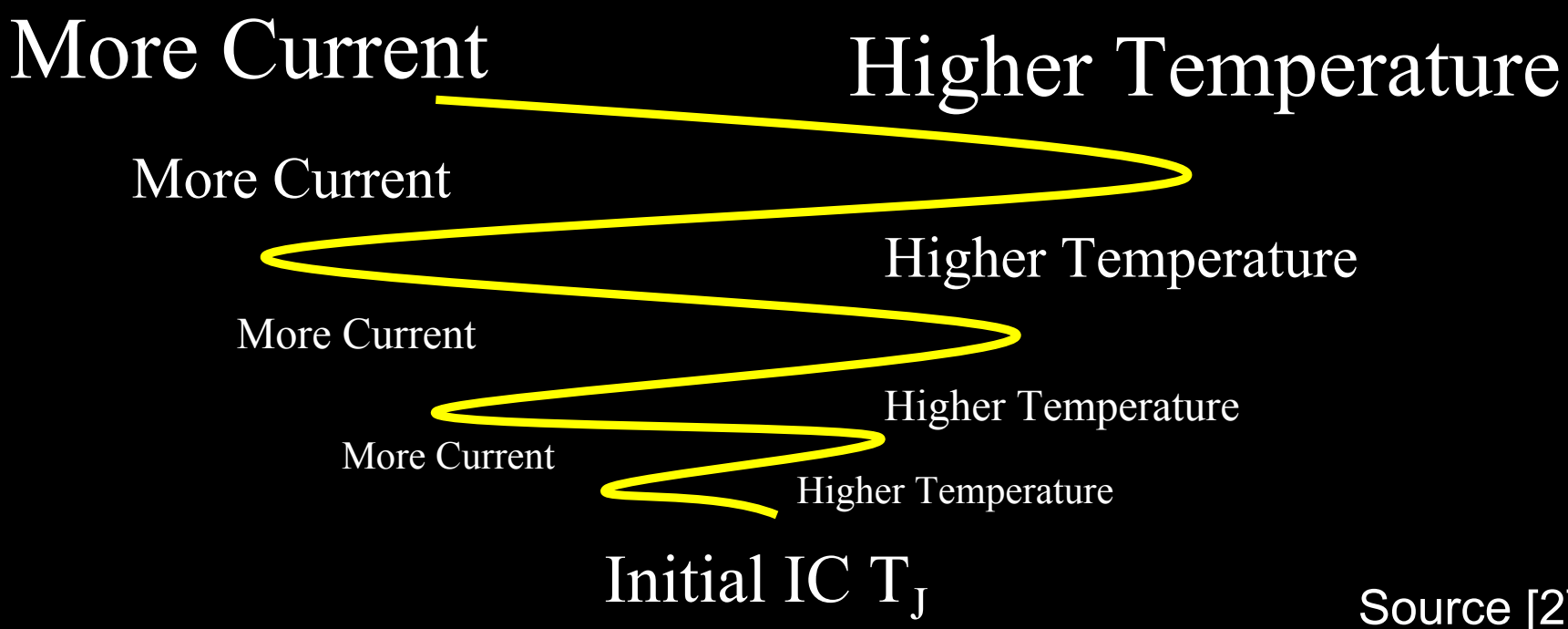
CHIP LEAKAGE HOTSPOTS
(microprocessor logic cores)



Source [2]

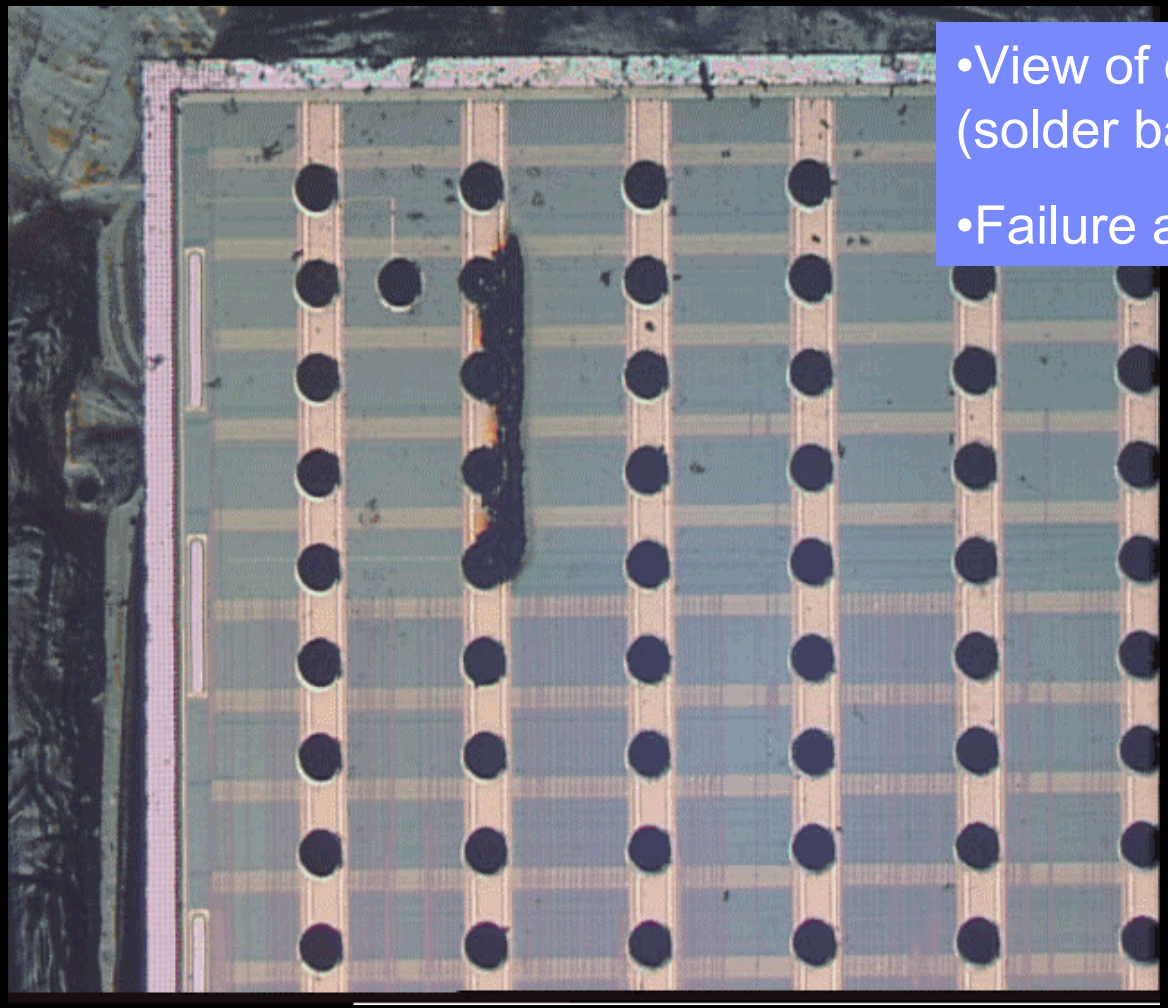
THERMAL RUNAWAY

- **Thermal runaway is a positive feedback phenomena in which leakage current and temperature interact in an exponential fashion with each other**



Source [2]

THERMAL RUNAWAY



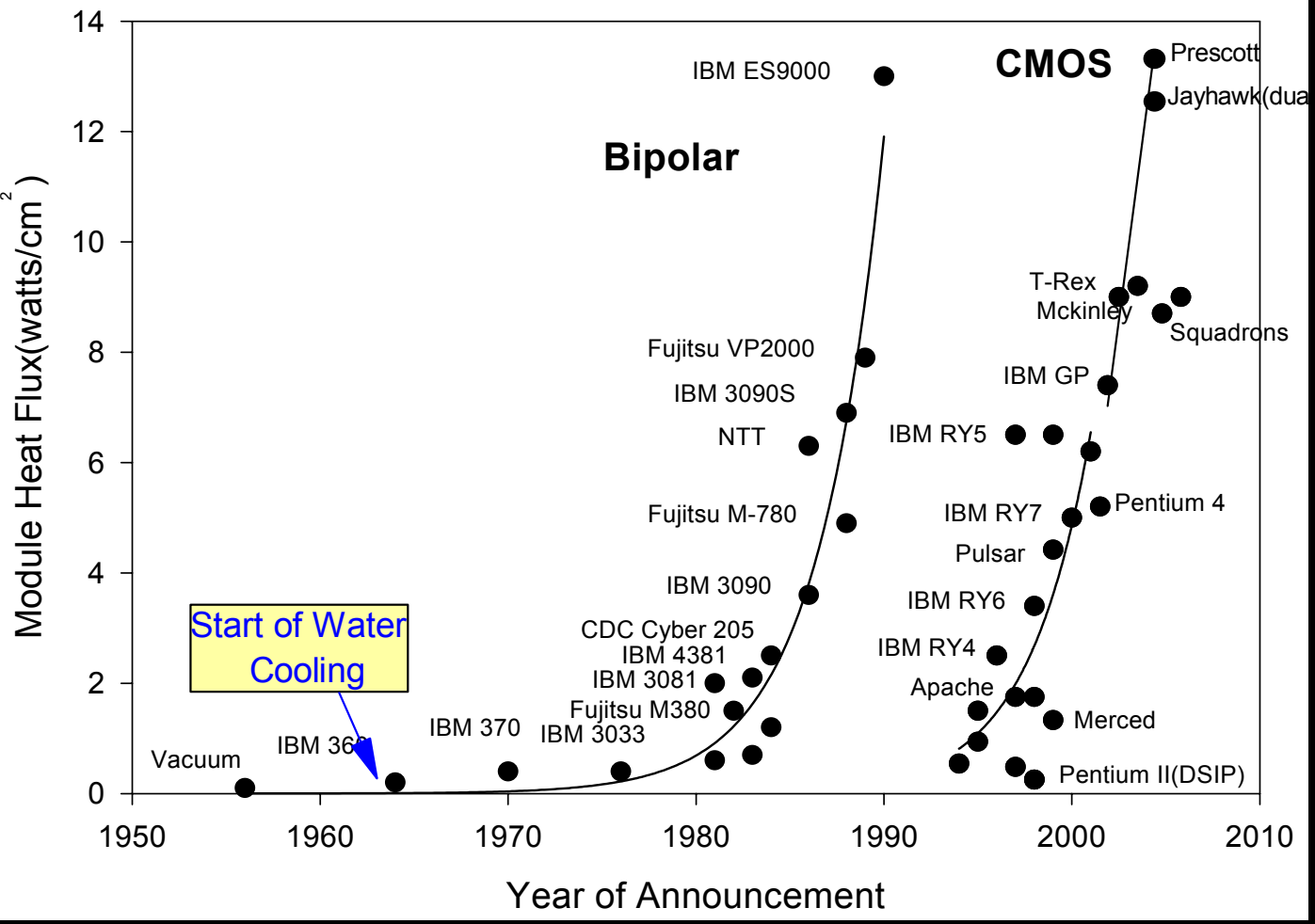
- View of damaged chip from C4 (solder ball) side
- Failure analysis photo

Source [2]

Thermal Problems at Wafer Test

- **Sharply increasing power roadmap**
  - Predicts that module test problems will also be seen at wafer test

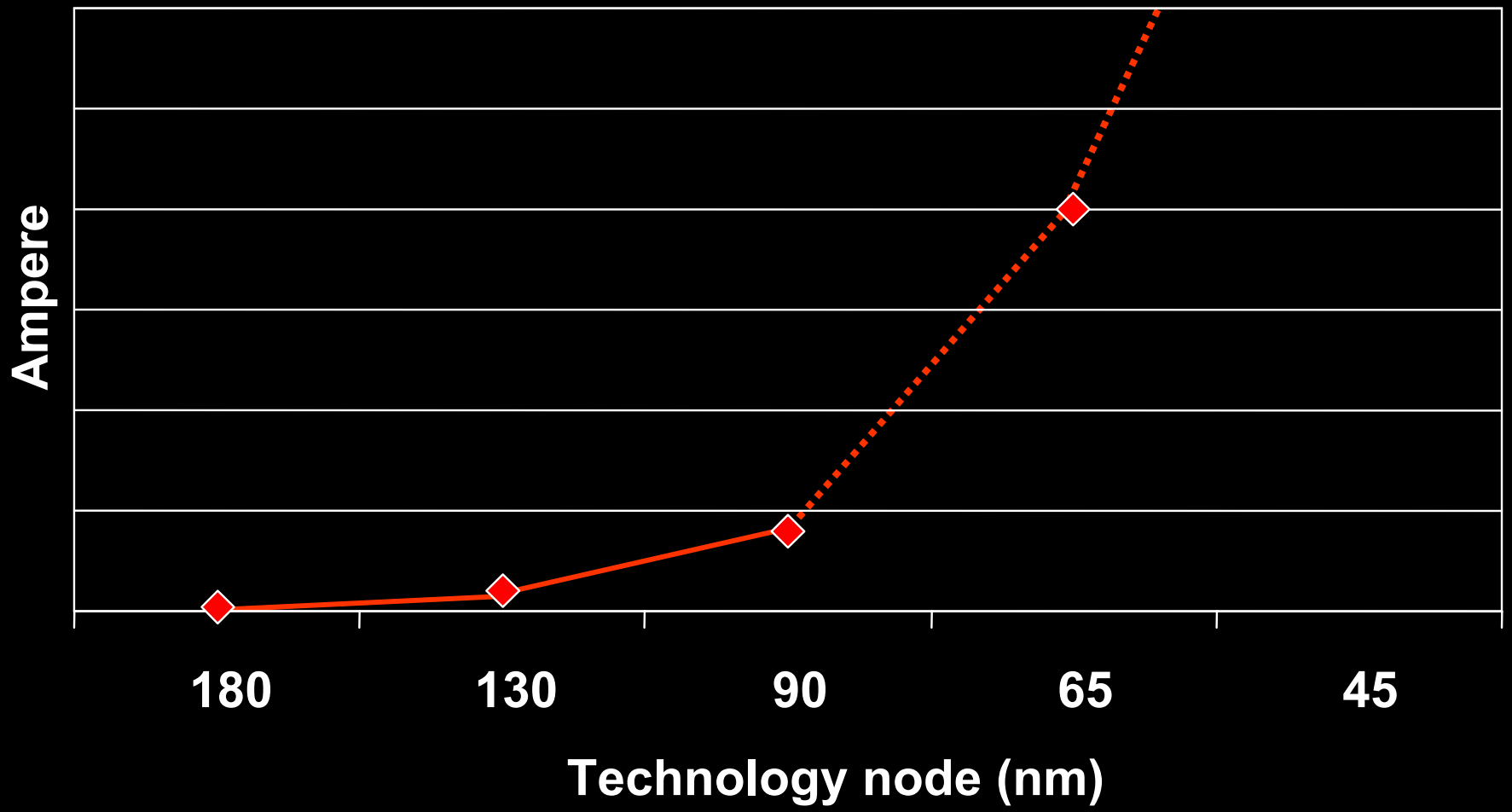
Module Power Trends



Source [1]

Leakage Current Roadmap

High Performance Microprocessor



Anticipated Thermal Problems at Wafer Test

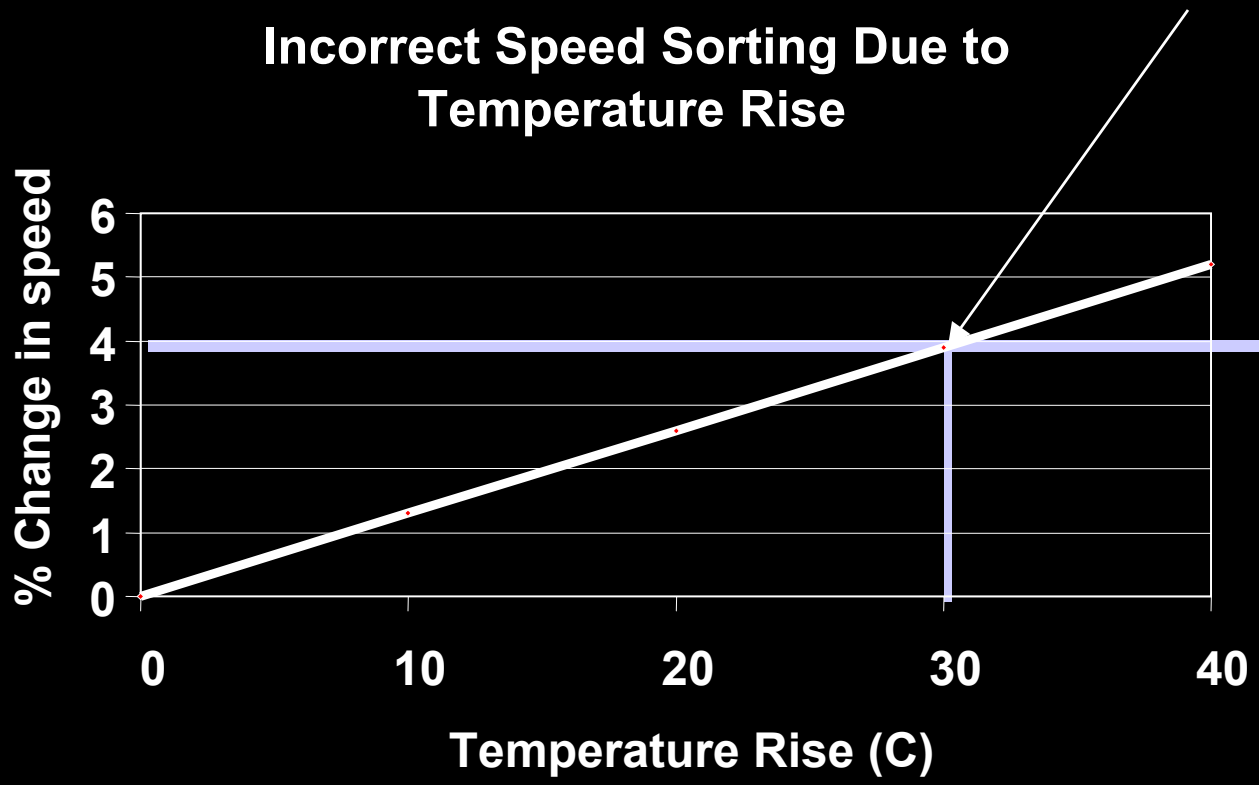
- **Problems from high power levels**
  - Wafer damage
  - Unknown wafer sort status due to incomplete test (over-current shutdown)
  - Incorrect speed sorting due to temperature rise and resulting speed shift
  - Probe card damage

Incomplete Wafer Testing

- **High leakage parts may exceed power supply capacity**
- **These untested parts are passed on to module test**
- **Increased number of defective parts causes higher packaging and test costs**

Thermal Problems at Wafer Test

Power variations can cause a temperature difference greater than 30 C



Probe Card Damage

- **High currents can damage probe cards**
  - Expensive to repair or replace
  - Delay in shipping tested wafers (if cards in limited supply)

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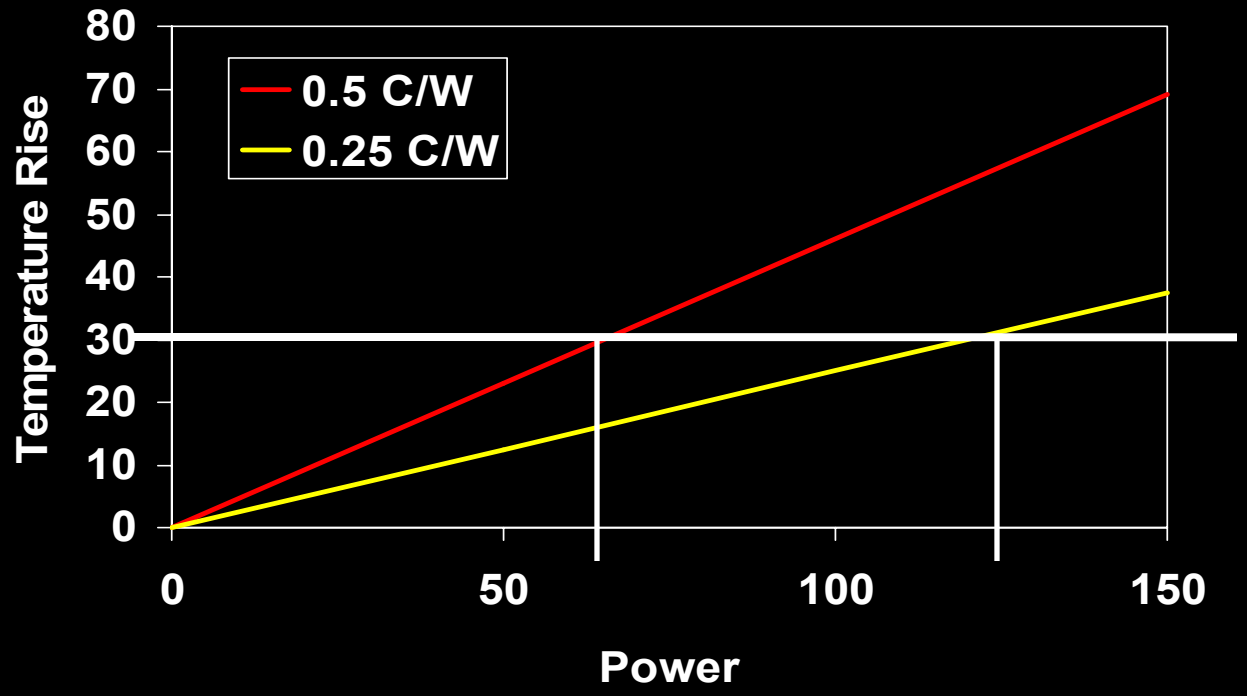
Solution

- **Thermal resistance improvement**
  - This provides three benefits:
    - Reduces the temperature rise vs. power
    - Reduces the die to die temperature variation (due to varying power levels)
    - Reduces the effect of across the chuck resistance variation

Speed sorting benefit from reduced thermal resistance

Larger power variation without sort error



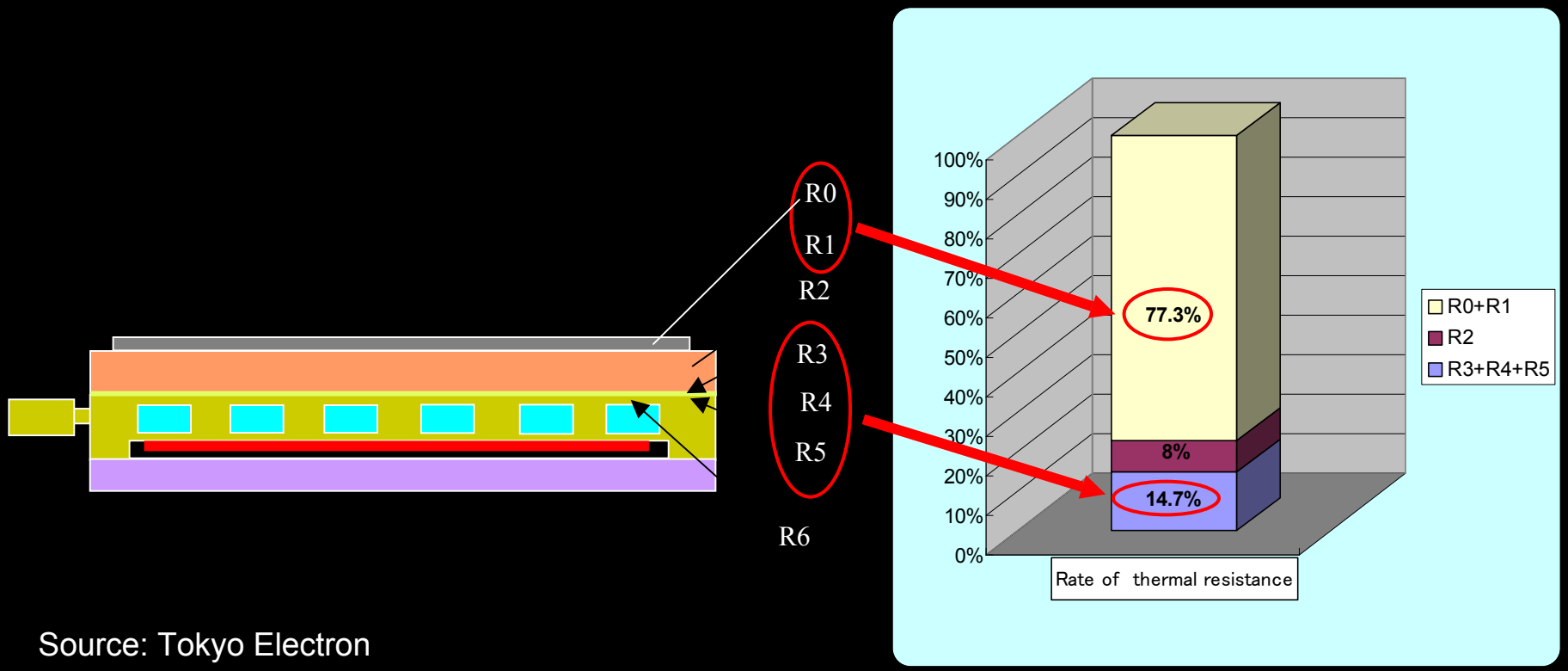
10 X 10 mm powered area

Assessing the Most Effective Approach to Reduce Thermal Resistance

- First step is to quantify the contributors to thermal resistance

Thermal Resistance Components

Wafer to chuck resistance (R0+R1) is largest contributor



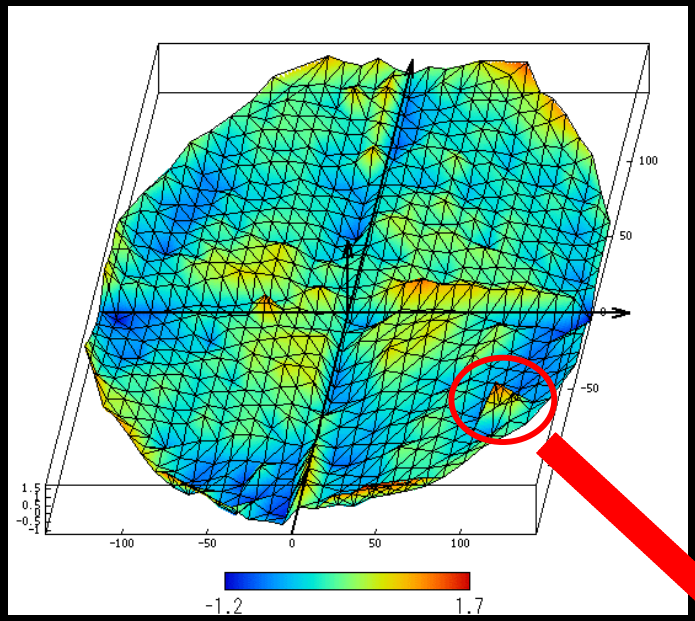
Source: Tokyo Electron

Improving wafer to chuck dry contact

- Theoretically, resistance could be improved by increasing chuck and wafer smoothness and flatness
- However, this resistance would be likely be sensitive to any particles or surface damage
- Measurements showed that it wasn't possible to match wafer and chuck contours
- Backside polishing of 300 mm wafers gave only 5 to 10% improvement and added processing cost

(Data courtesy of David Audette, IBM)

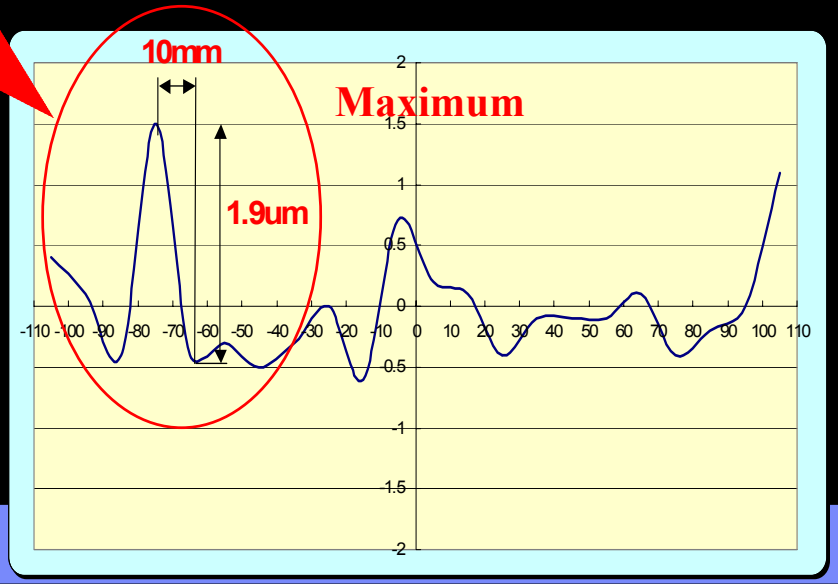
Chuck top Smoothness



1. Overall chuck flatness was 2.9um across more than 300 mm. (High quality surface)

2. However, localized roughness was 1.9 um

(Silicon wafer is about 0.35 um)



3. Conclusion: it is not practical to make sufficiently smooth matching surfaces (chuck to wafer)

Source: Tokyo Electron

Thermal Resistance Options

- **Interface Gas**
  - Helium would give some improvement but not enough (approximately 20%)

Thermal Resistance Benefit from Wet Interface

- **Main resistance is at interface of wafer to chuck**
- **Fluid replaces air in microscopic gaps**
- **Note that the heat is not carried away by fluid flow; it is conducted through the fluid into the chuck**
- **Thermal uniformity is less sensitive to surface finish or particles, since fluid fills any gaps.**

Liquid Interface Chuck System

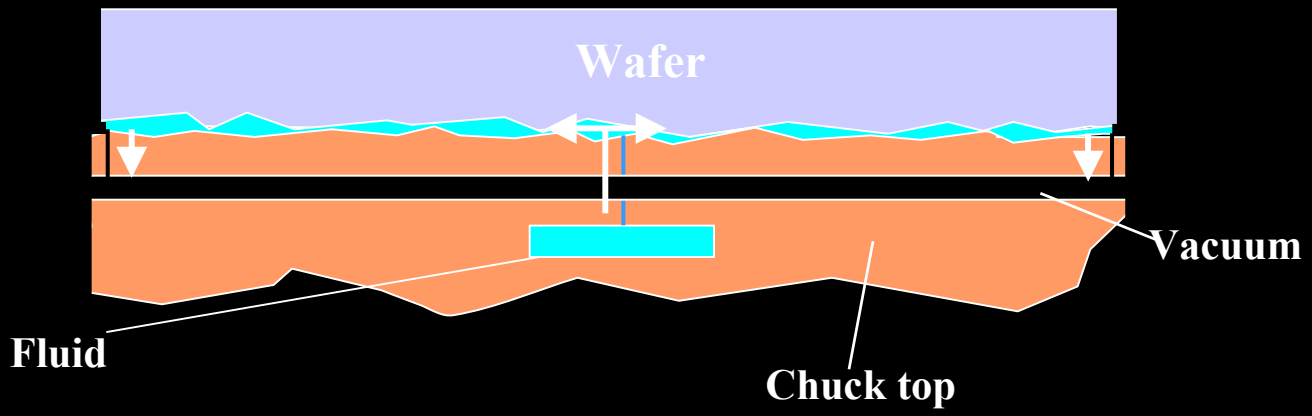
- **Goal : achieve the minimum thermal resistance and maximum thermal uniformity.**
- **At least 600 W capability**
- **Approach must be consistent with the following guidelines**
  - Avoid radical change to the tool
    - Avoid large development costs, and reduce lead time
    - Upgrade must be retrofittable to minimize the cost
  - Minimize additional processing cost
  - Dry or wet mode operation (same prober, with minimal transition time)
  - 200 and 300 mm

Concept

a) The wafer is pulled tightly onto the dry chuck by vacuum.

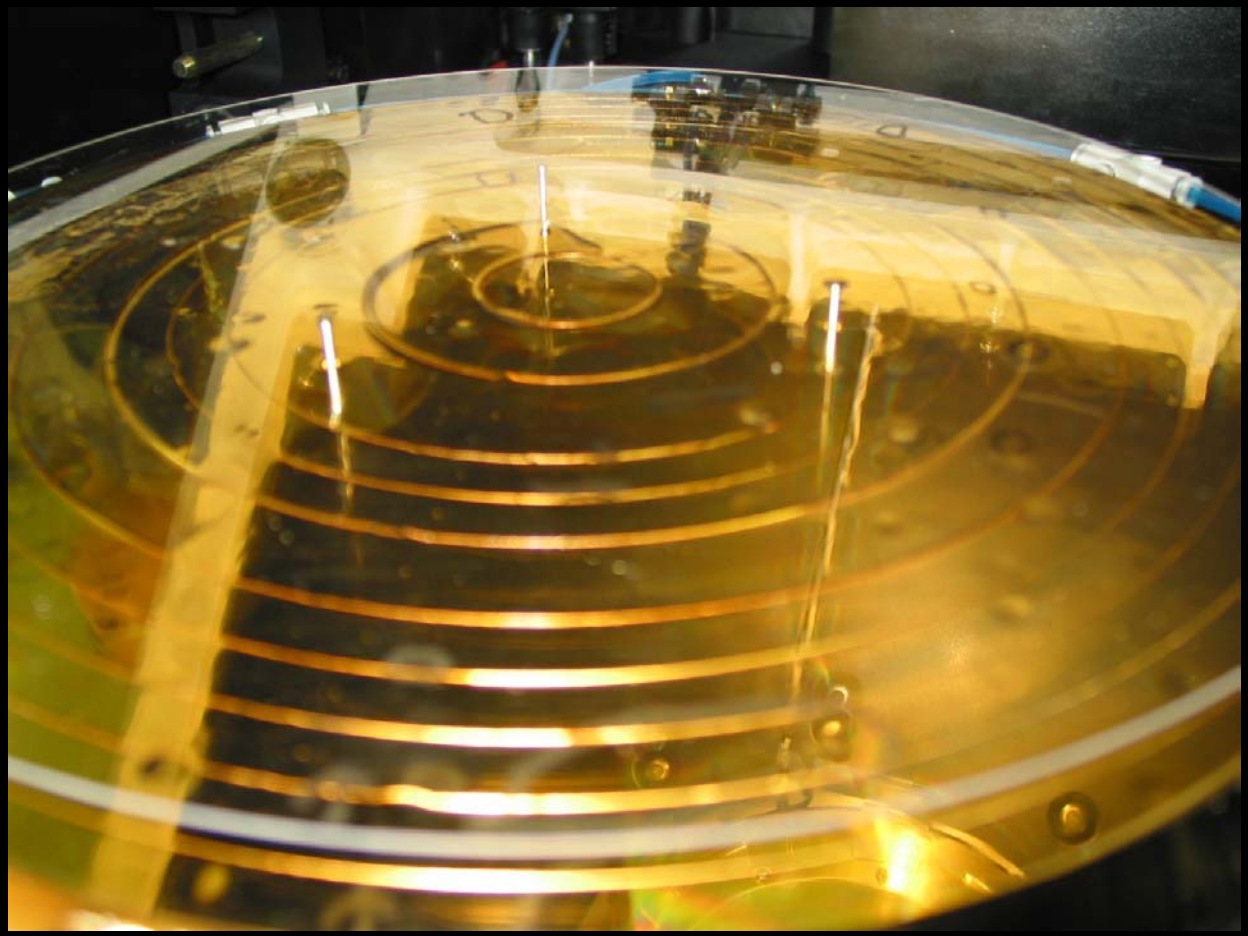
b) Fluid is supplied under pressure on the supply side and pulled by vacuum at the recovery side.

c) The fluid seeps between the supply and recovery sides via the wafer / chuck interface.



Source: Tokyo Electron

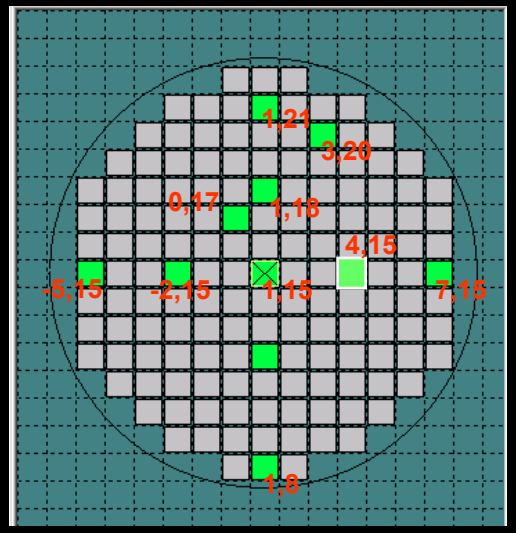
Fluid Under Glass Wafer (Prototype Chuck)

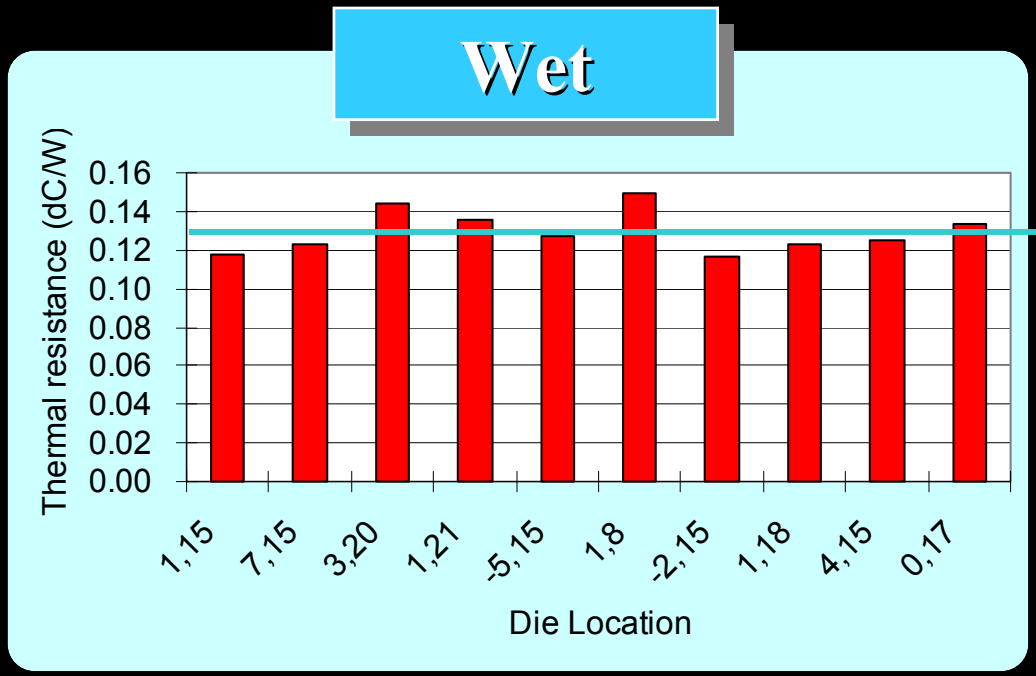


Note that the wafer is lifted up on the pins, at which point the fluid is normally completely recovered.

Source: Tokyo Electron

LTI Testing Results



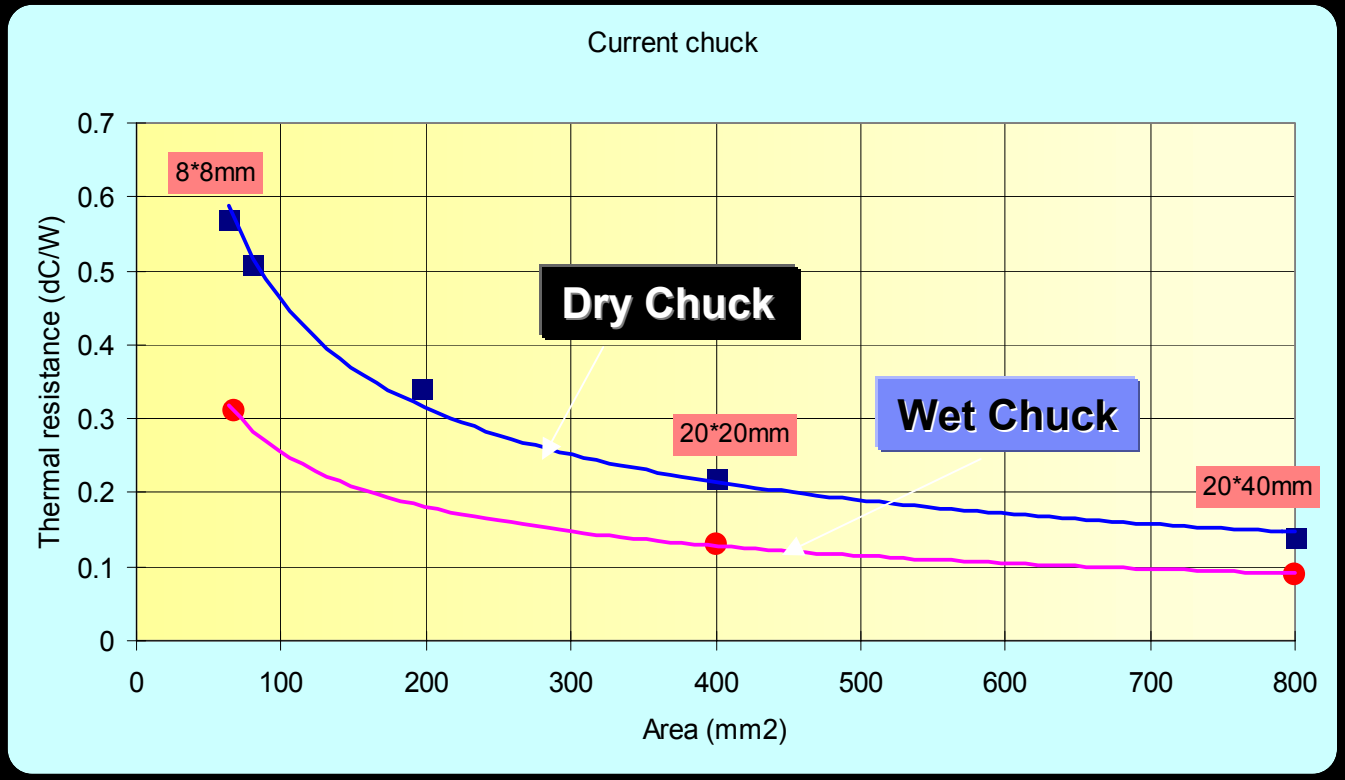


0.13 C/W (Avg)

Source: Tokyo Electron

Thermal Resistance vs. Die size

Experimental data



Source: Tokyo Electron

Installed System

Circulator for liquid interface with TEL P12XLn and Teradyne J973

Current Status

- **System meets all specifications**
  - Reduces thermal resistance by 50%
  - Uniformity is better by 70 %
  - Maintains performance at 600 W or more
- **Liquid thermal interface system has been installed and has run engineering wafers**
  - Wet vs. dry operation is transparent to operators (part of product file)
  - No wafer handling issues

Predicted Benefit

This chuck will be an essential tool for

- Preventing thermal runaway
- Improving speed sorting accuracy
- Reducing probe card damage

ACKNOWLEDGEMENTS

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Principal Contributors

- IBM: Phil Diesing, David Audette, David Gardell
- TEL: Yutaka Akaike, Glen Lansman, Shane Pudvah, Yoshinao Kono

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