POWER DELIVERY MODEL OF TEST PROBE CARDS

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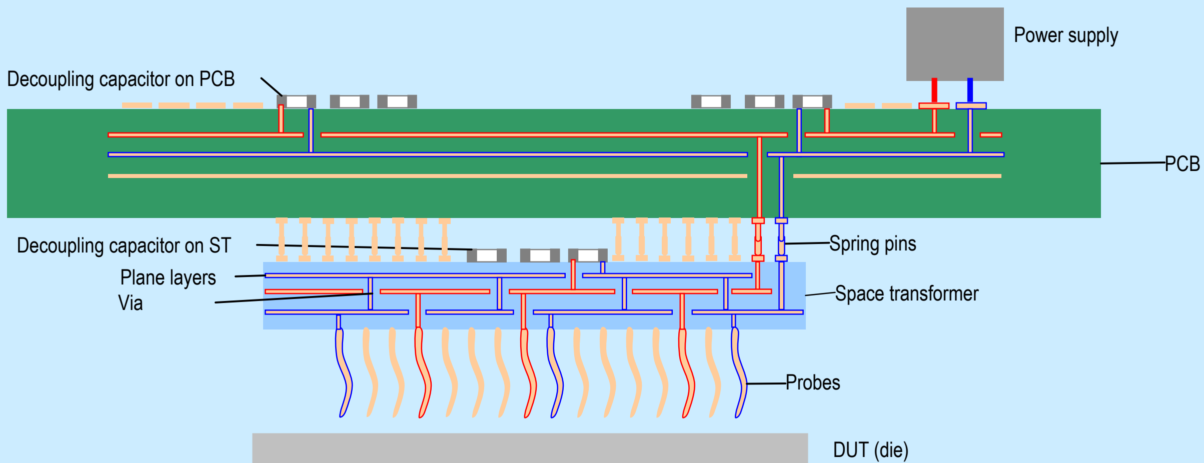
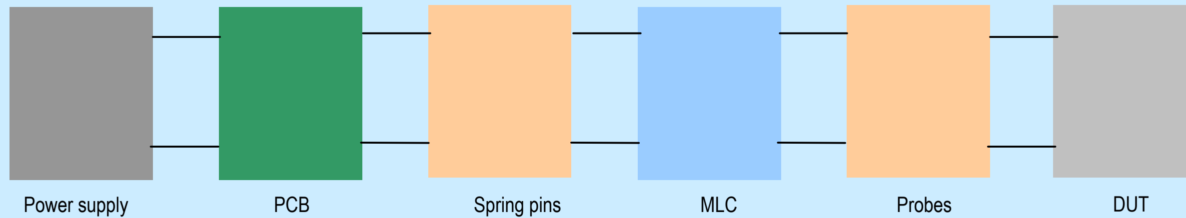
Overall system view





Challenge

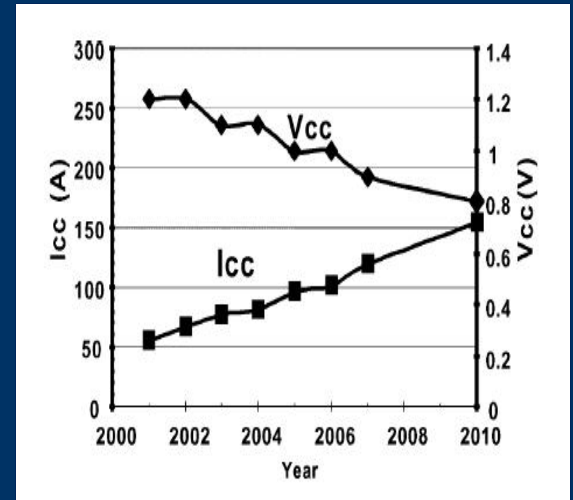
- Assuming one of the latest generation processor is being tested
- Power consumption:100W
- Supply voltage:1V
- What if DUT ramps from 0 A to 100 A in 5 ns having 20 A/ns slew rate [Ref1].

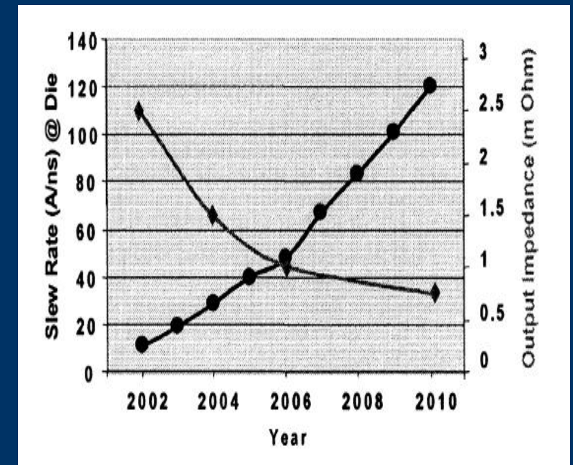
Any resistance and inductance seen on the path will create voltage drop defined by Vdrop=Lpath*Δi/Δt+Rpath*I

- Given maximum allowed voltage drop of 0.5V (0.25V inductance related + 0.25V resistance related)

Maximum path inductance 12.5pH

Maximum path resistance 2.5 mohm





Achievable?

- Can 12.5 pH and 2.5 mohm be achievable?
- Assuming DUT has 1000 (500 VCC – 500 GND) probe pads
- For given probe height (h)=200mil, probe diameter(2*r)=80um, probe pitch (s)=200um.
- For given total system height (h_{tot})

$$L_{tot} = \frac{h_{tot}.2.\mu_0.\mu_s}{n.\pi} \ln\left(\frac{s-r}{r}\right)$$

Probe + ST + Spring pin +PCB

200+100+100+200=600mils

Total inductance = **16.9 pH**

Assuming 70 percent of the path resistance is created by the contact resistance of probes, then

Max contact resistance for each probe = **437 mohm**

- Rough calculations show that system requires careful analysis of each stage

Goal of the study

- Modeling of each block from transient analysis perspective including 3D electromagnetic modeling
- Observe transient voltages in each stage (subsystem)
- Determine highest voltage drop contributors
- Reduce voltage fluctuations by means of changing: design, routing and mechanical structure and/or developing new strategies.

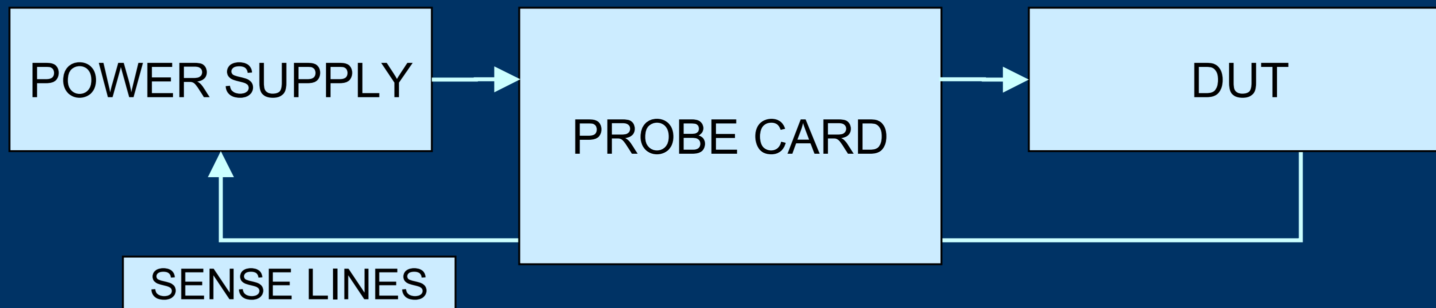
Distributed vs. lumped model

- Major inductance components are height dependent and height of the system is small compared to wavelength/10
- Second biggest contributor; contact resistance may be represented better by lumped model
- For PCB and ST design, EM based simulation tools can be run such as PowerSI from Sigrity Inc. or Ansoft Q3D using distributed model [Ref 3]. Mechanical designs, spring pins and probes require special attention.
- Lumped model representation has been selected for the reason of being faster and accurate in reasonable boundary.
- What if each probe carries different amount of current?

  Current differences will be equalized on ST level (plane connection).

HCDPS (High current device power supply)

- Modeling is based on short term transient response. (<1 uS)
- During simulation duration power supply correction loop is nonfunctional (existing power supply closed system bandwidth is limited to kHz region)[Ref 2]



PCB

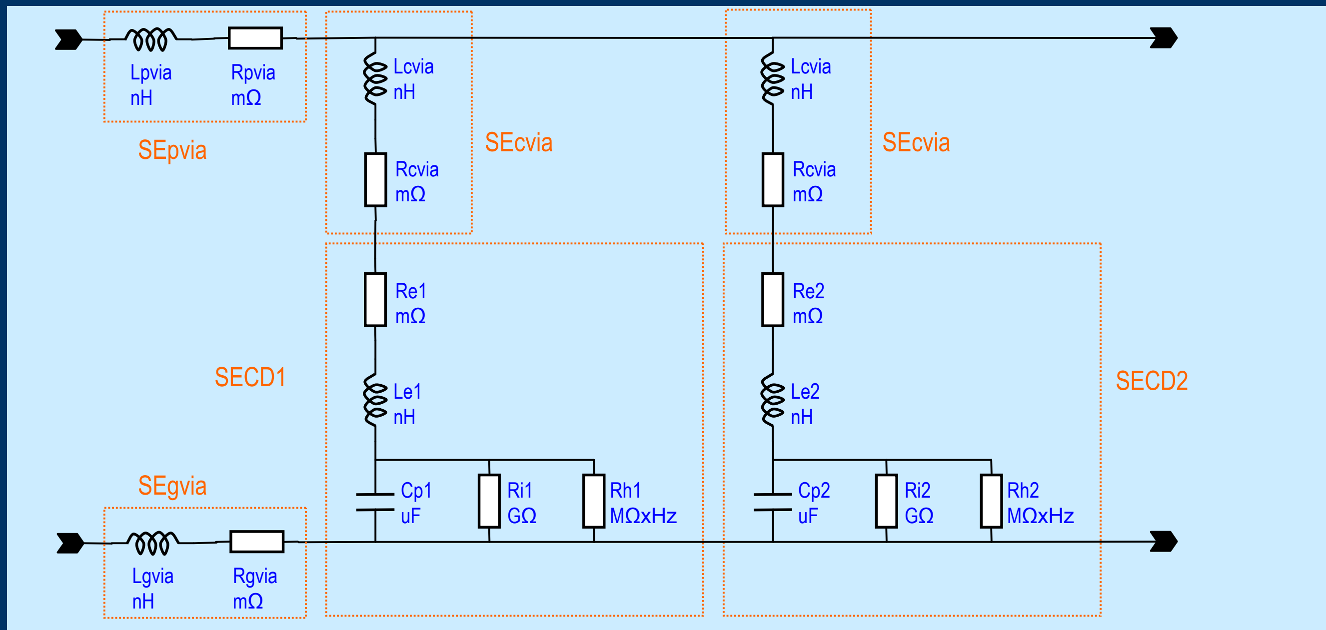
- Main contributors : Via inductance , plane layer inductance.
- Number of vias can be increased to reduce via inductance effects to negligible level
- PCB area has enough space to put decoupling capacitors to compensate inductance effects.
- For decoupling capacitors via effects should be minimized.
- Better ESL and ESR decoupling capacitors should be used
- Due to space convenience PCB contribution to overall system voltage drop budget can be minimized easily (<3%)

$$L_{layer} = \mu_0 \mu_s \frac{d}{w} l$$

$$L_{via} = \frac{\mu_0}{2.\pi}\left[h \ln\left(\frac{h+\sqrt{r^2+h^2}}{r}\right) + \left(r - \sqrt{r^2+h^2}\right) \right]$$

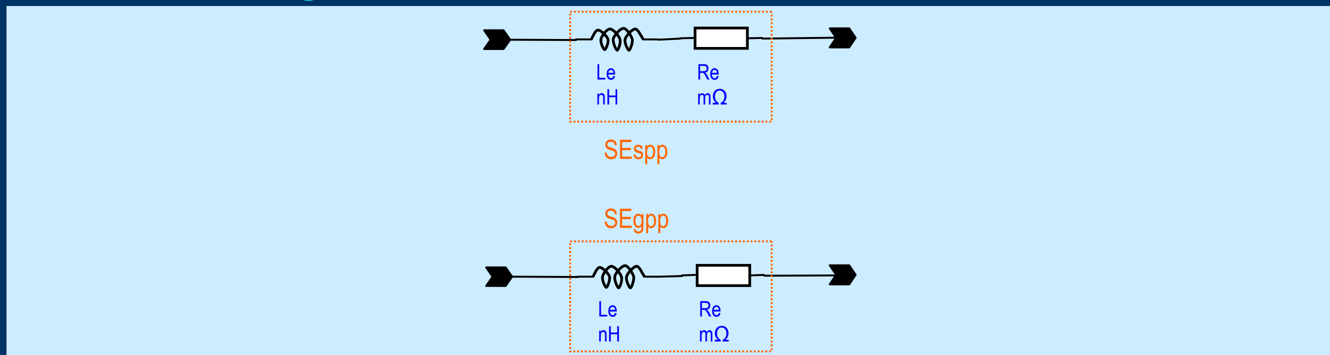
PCB model

- Different capacitor values are used to lower impedance on different frequency spots



Spring pins

- Main contributors: Pin inductance, contact resistance.
- Pin inductance could be reduced by making shorter and increasing pin diameter.
- Contact resistance can be minimized by solidly fixing one side of the pogo pin such soldering etc. which is a tradeoff with mechanical replaceability
- Each path models the half of the loop inductance including partial inductance and mutual inductance. Values are acquired from 3D electromagnetic simulator.

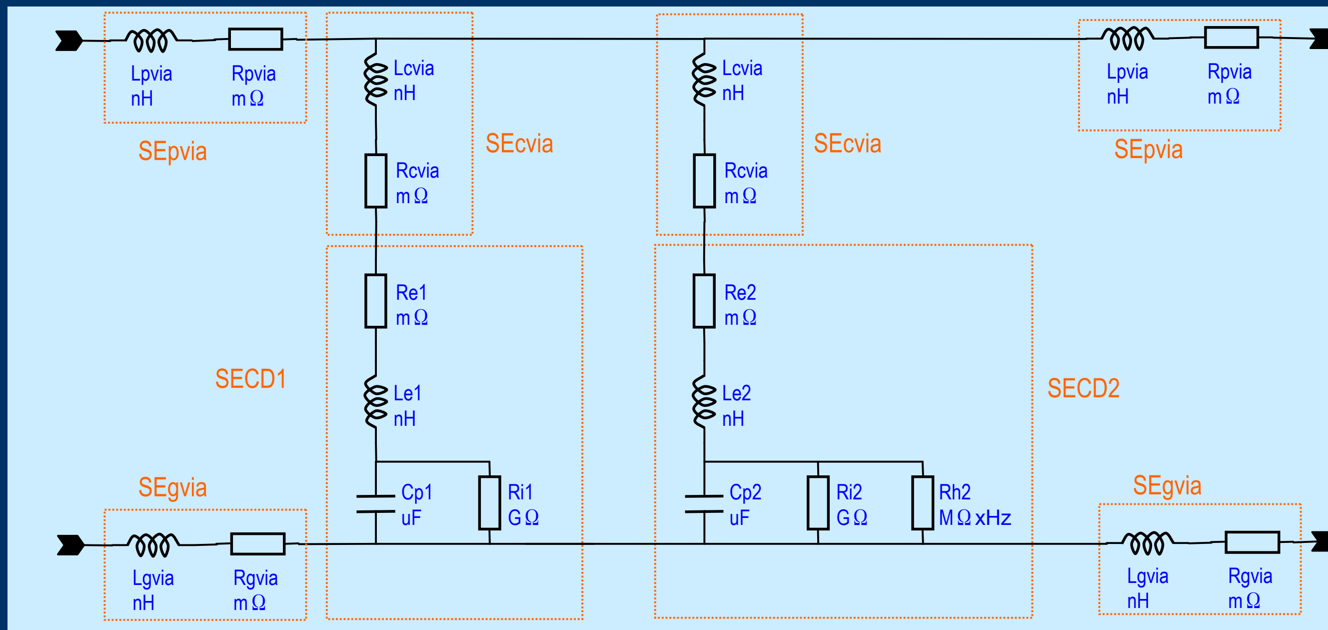


Space transformer (ST)

- Main contributors : Via inductance and plane layer inductance.
- Increasing number of vias is troublesome because it has limited area for additional vias, also tied by design rules
- Generally LTCC ceramics are used for base material and via spacing rules are wider due to shrinkage during sintering, limiting maximum via number
- Limited amount of decoupling capacitors could be added (backplane space limitation)
- For decoupling capacitors low ESL capacitors are used (IVX).
- Voltage drop contribution of space transformer is quite large (~25%)

ST model

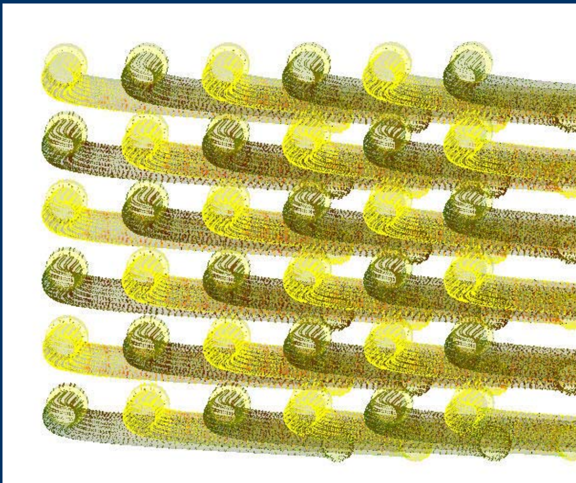
- Via effects are shared before and after decoupling capacitors

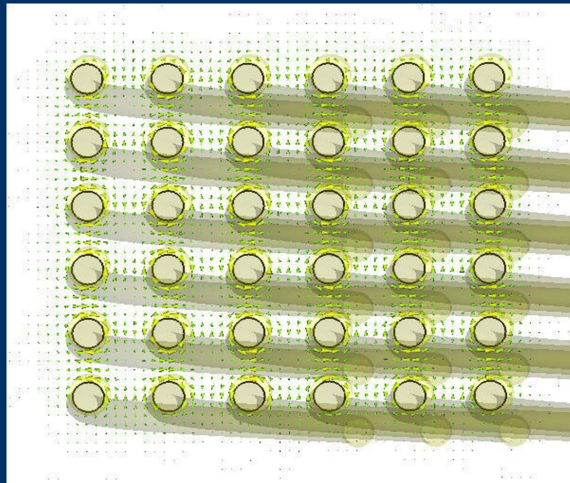


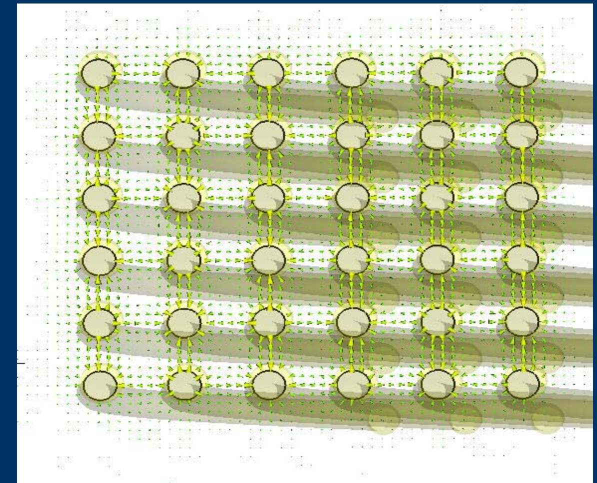
- Probe inductance and contact resistance are the main contributors.
- Inductance could be lowered by reducing probe height and increasing diameter of the probes, tradeoff with mechanical deflection and forces
- Contact resistance could be decreased by using one sided mounted probes.
- Could be modeled with partial inductance and mutual inductance

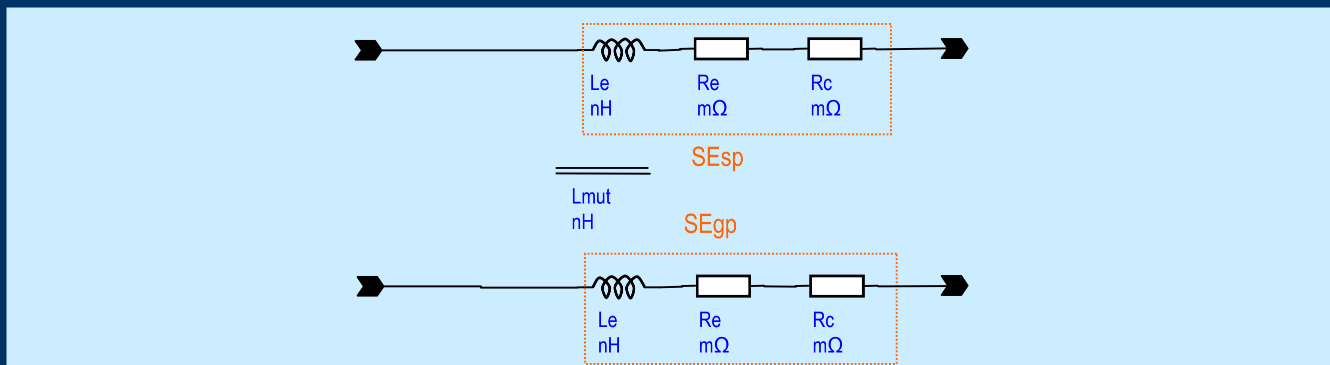
Probe model

- Mutual inductance lowers the total inductance by 20 percent for given pitch. Although smaller pitch reduces probe inductance, crosstalk becomes worse.



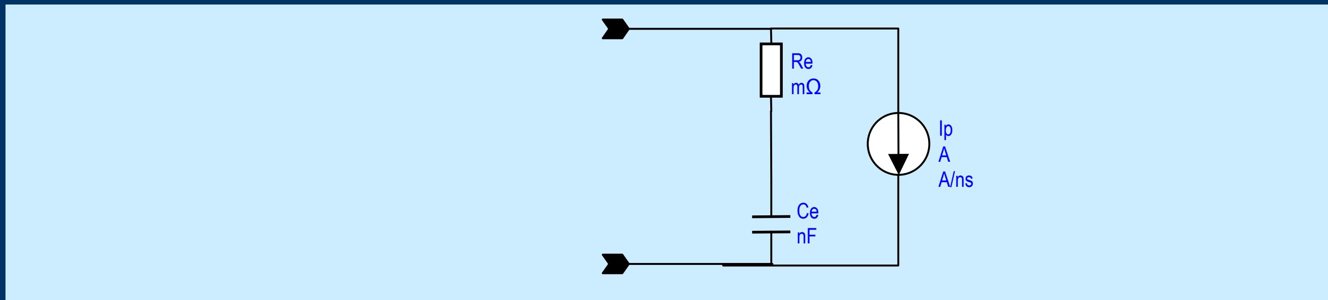




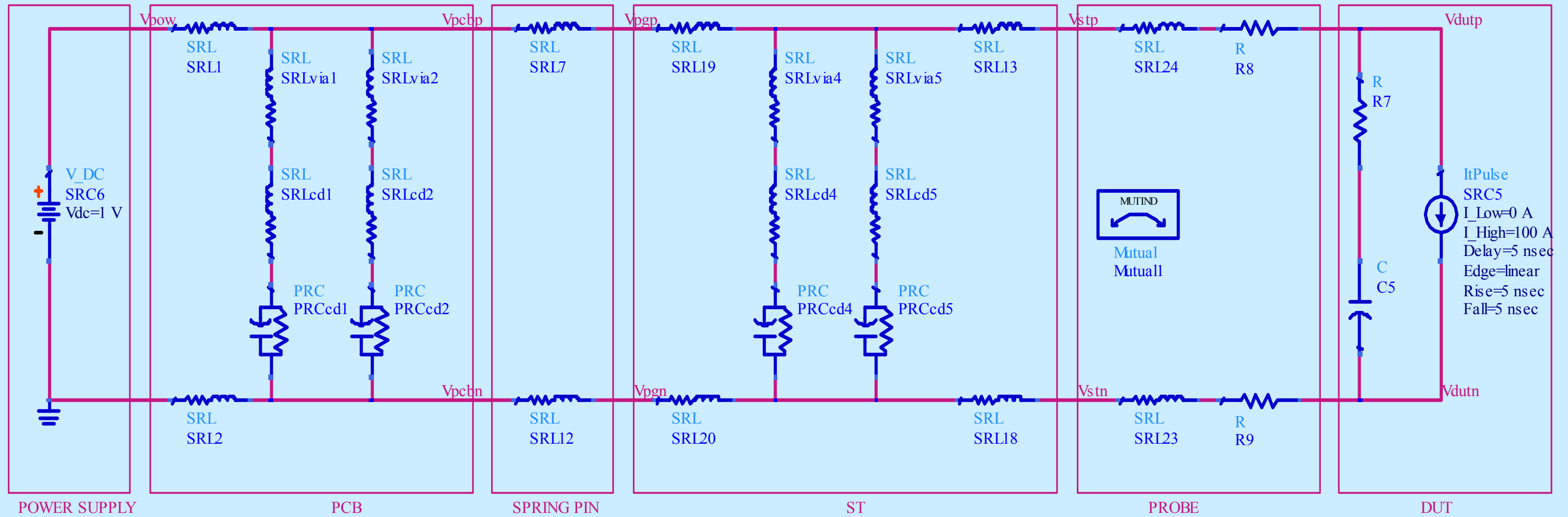


DUT

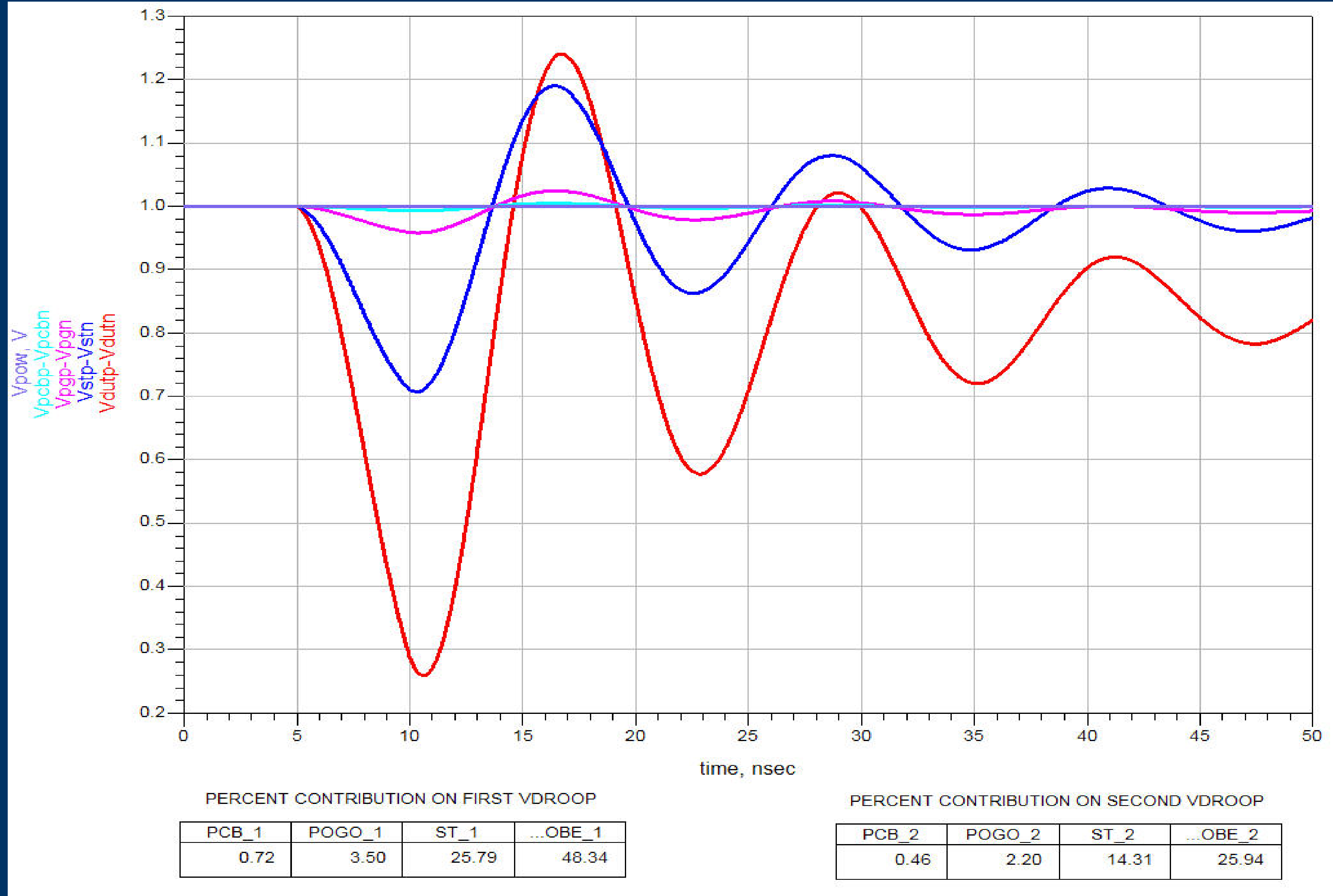
- Ondie capacitance created by supply line routing and device parasitics improves short term transient response.
- High slew rate ramping modeled by step current source.



Combined model



Transient response



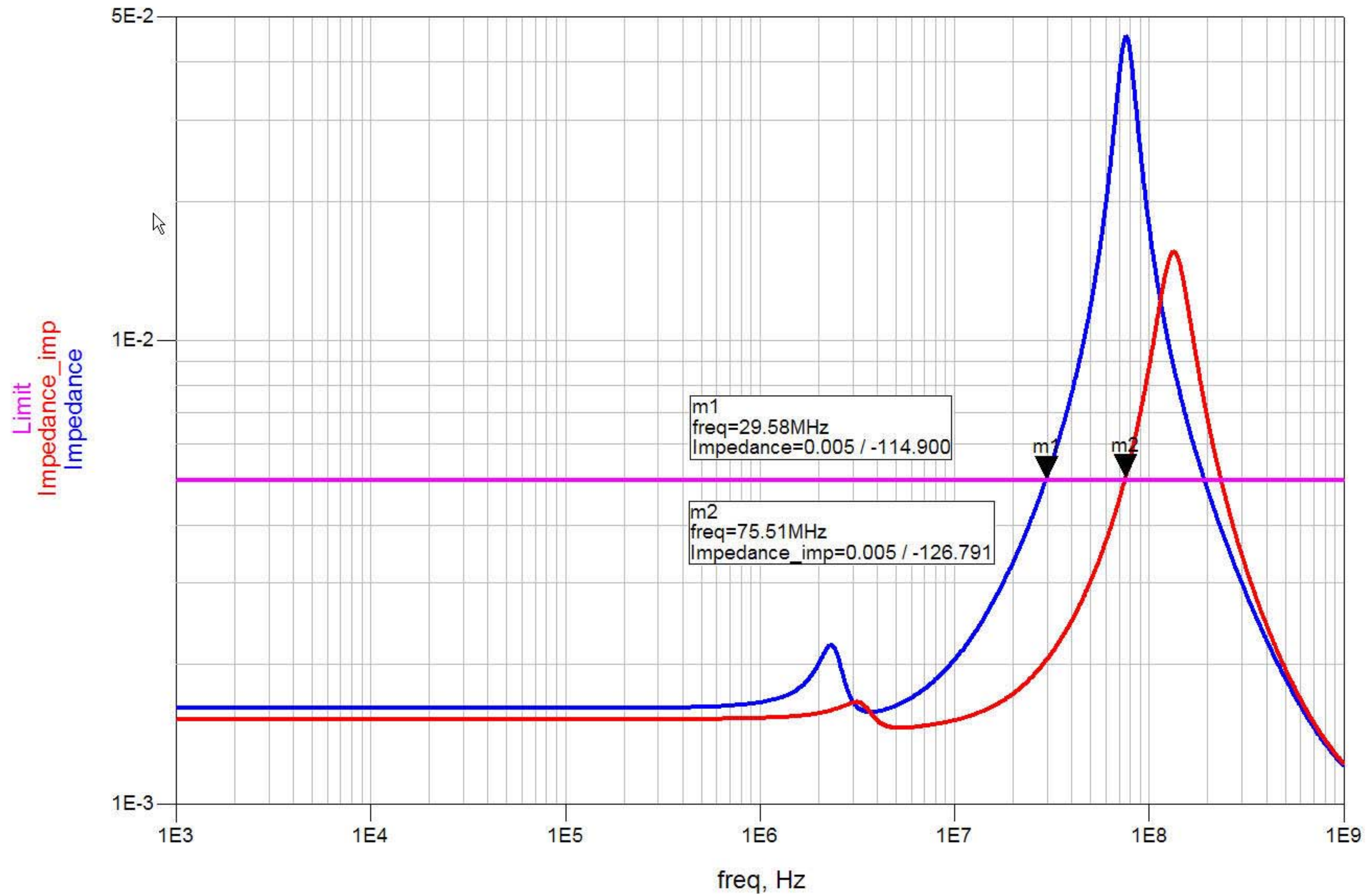
PERCENT CONTRIBUTION ON FIRST VDROOP

PCB_1	POGO_1	ST_1	...OBE_1
0.72	3.50	25.79	48.34

PERCENT CONTRIBUTION ON SECOND VDROOP

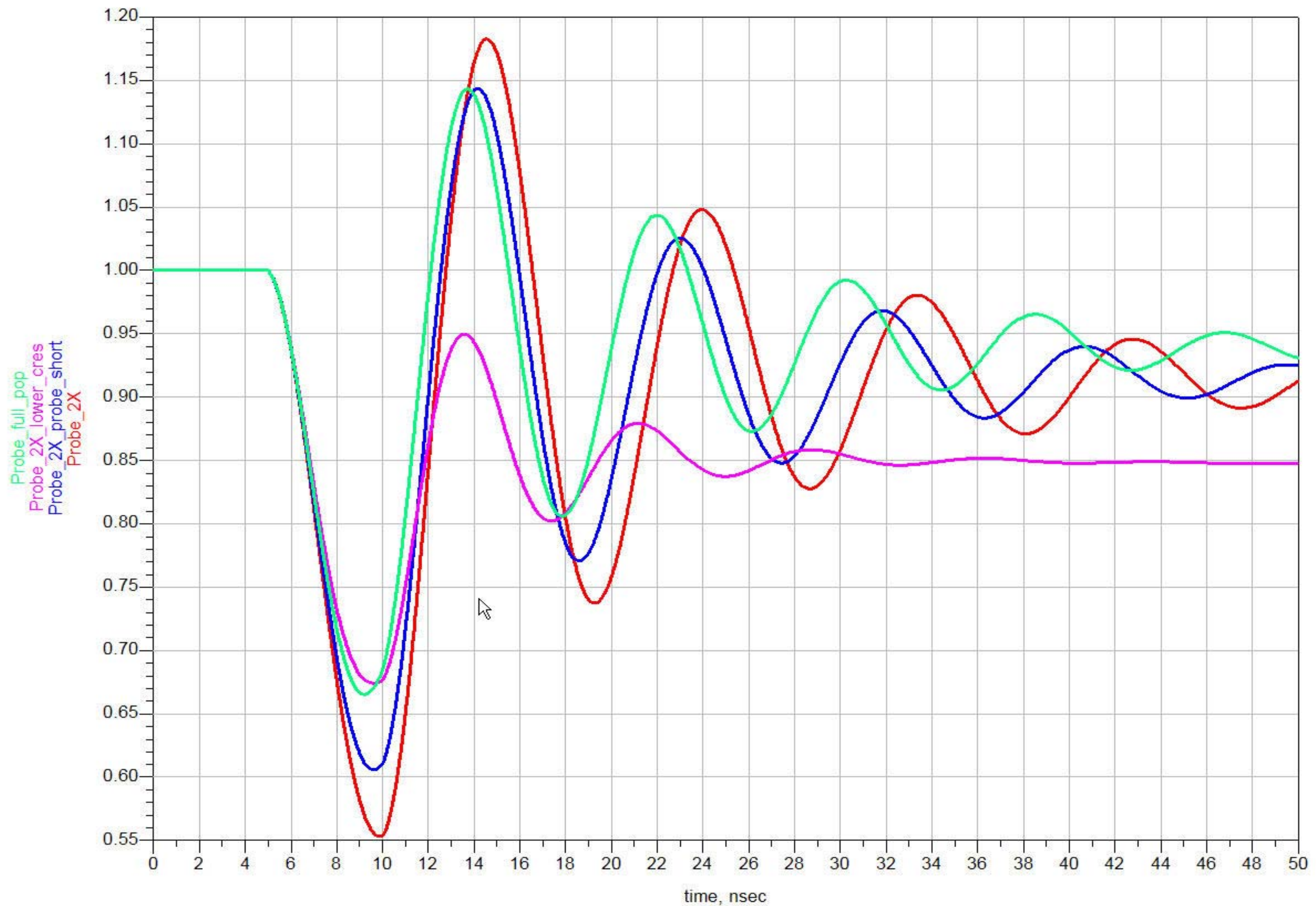
PCB_2	POGO_2	ST_2	...OBE_2
0.46	2.20	14.31	25.94

AC impedance seen by load



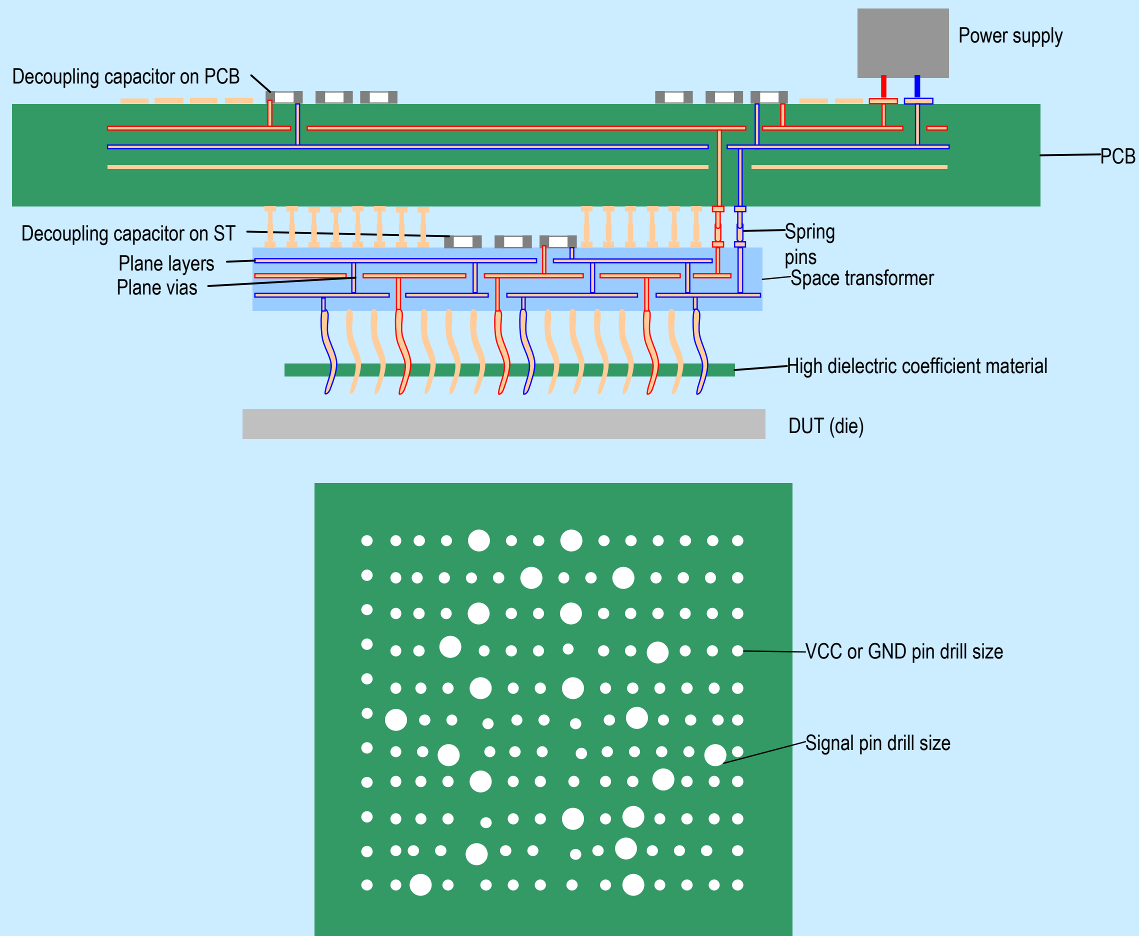
- Number of probes are increased. (different versions are simulated including two times the existing probe number and full populated version)
- Space transformer thickness optimized
- Different probe height versions have been experimented
- Space transformer design improved by means of increased via number and decoupling capacitors

After improvements



- New probe designs can be developed using reduced height
- Probe tip design and material can be optimized to reduce contact resistance
- Capacitors may be formed by dielectric layers close to probe tips reducing probe inductance effects (patent pending)
- On space transformer or PCB, fast transient feedback voltage regulator can be developed [Ref 4].

Dielectric layer



*patent pending

Conclusions

- High slew rate (~nS range) DUT power changes create voltage fluctuations on supply lines affecting test performance and speeds.
- Power delivery improvements are possible by means of careful design of each stage
- Improvement methods mainly trades with mechanical restrictions
- New technologies require more elaborate research

References

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Thank you for your interest and listening.