QUALCOMM CDMA Technologies

QUALCOMM CDMA TECHNOLOGIES

QUALCOMM PUBLIC

Integrated Fabless Manufacturing

"The" technical and business

model for the future.

Michael Campbell
QUALCOMM CDMA Technologies

Business and Technology Trends

- " The five "megatrends" that are shaping the industry are:
  - Continued integration due to Moore's Law,

From: Electronic News June 8th, 2006

Turbulent Times Ahead, Gartner Says

By Ann Steffora Mutschler

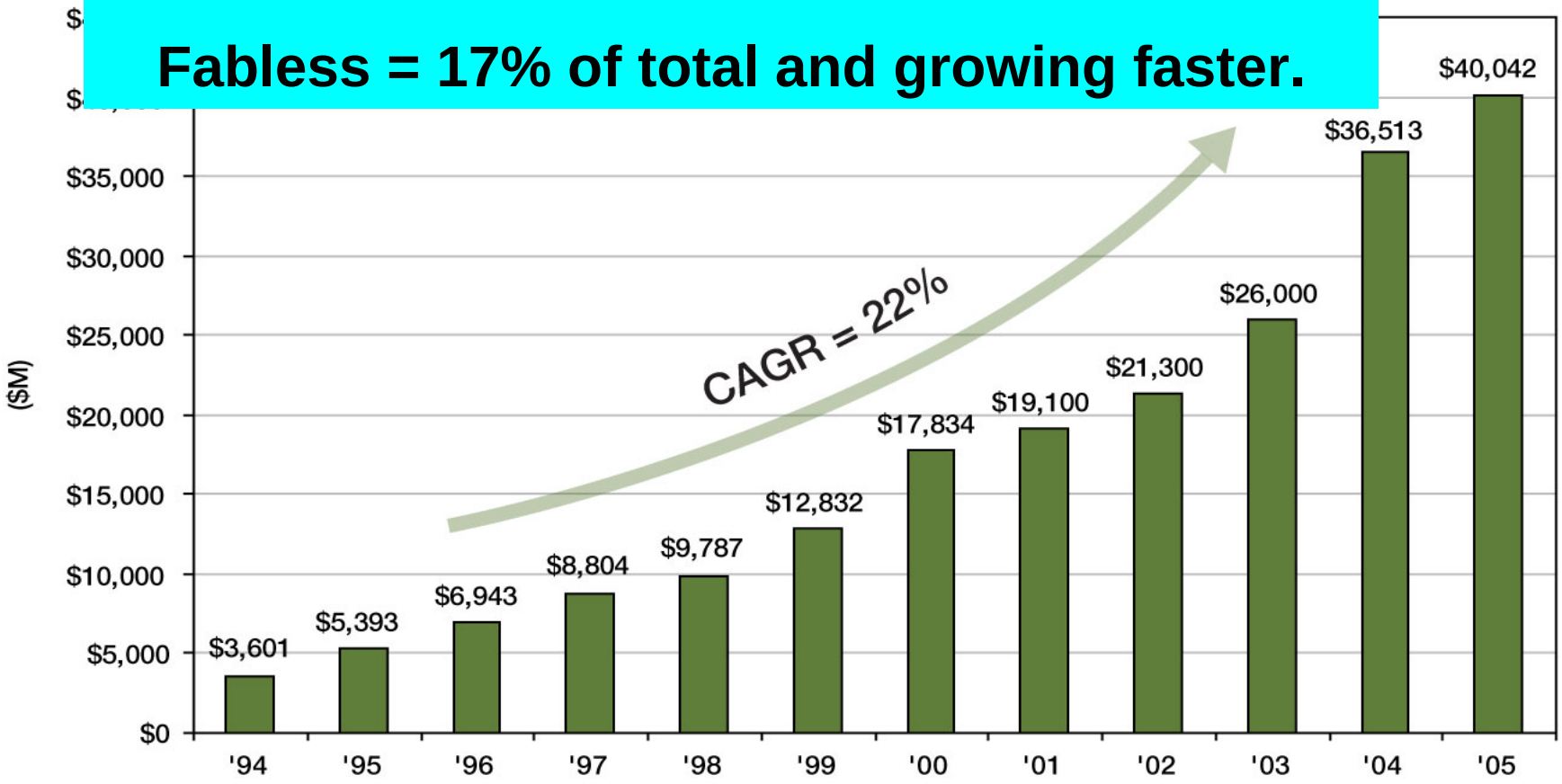
- Market growth rate is slowing, costs within the industry are not.
  - Continued integration leads to increasing complexity of devices
  - Escalating design costs will force companies to amortize those costs across more end users – single customer chips are dinosaurs. Killer apps harder to find

- "Fabs are getting bigger and more expensive,
  - Chip makers will either get bigger through mergers as more IDM become fabless or share manufacturing facilities;
  - Economies of operations will favor chip standardization leading to fewer chip manufacturers and more commoditization of silicon. (Gartner believes competition will prevail in any case, so that chip prices can remain low)
- Meeting consumer demand is tough, unpredictable and driven by fads and fashions that require fast time to market

Rapid Growth of the Fabless Industry

Global semiconductor sales amounted to $237.1 billion in 2005, up 3.6 percent from $228.8 billion in 2004 –

Fabless = 17% of total and growing faster.



Who is Qualcomm CDMA Technologies?

	Mkt Share	Rank	Leader	Source
RFIC	**20%**	**1**	**QCT**	**IDC**
3G Handset	**17%**	**2**	**Txn**	**IDC**
Mobile phone	**16%**	**2**	**Txn**	**Gartner**
Communication	**6%**	**2**	**Txn**	**IDC**
All IC markets	**1.4%**	**14***	**INTC**	**isuppli**

QCT Position:

#1 in RFIC

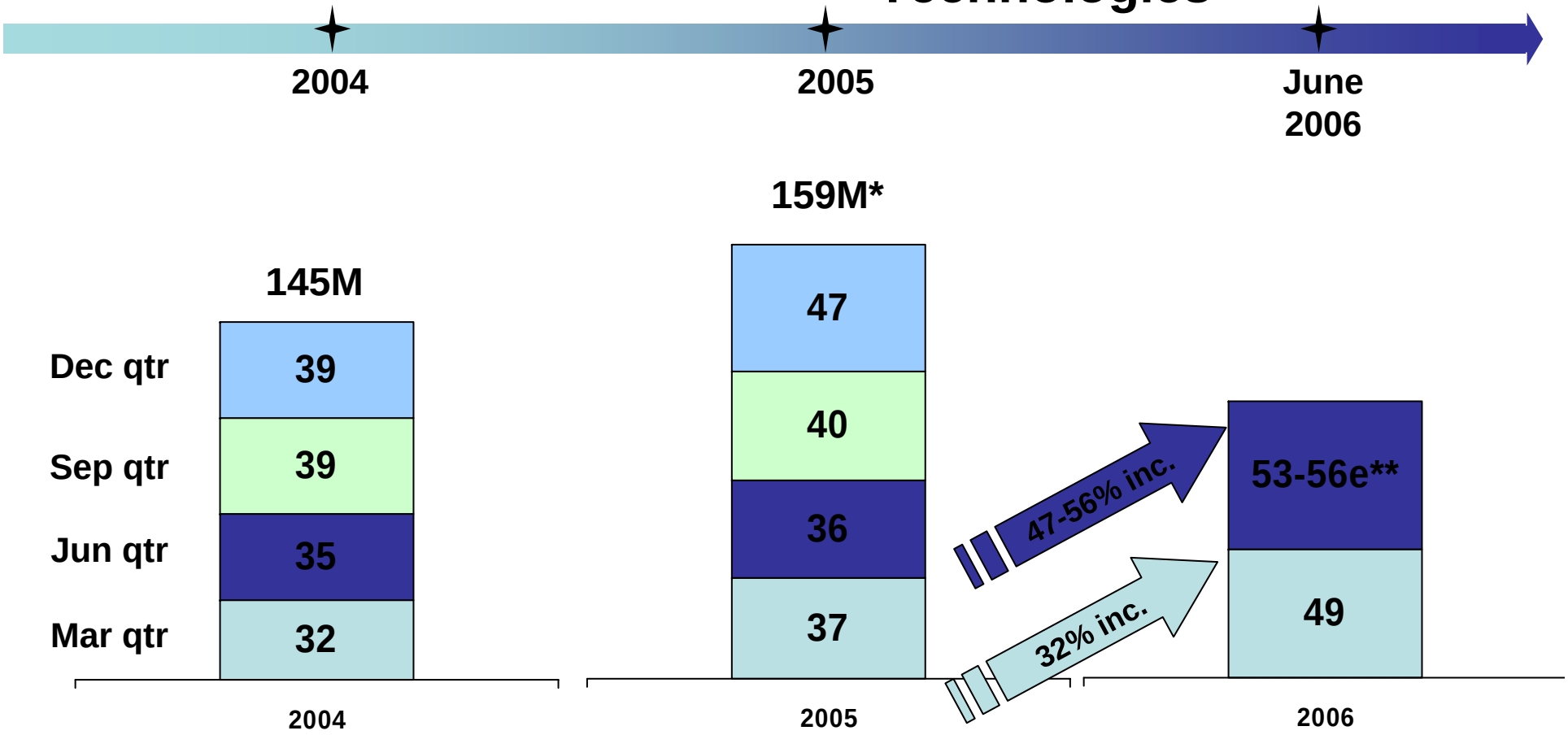
#2 in revenue for 3G phones

#2 in revenue for mobile phones

* Excludes memory and foundry revenue

Data from May 4th Analyst Meeting

Qualcomm CDMA Technologies



CDMA and WCDMA QUALCOMM MSM Shipments Accelerating

(Calendar Year, Millions)

*Sum of quarterly amounts do not equal total due to rounding.
**Guidance as of May 3, 2006

Leading WCDMA with Cost Effectiveness and Advanced Technology

First Commercial HSDPA Devices

ZTE MF330
1st MSM6280

Sierra Wireless
AirCard 860

Option Wireless
Globe Trotter

Novatel
Merlin U740

First HSDPA for Europe

Samsung Z560
16mm thin

First HSDPA in US

LGE CU320
HEDGE Cingular

Samsung ZX20
HEDGE1.8 Cingular

Feature-Rich Devices

36 New Handsets Launched in March and April

Toshiba V903T
AGPS

Samsung Z150
9.8 mm thin

Huawei U636
Entry Level

LGE U900
UMTS + DVB-H

ZTE F608
Low Cost Leader

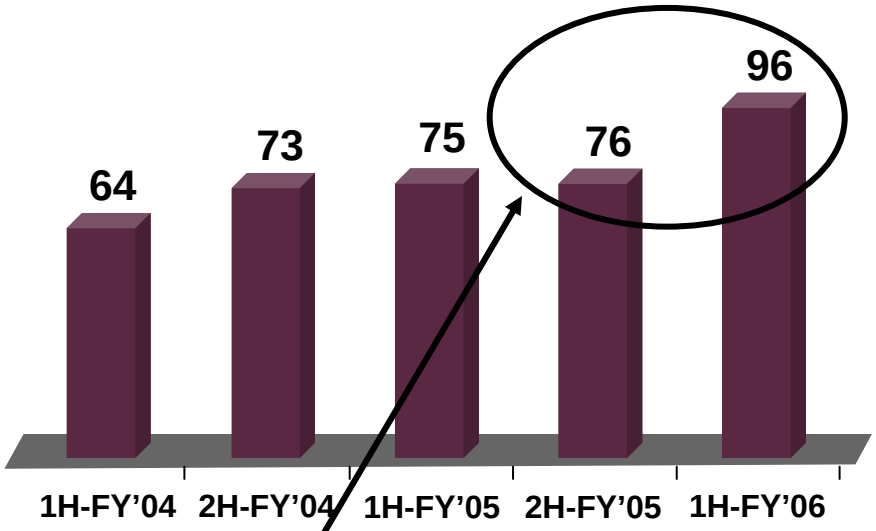
Sanyo SA800i
AGPS Kid Phone

Data from May 4th Analyst Meeting

Qualcomm CDMA Technologies

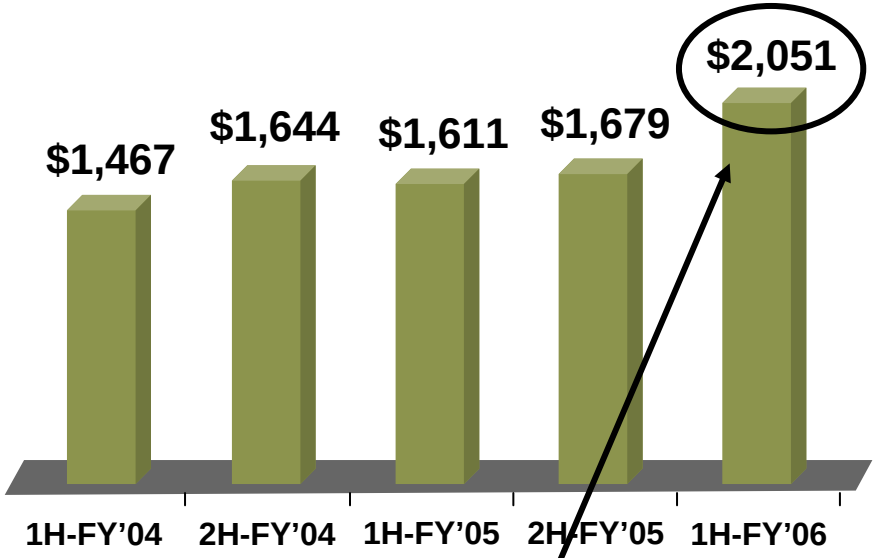
QUALCOMM Execution Continues to Generate Strong Results

Semi-Annual MSM Shipments (Millions)



Three consecutive quarters of record MSM shipments

Semi-Annual QCT Revenue Trend (Millions)



Two consecutive quarters of $1B+ revenue

Who is Qualcomm CDMA Technologies?

Leader in the CDMA / WCDMA / UMTS wireless and in the fabless manufacturing worlds

We are an "Integrated Fabless Manufacturer"

Partnering with EDA, Foundries and Assembly / Test companies to drive Process-Design Integration and a product delivery system fueled by each partner's expertise and that delivers value to all partners,

Including the end customer.

2005 Shipped our 2nd billionth chip

57,000 every hour and

Accelerating

What is the
The Integrated Fabless Manufacturing Model….

- Delivering Leading Edge Products in a Dynamic Environment
- Partnership
- Focus on technology leadership in end user markets
  - Maximum flexibility
  - Effective use of capital for design R&D
- Collaboration supply-chain partners
  - Designers, EDA, Foundries, IP and Assembly / test subcontractors

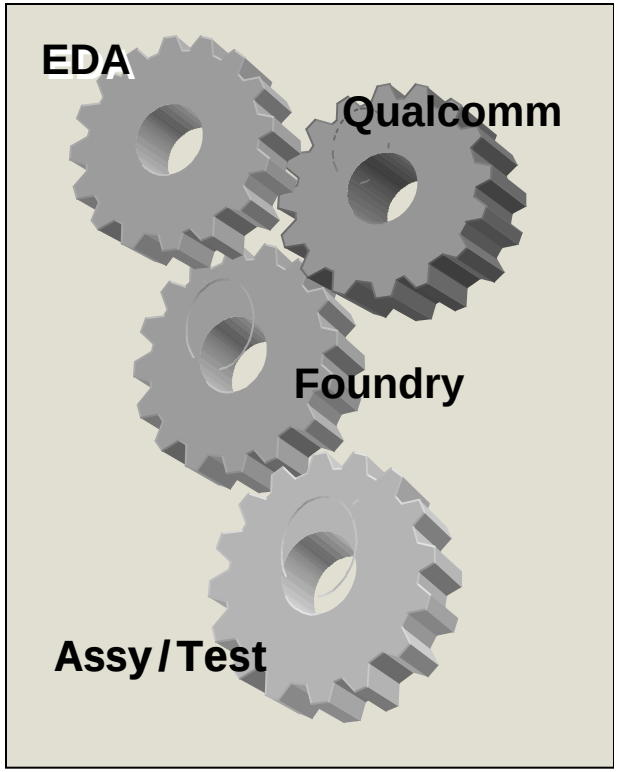
Supports standards to help the inclusion of third-party IP into the semiconductor supply chain

  - IP protection
- Enables all parties to focus on and invest in core strengths

Integrated Fabless Manufacturing – A Collaborative Effort

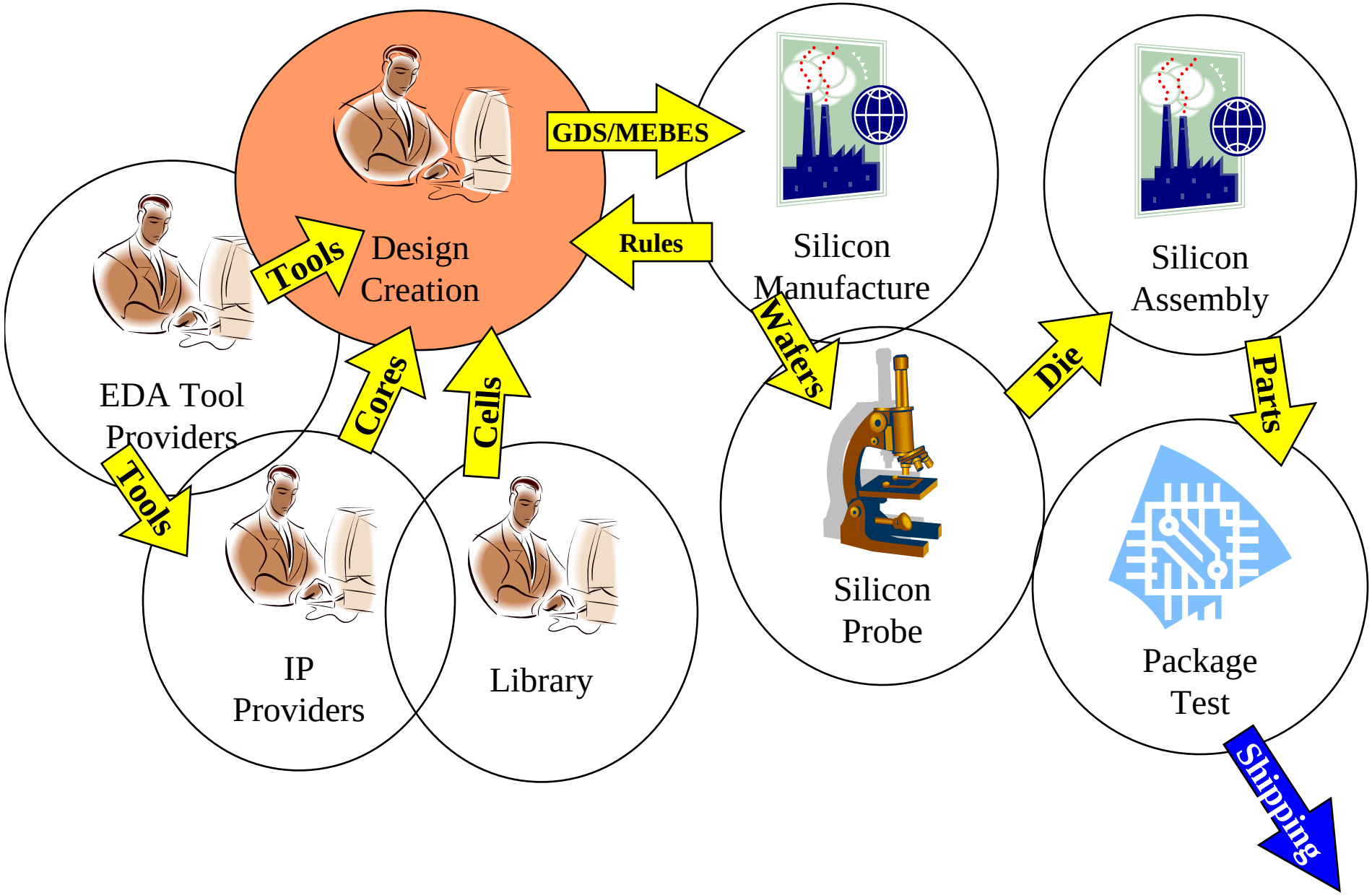
- Selecting, Evaluating, Qualifying, & Managing EDA, Foundries, and SATS is a collaborative effort
  - QCT owns the design and implementation
    - Catalyst for change and cooperation
  - EDA companies provide the tools for leveraged success
  - Foundries develop the process
    - Provide capacity and quality
  - SATS - Assembly and Test - vehicle for customer delivery
    - Assembly – packaging growing in complexity
    - Test – leverages industry platforms for low cost and high quality

The Integrated Fabless company



For Success we all must work together

Collaboration in the supply chain



Leveraging our supply chain:

At Qualcomm the Integrated Fabless Manufacturing business model drives excellence in supply chain management:

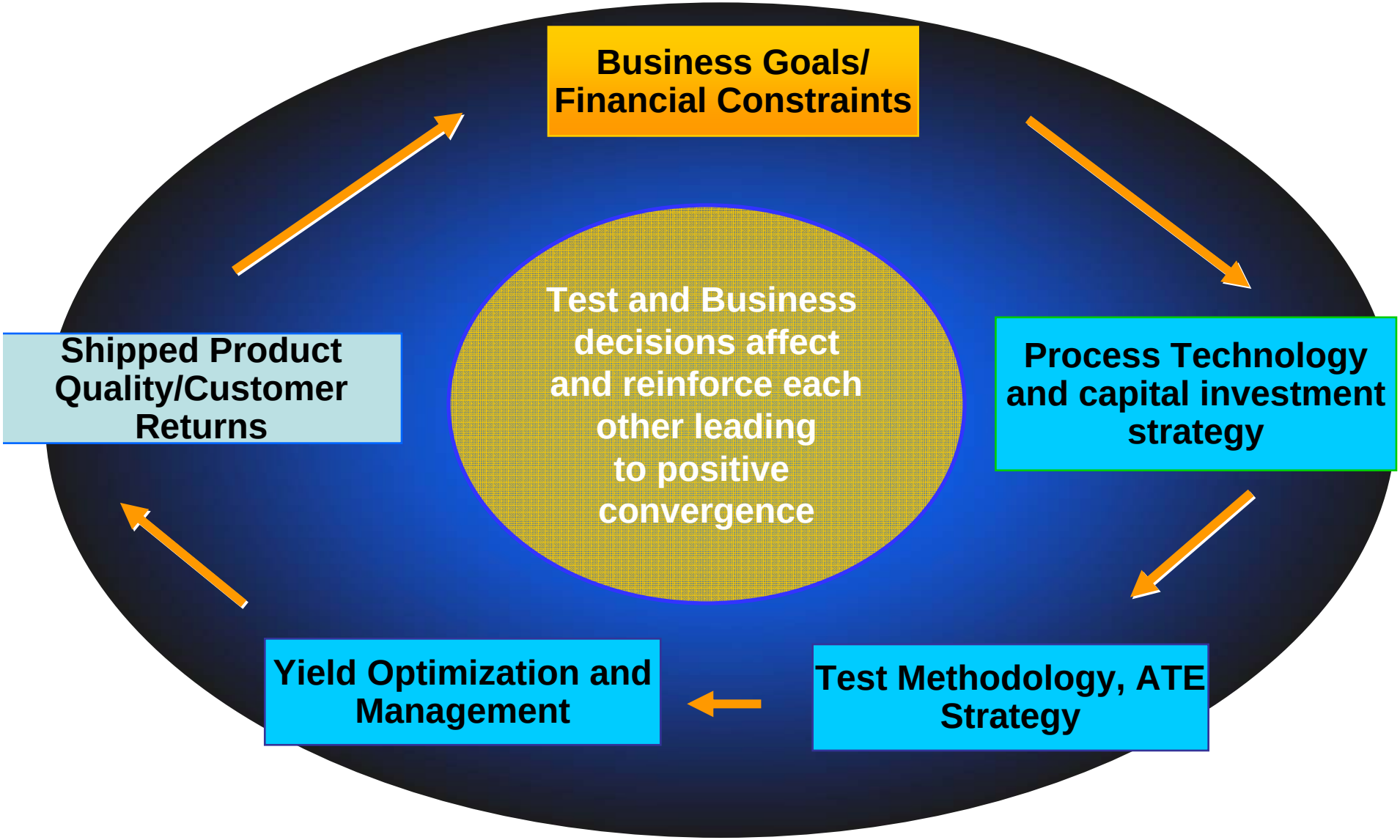
- Digital foundries – 5
- IP providers – 5+
- Analog foundries – 4
- RF foundries – 5
- Assembly suppliers – 3
- Test providers - 7
- ATE platforms - 3
- EDA companies – 15+
- Fabs – USA, Taiwan, Korea, China, Singapore
- Assembly – Korea, Philippines, Singapore, Taiwan, China, Malaysia

Die sizes-

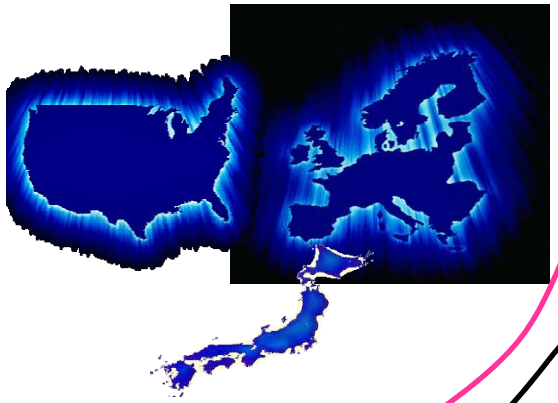
1x2 to 22x 21

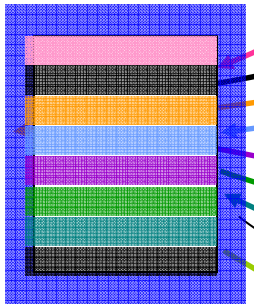
Lets talk about test

Test helps enhance value in the chain



Maximizing Value of Test





Vertically Integrated Companies

- Foundry
- Packaging
- Semiconductor
- System
- ATE
- EDA
- IP
- Equipment
- Universities

Disaggregation enables specialization and reduced cost…

…but makes it difficult to realize full potential of Test / DFY solutions

Regain value lost from disaggregation through optimal business interactions

Courtesy of Cadence - Sanjiv Taneja

Business and Test

- The test business validates product functionality and separates the good from the bad.
  - Cost efficiency demands early identification and removal of discrepant material.
  - Each step increases the cost of failure and the risk that the product will not go to market on time.
  - The cost of “test” has continued to grow with increasing product complexity
  - Customer requirements drive the test process to execute on rigorous / exhaustive test plans.
- Change is needed for success.
- Time to market and test cost must be reduced.

Test and Business

- Solutions from system models to silicon test must be automated.
  - Structural test has an almost direct link from the EDA tools to test and yield
  - Linkage must be driven into the fab's automated defect detection systems.
  - Data sets optimized for statistical process / decision making
- Functional test have a poor correlation path to the ATE
  - Improve modeling capabilities to achieve the reliability and predictability.
- Advancements have been made; however, for full optimization of test cost:
  - EDA tools and ATE correlation must come together to reduce time to market and cost.

The industry is a buzz with the implications of test

Recent headlines say it loud and clear. Test is just not test anymore.

- **EDA conversion tools integrated with ATE software**
- **How much test compression is enough?**
- **Low-power IC test can be trying**
- **Tackling test challenges for low-power design**
- **Test takes new role in yield improvement**

Issues in the Real world

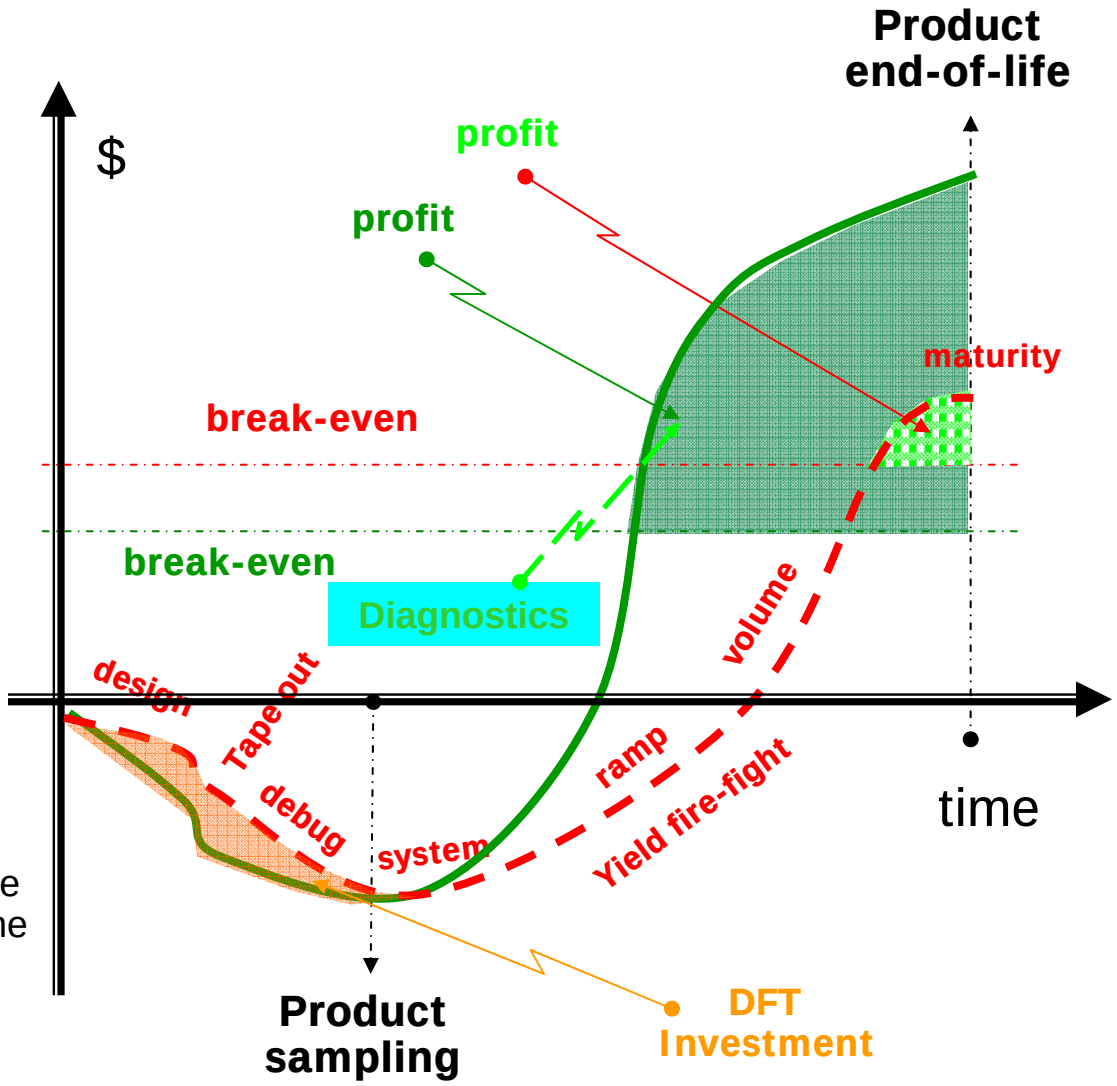
- Bit cell failures continue to dominate – need effective redundant memory scheme, ECC, and test strategy.
- Iddq control more difficult with DSM geometry. Delta Iddq, group Iddq, and “intelligent test” are paths forward.
- Broken Scan Chains – ATPG failures. Easy to find
- “Defective Scan Chains” - Voltage Sensitive Hold-Time Violations – Bridges – Route Defects Dominate
- Test Escapes – Customer Returns – continue – Mostly Timing reported, or lack of coverage (structural or functional)
- Temperature Sensitive Delay-Faults (Vias) have been found and presented in multiple journals
- More Process Monitors (R.O.s, Delay Lines, Canary Circuits) in use
- Systematic Design-based faults/defects present like random fail signatures

Business Realities

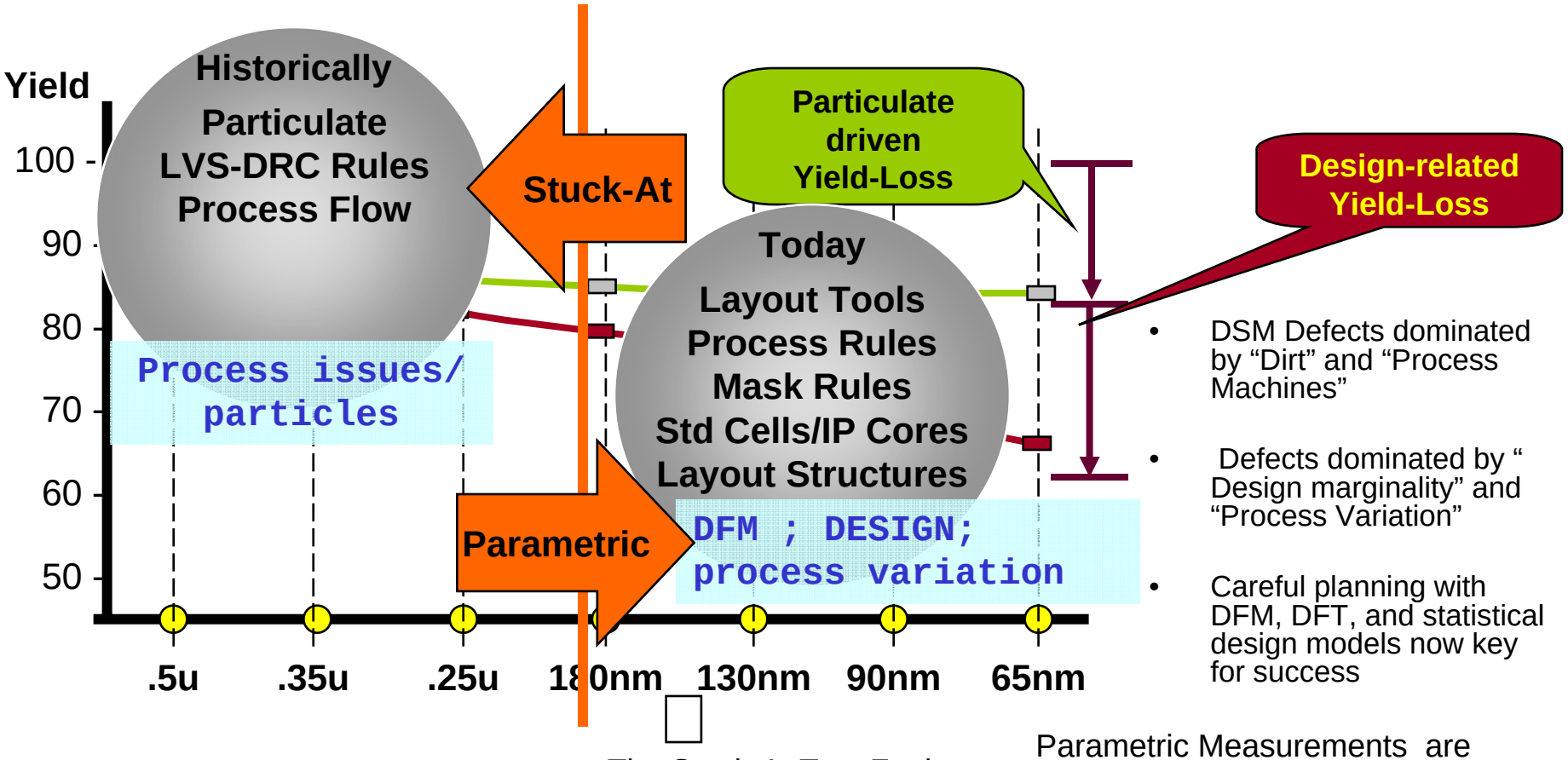
Yield and Business Realities

- Return on the (design & development) investment comes when there is volume
- Accelerated yield learning
  a) Decreases the investment and Shortens the investment period
  b) Increases and Prolongs the return period
- Product life, and ASP, are driven by market conditions

- Yield Learning Goes Straight to the Bottom Line
  – Anything that can be done to improve yield and yield learning is good for the business



Yield - Yesterday & Today



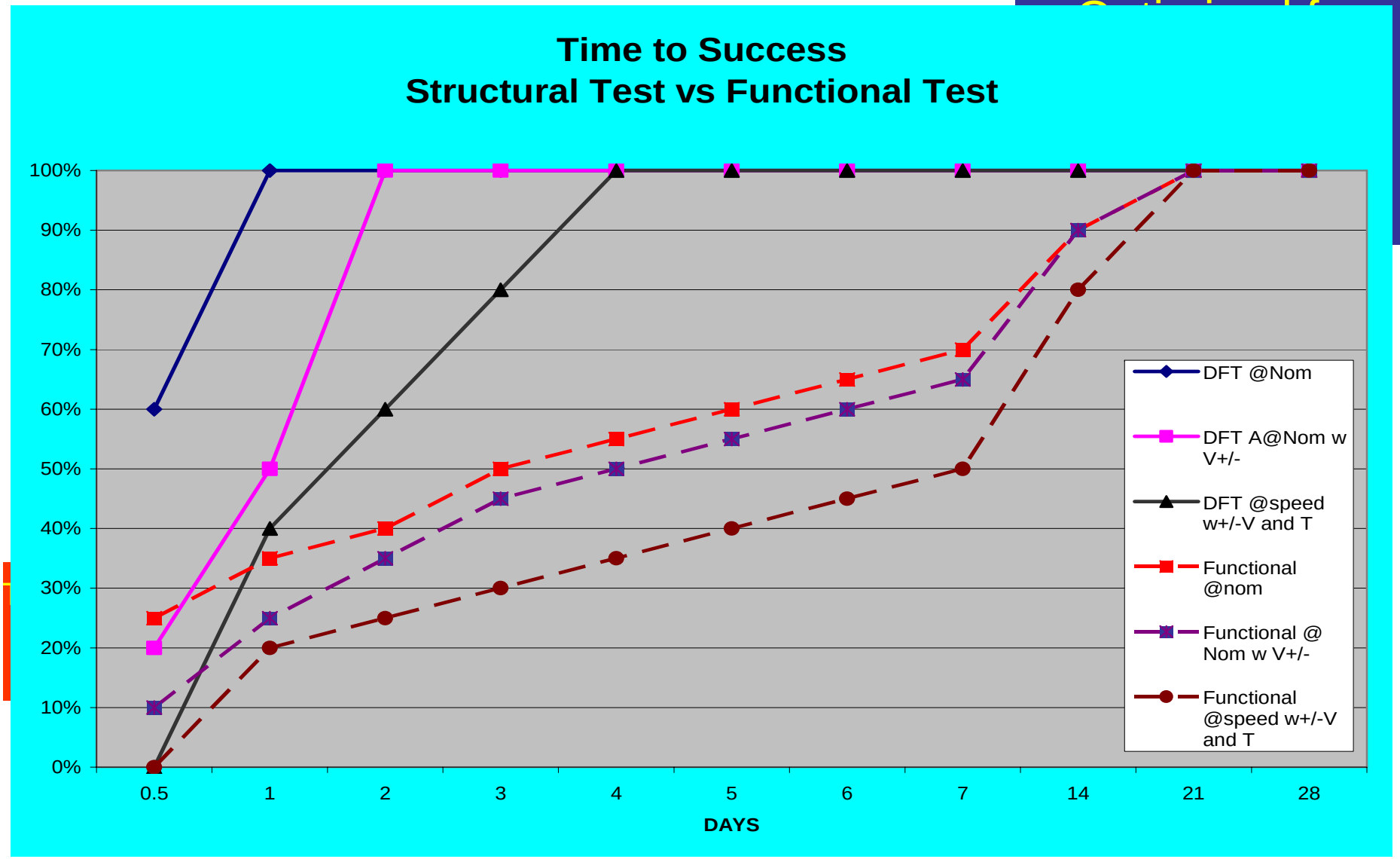
- DSM Defects dominated by “Dirt” and “Process Machines”
- Defects dominated by “ Design marginality” and “Process Variation”
- Careful planning with DFM, DFT, and statistical design models now key for success

Almost all of the new Yield-Loss issues can be related back to Systematic Design-based loss mechanisms & drivers

The Stuck-At Test Fault Model is less effective for DFM-driven loss

Parametric Measurements are more effective for DFM-driven loss

Modern Test is...



Business Value of Test

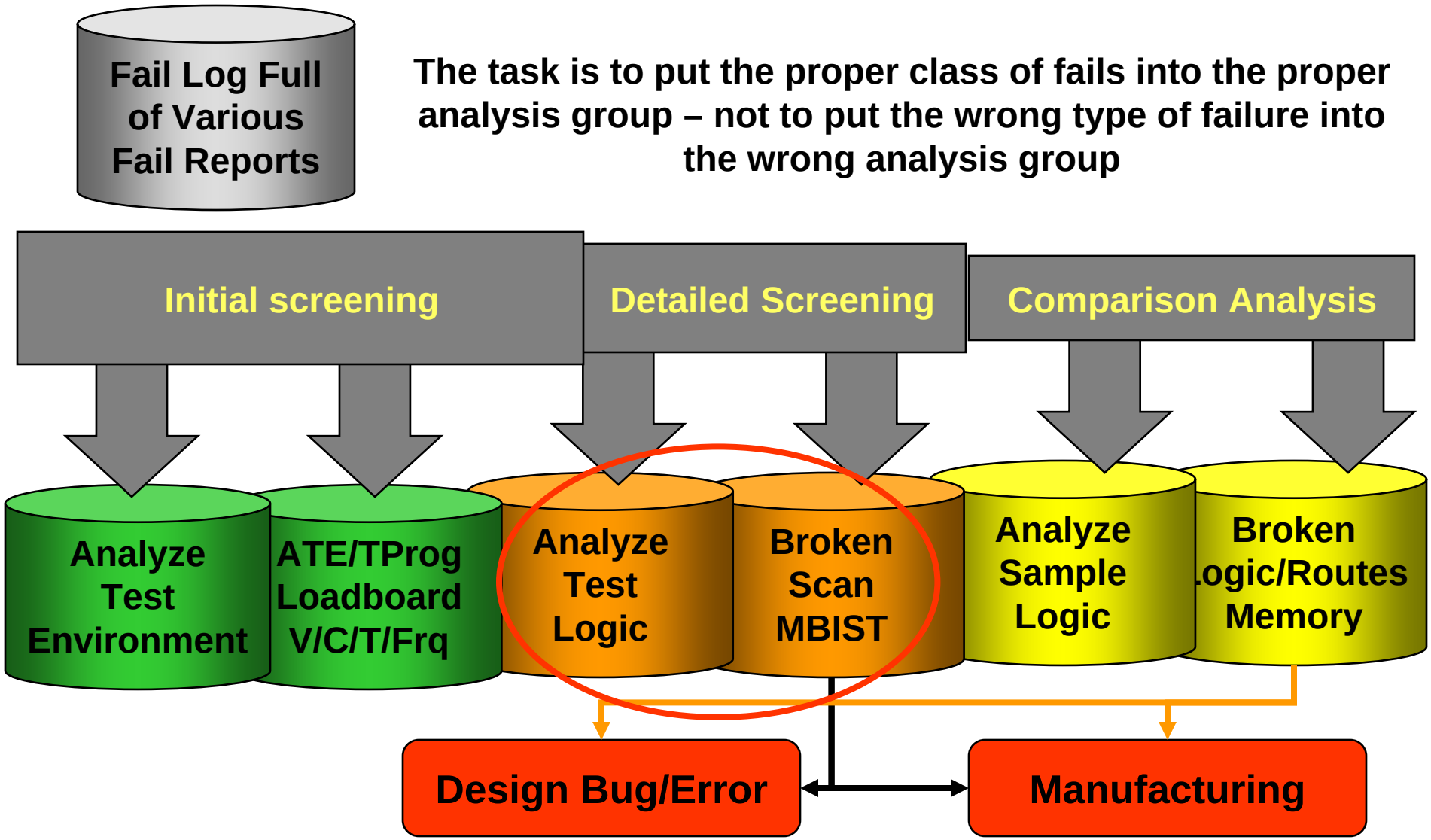
New commercial test technologies- leveraging DFT in designs are available from Verigy (Agilent) , Teradyne, Inovys, and Advantest .

The optimized systems improve ability to leverage structural test, offer higher level diagnostics and lower the overall cost of test.

Accelerate Yield - Leveraged diagnostics from wafer probe can help accelerate yield by weeks or months.

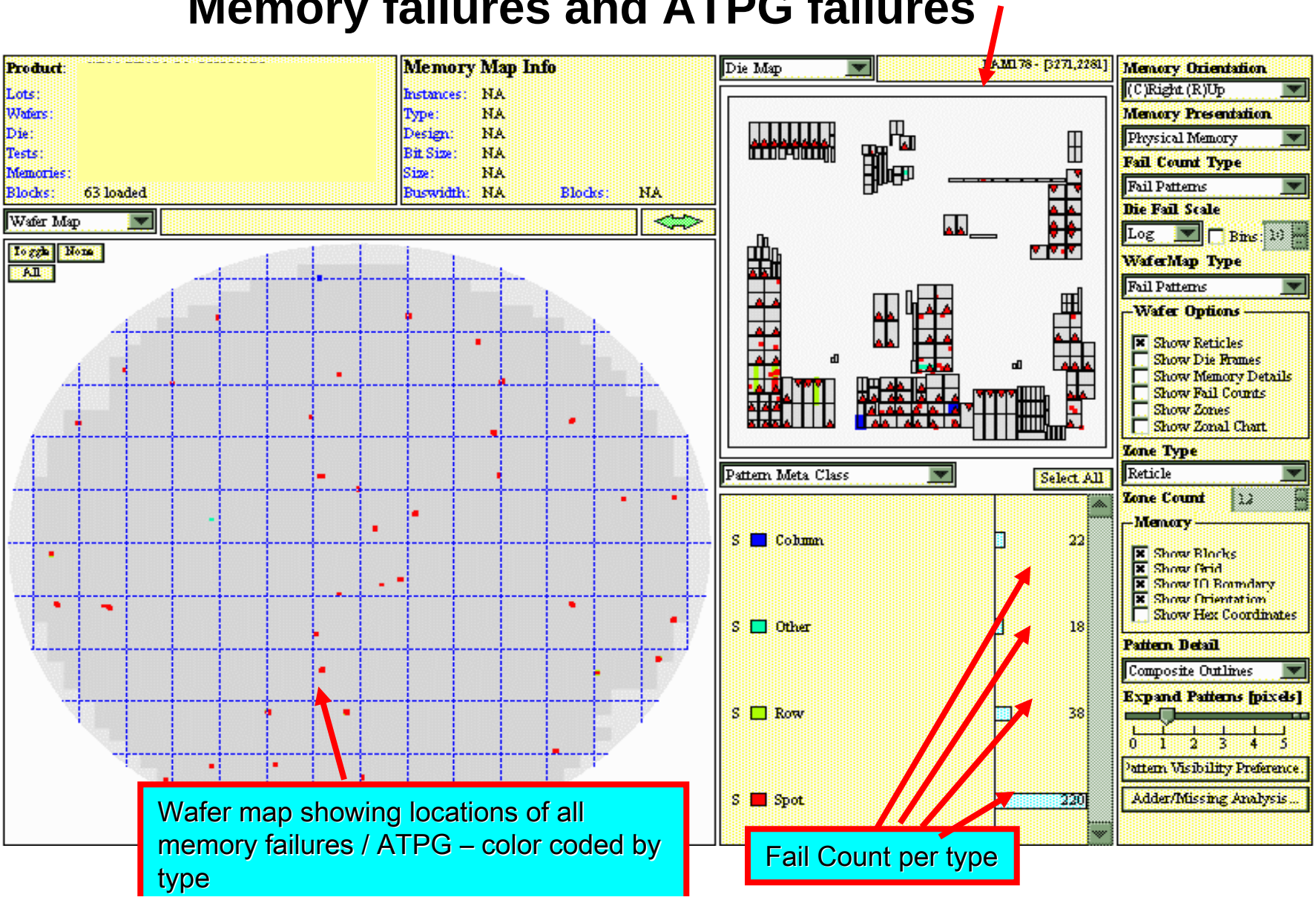
- **Leveraging wafer probe data back to KLA data --- Months or Quarters.**
- **Value = volume *savings*time**

Making Sense of it All



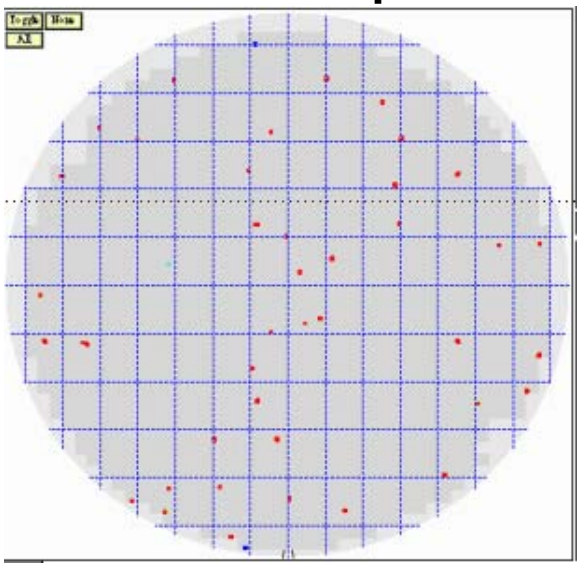
Driving yield with wafer level bit map sharing

Memory failures and ATPG failures

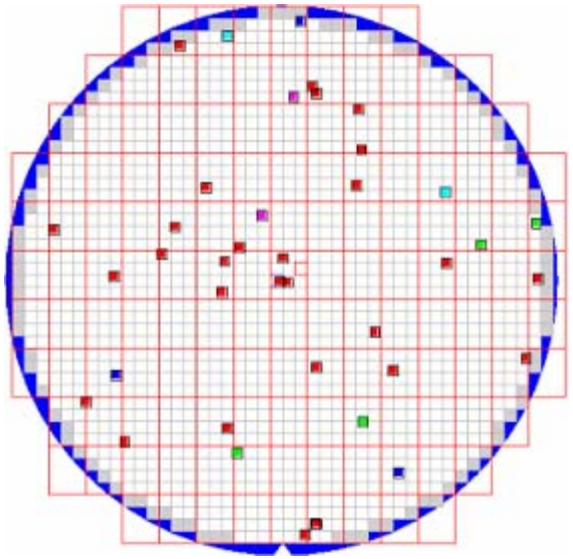


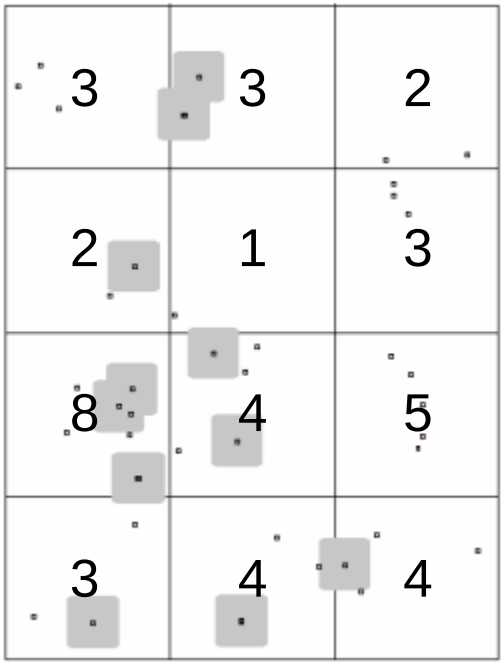
Comparing Wafer Level Bitmaps to KLA Results

CP bit map

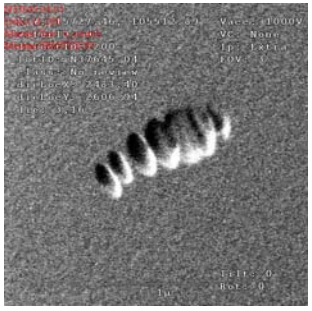


Inline defect map

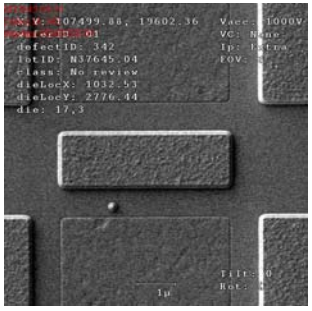




u_scratch



Pre-layer particle

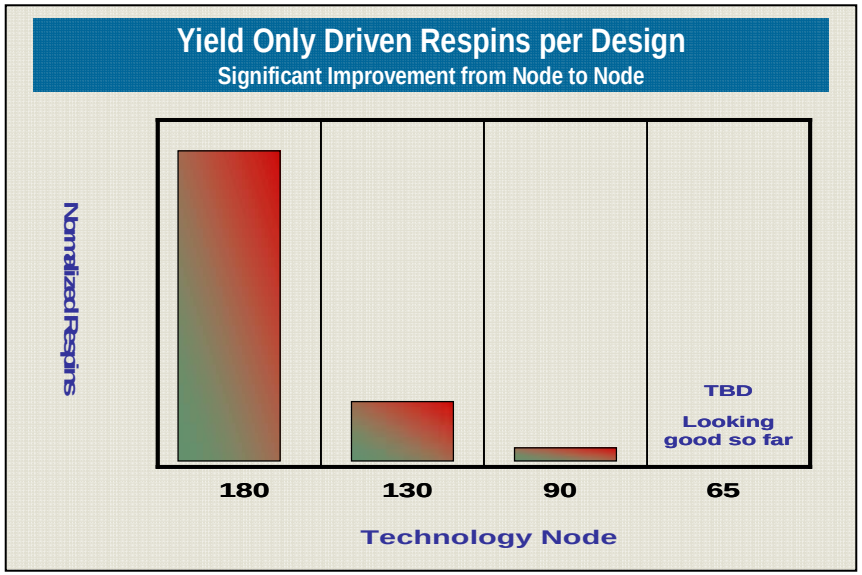


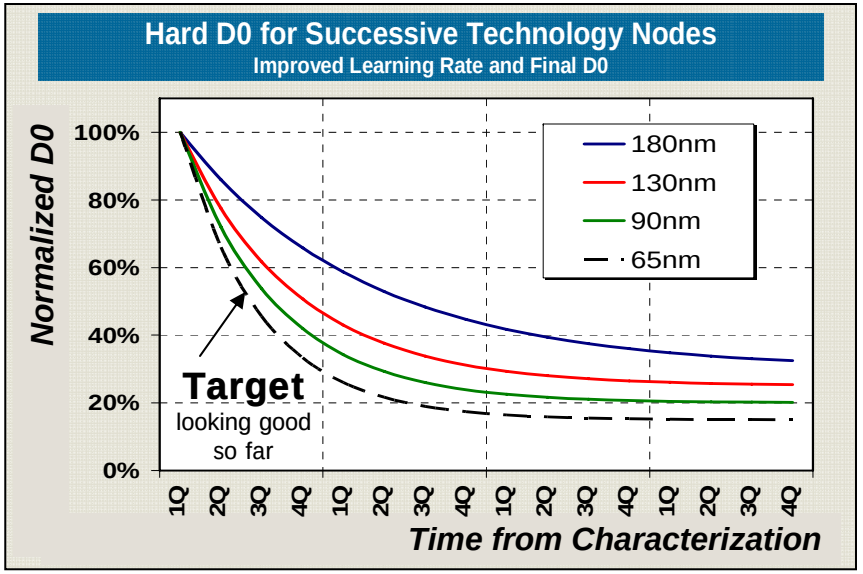
Surface PA

Yield Leaning and Tool development

- Test, Debug & FA Infrastructure
  - Excellent skill mix, people & tools
  - Structured procedures
  - ✓ *Accelerated feedback*
  - ✓ *Start low volume early to learn yield*
- Partnering Relationship
  - Very tight coupling with foundries
  - Aggressive goals
  - ✓ *Accelerated learning cycles and corrective action*
- Good Design
  - Extensive use of DFM Guidelines
  - Internal tools and utilities
  - ✓ *Conservative Lay Out practices*

It Worked for us …. So Far





THE END GAME

- The **TEST** business must help drive ON TIME, high quality, cost effective products to the markets:
  - We have the tools, the testers and the knowledge to do so.

- We must drive yield so that we deliver additional free cash is the system is the solution.

- Results:
  - Industry innovation accelerated. Competition based on Quality and time to market
  - More designs willing in the market drives more silicon in Fabs – everybody wins.
  - More business for us…