Development of a Next Generation Probe Card Maintenance Process for Wafer Sort

Zhiming Mei

Intel Corporation

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Outline

- Current PCM state in high volume manufacturing
- Establish successful PCM process
  - Tool capability and risks
  - Performance Evaluation Methodology
  - Established process control systems
- The challenge: Correlation between sort and PCM results on probe cards
- Summary/key message

Current PCM state in high volume manufacturing (HVM)

- Metrology tool usage is no longer like a lab tool as in validation sites:
  - Now a standard part of HVM
    - Goal is quick determination as to whether the probecard was the source of failure in a sort module
    - 24x7 utilization, high volume of probecards
    - Large user base with minimum tool operation knowledge
    - Multiple toolsets
  - Metrology needs to encompass increasing complexity
    - Multiple products
    - More complex sort failures due to increased test capability

Current state in high volume manufacturing (HVM) cont.

- Current PCM equipment has limited Process Control Capability
  - Access to several databases is required to get basic information
    - Wafer test (Sort) failure details
    - Metrology data history
    - Analysis of probe marks on wafer

- Goal: Develop a Probe Card Metrology (PCM) Process that meets HVM needs in both quality and throughput

Establishing successful PCM

- Develop critical capabilities to meet technology needs over multiple generations
- Evaluate performance
  - Engineering/enabling
  - Robust for Manufacturing
- Ensure Process Control Capability

Develop critical capability

- Determine which metrology capabilities are essential to sort and probing process to ensure you get the desired result → detect sort failures
- Evaluate risk of not copying sort conditions exactly
  - Ex: Are their unique probecard failures at elevated temperatures that will be missed in PCM analysis?

Establishing successful PCM

- Determine critical technology needs over multiple generations
- Evaluate performance
  - Engineering/enabling
  - Robust for Manufacturing
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Metrology tool performance evaluation

- Evaluation includes multiple phases:
  - Early engineering capability
    - some instability and manual assists
    - Establishing initial capability
  - Technology and transfer certifications
    - Higher volumes → longer time scale
    - Evaluation of HVM variances
      - Tool fleet variation
      - Site to site variation
      - Probe card
      - Operator
      - Within tool health over time, etc.

Expected Outcome: A "Certified" process that is HVM capable and robust w/o process tweaks.

Metrology tool performance evaluation

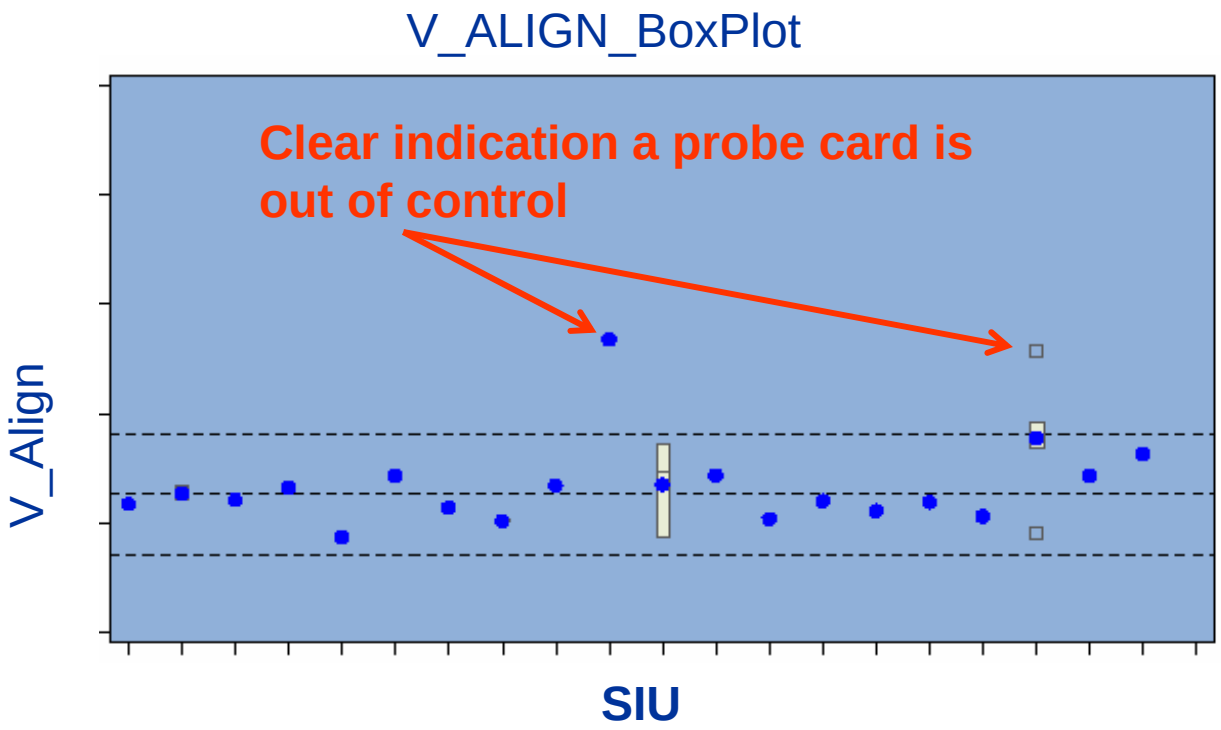
- Suggested Tool reliability indicators
  - Diagnostics and calibration: enhance self-diag and calibration to *minimize human error*
  - Repair and maintenance: easy repair and maintenance to *minimize downtime and cost*
  - Failure frequency and pareto: focus on high failure modes to *maximize tool availability*
  - Training and response flow chart: focus on essential training to *minimize impact to ops*

Easy to decide, fix and eliminate tool related issues

Establishing successful PCM

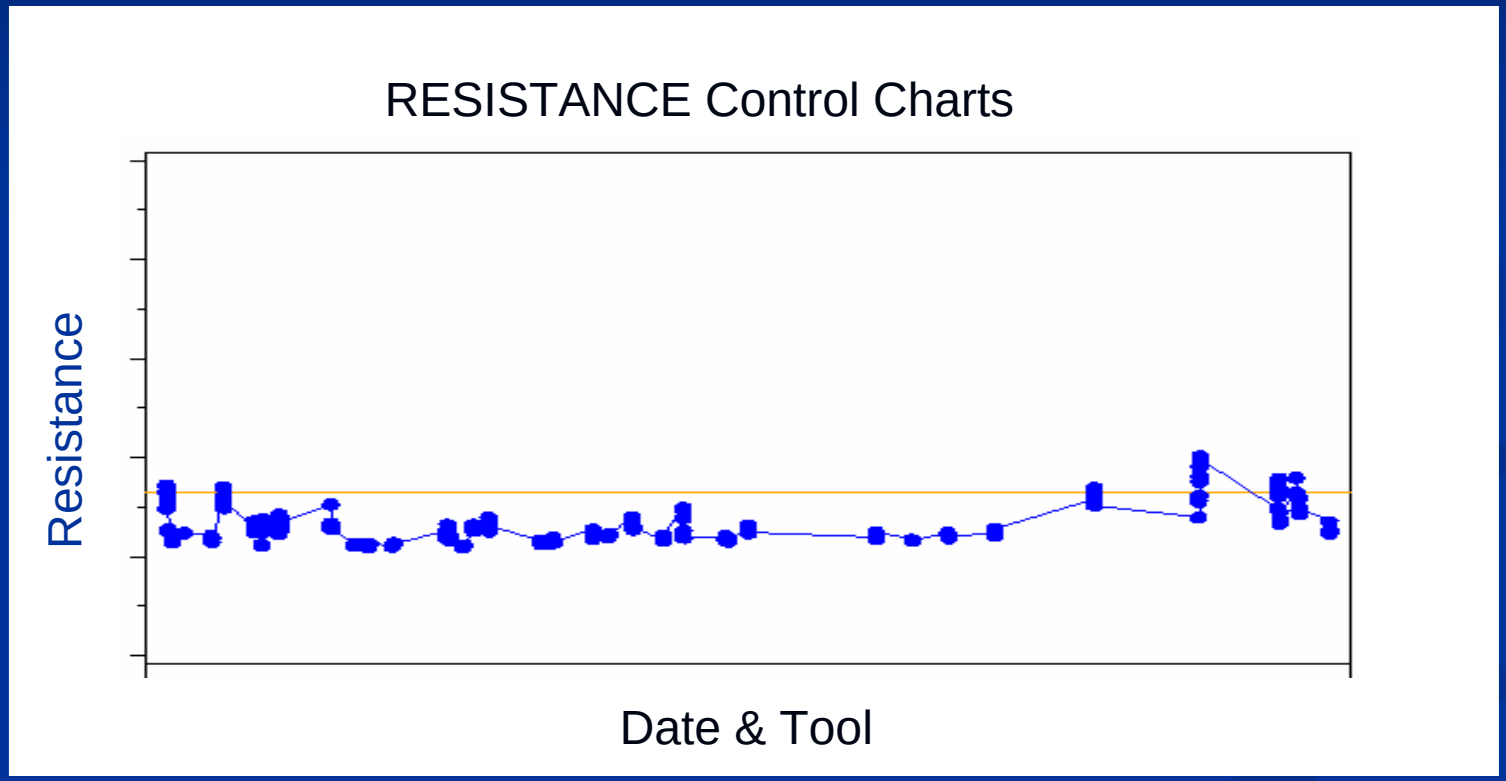
- Determine critical technology needs over multiple generations
- Evaluate performance
  - Engineering/enabling
  - Robust for Manufacturing
- Ensure Process Control Capability

Process control systems



⇨**Process control ensures both tool and probe card fleet are in control**

Example: Measuring control card across metrology fleet



SPC card monitors metrology tool fleet over time, ensure tool fleet stable and matched

Metrology goal

- Quick determination as to whether the probe card was the source of failure in a sort module
- Key enabler/Key challenge: Establishing a strong correlation between metrology results and results in the sort module

Correlation of metrology to wafer sort

- Correlation is essential but not straightforward
  - many factors are different → introduce metrology detectable signals for sort failures
  - Pass-Pass: a probe card that passes metrology should pass a sort setup
  - Fail-Fail: a probe card related sort failure should not pass relevant metrology tests
  - Currently, correlation studies require manual access to various data sources.

Correlation of metrology to wafer sort

- Correlation evaluation is difficult to track
  - PCM only addresses failures related to the probe card.
    - Excluded from analysis: tester, prober, test program and marginality in incoming Silicon or product design.
    - Additional variability due to probe card fleet.
  - Data are located at various sources: metrology, probe card inventory database, sort failures
- Even so, limited results to date show promise
  - Case study results

Case 1

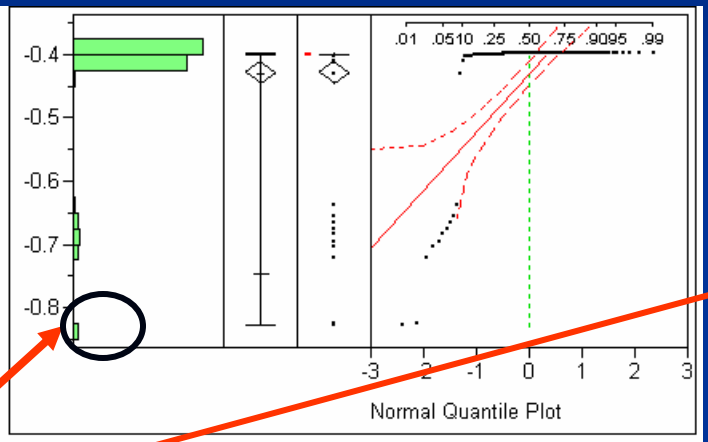
- Bin99 sort failures: over 3 months, 6 cards have multiple Bin99 failures cross multiple testers
  - Bin99 is a misc sort failure and could be product/tester dependent
  - Drilled down the failure message inside log files => “power supply sense open”
  - Probe cards passed metrology tool on power sense lines per design
  - Mis-correlation?
    - No. Further investigation showed the sense lines caused B99 were not tested on metrology tool, probe card design didn’t include them (they are part of possible sense line pins).
    - No further such failures after these pins were added into the test

- **An integrated database with sort and metrology data will help to track and flag such mis-correlation events easily, then to enable engineering to close gaps**

Case 2

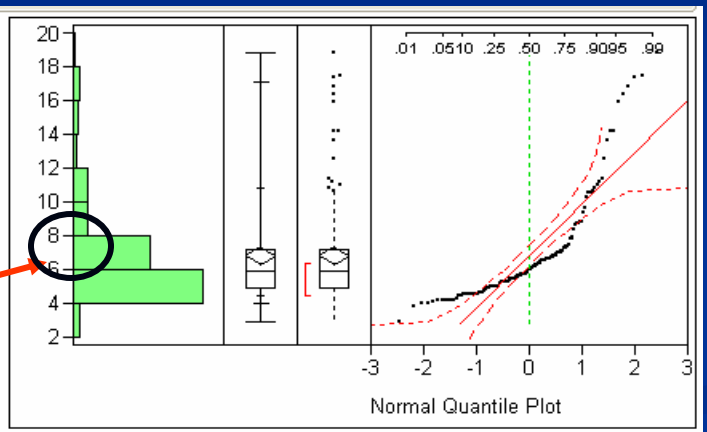
- Two test channels open at sort but passed on metrology tool
  - Two channels measured ~2X higher than the majority at sort

Sort failures pins



Quantiles		
100.0%	maximum	-0.3980
99.5%		-0.3980
97.5%		-0.3980
90.0%		-0.3990
75.0%	quartile	-0.3994
50.0%	median	-0.4005
25.0%	quartile	-0.4015
10.0%		-0.4308
2.5%		-0.7459
0.5%		-0.8285
0.0%	minimum	-0.8285

Sort data



Quantiles		
100.0%	maximum	18.795
99.5%		18.795
97.5%		17.095
90.0%		10.837
75.0%	quartile	7.187
50.0%	median	5.914
25.0%	quartile	4.926
10.0%		4.412
2.5%		3.986
0.5%		2.900
0.0%	minimum	2.900

Metrology data

Metrology and sort are not measuring the same thing, Need to improve test methods to be able to compare

Case 3

- Ch320 failed for high cres (Bin30) on one card, but other cards are ok
- Probecard passed metrology tests

ProbeID	Trace	Electric	Resistar
610	120	2.9	3.949
582	121	1.5	4.869
599	122	2.367	4.856
617	123	-0.667	4.386
602	124	-0.283	4.384
574	125	-0.667	4.402
591	126	-2	4.021
609	127	1.067	5.537
569	320	0.533	15.234
570	321	7.4	6.66
868	1A3	-7.167	0.854
1130	1A33	Not Testec	0.296
1131	1A33	Not Testec	0.296

Metrology show ch 320 has much higher path resistance

Trace	ResistVal
120	6.183
121	8.514
122	7.973
123	6.767
124	6.228
125	7.178
126	6.052
127	6.516
320	4.442
321	4.723

However ch 320 on another card has "normal" path resistance

Probecard variation can cause mis-correlation, need to minimize such variation

Case 4

- Bin15 sort failure on part of wafer on probecard #1
  - Resort wafer with a different probecard, no Bin15
  - Probecard #1 passed all metrology tests
- Further investigation show this is a combination of variations from probecard, bump height and probing process.

- **Easy access to various data sources can improve/optimize our process: bump inspection data, probecards data and sort data.**

Key messages

- Establish correlation to sort failures
  - Features enable test methods optimization
  - Automation solution for easy data access and analysis along with sort data
- Develop critical capability
  - Provide modular options to suit various customer's needs
  - Low cost by remove non-critical components
- Improve tool reliability
  - Minimize tool related issues on testing and results (self checks for setup, system key components etc.)
  - Minimize human error (self-diag & calibration, easy repair etc.)
- HVM friendly features to improve the process
  - Minimize human intervention needed for HVM variance
  - Minimize tool to tool variation allow process transfer